EE247  
Lecture 16

- **D/A Converters (continued)**
  - DAC reconstruction filter

- **ADC Converters**
  - Sampling
    - Sampling switch considerations
      - Thermal noise due to switch resistance
      - Clock jitter related non-idealities
      - Sampling switch bandwidth limitations
      - Switch conductance non-linearity induced distortion
    - Sampling switch conductance dependence on input voltage
    - Clock voltage boosters
    - Sampling switch charge injection & clock feedthrough

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**Summary Last Lecture**

- **D/A converters**
  - Practical aspects of current-switched DACs (continued)
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations
  - Self calibration techniques
    - Current copiers
    - Dynamic element matching
**DAC In the Big Picture**

- **Learned to build DACs**
  - Convert the incoming digital signal to analog
- **DAC output → staircase form**
- **Some applications require filtering (smoothing) of DAC output**
  → **Reconstruction filter**

**DAC Reconstruction Filter**

- **Need for and requirements depend on application**

- **Tasks:**
  - Correct for sinc droop
  - Remove “aliases” (stair-case approximation)
Reconstruction Filter Options

- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth $B \ll f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band $\sin(x)/x$ amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter Example: Voice-Band CODEC Receive Path

Note: $f_{\text{sig}}^{\text{max}} = 3.4$ kHz
$f_{\text{DAC}} = 8$ kHz
$\sin(\pi f_{\text{sig}}^{\text{max}} x T_s)/(\pi f_{\text{sig}}^{\text{max}} x T_s)$
= -2.75 dB droop due to DAC $\sin(x)/x$ shape

Ref: D. Senderowitz et. al., “A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip,”
Summary
D/A Converter

• D/A architecture
  – Unit element – complexity proportional to $2^B$, excellent DNL
  – Binary weighted- complexity proportional to $B$, poor DNL
  – Segmented- unit element MSB($B_1$)+ binary weighted LSB($B_2$)
    $\rightarrow$ Complexity proportional ($(2^{B_1-1}) + B_2$) -DNL compromise between the two

• Static performance
  – Component matching

• Dynamic performance
  – Time constants, Glitches

• DAC improvement techniques
  – Symmetrical switching rather than sequential switching
  – Current source self calibration
  – Dynamic element matching

• Depending on the application, reconstruction filter may be needed

What Next?

• ADC Converters:
  – Need to build circuits that "sample"
  – Need to build circuits for amplitude quantization

Anti-Aliasing Filter
Sampling + Quantization
"Bits to Staircase"
Reconstruction Filter
Analog-to-Digital Converters

• Two categories:
  – Nyquist rate ADCs \( f_{\text{sig}}^{\text{max}} \approx 0.5f_{\text{sampling}} \)
    • Maximum achievable signal bandwidth higher compared to oversampled type
    • Resolution limited to <14 bits
  – Oversampled ADCs \( f_{\text{sig}}^{\text{max}} < < 0.5f_{\text{sampling}} \)
    • Maximum achievable signal bandwidth significantly lower compared to nyquist
    • Maximum achievable resolution high (18 to 20 bits!)
Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage $v_{IN}$ onto the capacitor $C$

  → Output Dirac-like pulses with amplitude equal to $V_{IN}$ at the time of sampling

- In practice not realizable!

Ideal Track & Hold Sampling

- $V_{out}$ tracks input for $\frac{1}{2}$ clock cycle when switch is closed
- Ideally acquires exact value of $V_{in}$ at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)
**Ideal T/H Sampling**

- Continuous Time
- T/H signal (Sampled-Data Signal)
- Clock
- Discrete-Time Signal

**Practical Sampling Issues**

- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of $\phi_1$)
- Finite $R_{sw} \rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection & clock feedthrough
Sampling Circuit kT/C Noise

- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in \( \text{Total noise variance} = \frac{kT}{C} @ \text{the output} \) (see noise analysis in Lecture 1)
- In high resolution ADCs with such sampling circuit right at the input, \( \frac{kT}{C} \) noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times slightly larger compared to quantization noise:

Assumption: \( \rightarrow \) Nyquist rate ADC

For a Nyquist rate ADC: Total quantization noise power \( \approx \frac{\Delta^2}{12} \)

Choose \( C \) such that thermal noise level is less (or equal) than \( Q \) noise

\[
\frac{k_B T}{C} \leq \frac{\Delta^2}{12}
\]

\[
\rightarrow \quad C \geq 12k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2
\]

\[
\rightarrow \quad C \geq 12k_B T \times \frac{2^{4B}}{V_{FS}^2}
\]
Sampling Network kT/C Noise

\[ C \geq 12k_B T \frac{2^B B}{V_{FS}^2} \]

<table>
<thead>
<tr>
<th>B</th>
<th>( C_{\text{min}} ) (( V_{FS} = 1V ))</th>
<th>( C_{\text{min}} ) (( V_{FS} = 0.5V ))</th>
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<tbody>
<tr>
<td>8</td>
<td>0.003 pF</td>
<td>0.012 pF</td>
</tr>
<tr>
<td>12</td>
<td>0.8 pF</td>
<td>2.4 pF</td>
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<tr>
<td>14</td>
<td>13 pF</td>
<td>52 pF</td>
</tr>
<tr>
<td>16</td>
<td>206 pF</td>
<td>824 pF</td>
</tr>
<tr>
<td>20</td>
<td>52,800 pF</td>
<td>211,200 pF</td>
</tr>
</tbody>
</table>

The large area required for \( C \) → limit highest achievable resolution for Nyquist rate ADCs
Oversampling results in reduction of required value for \( C \) (will be covered in oversampled converter lectures)

Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of \( \phi_1 \))
- Finite \( R_{sw} \) → limited bandwidth → finite acquisition time
- \( R_{sw} = f(V_{in}) \) → distortion
- Switch charge injection & clock feedthrough
Clock Jitter

• So far: clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)

• Real clock generator → some level of variability

• Variability in T causes errors
  – "Aperture Uncertainty" or "Aperture Jitter"

• What is the effect of clock jitter on ADC performance?

Clock Jitter

• Sampling jitter adds an error voltage proportional to the product of (t_j - t_0) and the derivative of the input signal at the sampling instant.

\[ x(t) \quad x'(t_0) \]

actual sampling time \( t_j \)

nominal (ideal) sampling time \( t_0 \)
Clock Jitter

• The error voltage is

\[ e = x'(t_0)(t_j - t_0) \]

• Does jitter matter when sampling dc signals (\(x'(t_0)=0\))? 

Effect of Clock Jitter on Sampling of a Sinusoidal Signal

**Sinusoidal input**

- **Amplitude:** \( A \)
- **Frequency:** \( f_s \)
- **Jitter:** \( dt \)

\[ x(t) = A \sin(2\pi f_s t) \]

\[ x'(t) = 2\pi f_s A \cos(2\pi f_s t) \]

\[ |x'(t)|_{\text{max}} \leq 2\pi f_s A \]

*Then:*

\[ |e(t)| \leq |x'(t)|_{\text{max}} dt \]

\[ |e(t)| \leq 2\pi f_s A dt \]

**Worst case**

- \( A = \frac{A_{FS}}{2} \)
- \( f_s = \frac{f_s}{2} \)

\[ |e(t)| \ll \frac{A_{FS}}{2^{b+1}} \]

\[ dt \ll \frac{1}{2^{b} f_s} \]

<table>
<thead>
<tr>
<th># of Bits</th>
<th>( f_s )</th>
<th>( dt \ll )</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1 MHz</td>
<td>78 ps</td>
</tr>
<tr>
<td>16</td>
<td>20 MHz</td>
<td>0.24 ps</td>
</tr>
<tr>
<td>12</td>
<td>1000 MHz</td>
<td>0.07 ps</td>
</tr>
</tbody>
</table>
Statistical Jitter Analysis

• The worst case looks pretty stringent … what about the “average”?
• Let’s calculate the mean squared jitter error (variance)
• If we’re sampling a sinusoidal signal
  \[ x(t) = A \sin(2\pi f_x t), \]
  then
  \[ x'(t) = 2\pi f_x A \cos(2\pi f_x t) \]
  \[ \mathbb{E}\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2 \]

• Assume the jitter has variance \( \mathbb{E}\{(t_j - t_0)^2\} = \tau^2 \)

Statistical Jitter Analysis

• If \( x'(t) \) and the jitter are independent
  \[ \mathbb{E}\{[x'(t)(t_j - t_0)]^2\} = \mathbb{E}\{[x'(t)]^2\} \mathbb{E}\{(t_j - t_0)^2\} \]

• Hence, the jitter error power is
  \[ \mathbb{E}\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2 \]

• If the jitter is uncorrelated from sample to sample, this “jitter noise” is white
Statistical Jitter Analysis

\[ DR_{\text{jitter}} = \frac{A^2}{2\pi f_s A^2 \tau} \]
\[ = \frac{1}{2\pi f_s \tau^2} \]
\[ = -20 \log_{10}(2\pi f_s \tau) \]

Example: ADC Spectral Tests

Summary
Effect of Clock Jitter on ADC Performance

• In cases where clock signal is provided from off-chip → have to choose a clock signal source with low enough jitter.
• On-chip precautions to keep the clock jitter less than single-digit pico-second:
  – Separate supplies as much as possible
  – Separate analog and digital clocks
  – Short on-chip inverter chains between clock source and destination
• Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  – RMS noise proportional to input signal frequency
  – RMS noise proportional to input signal amplitude
→ In cases where clock jitter limits the dynamic range, it’s easy to tell, but may be difficult to fix...

Practical Sampling Issues

• Switch induced noise due to M1 finite channel resistance
• Clock jitter (edge variation of \( \phi_1 \))
  => Finite \( R_{sw} \) → limited bandwidth → finite acquisition time
• \( R_{sw} = f(V_{in}) \) → distortion
• Switch charge injection & clock feedthrough
**Sampling Acquisition Bandwidth**

- The resistance $R$ of switch $S_1$ turns the sampling network into a lowpass filter with finite time constant:
  \[ \tau = RC \]

- Assuming $V_{in}$ is constant or changing slowly during the sampling period and $C$ is initially discharged.

- Need to allow enough time for the output to settle to less than 1 ADC LSB → determines minimum duration for $\phi_1$ or maximum ADC operating freq.

\[ v_{out}(t) = v_{in}(1 - e^{-t/\tau}) \]

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**Sampling: Effect of Finite Switch On-Resistance**

$V_{in}^n - V_{out}^n \ll \Delta$ since $V_{out}^n = V_{in}^n(1 - e^{-t/\tau})$

$\rightarrow V_{in}e^{-t/\tau} \ll \Delta$ or $\tau \ll \frac{T_s}{2} \ln \left( \frac{V_{in}}{\Delta} \right)$

Worst Case: $V_{in} = V_{FS}$

\[
\tau \ll \frac{T_s}{2} \ln \left( \frac{2^B - 1}{2^B} \right) \approx \frac{0.72 \times T_s}{B}
\]

\[
R \ll \frac{1}{2f \cdot C \ln \left( 2^B - 1 \right)} \approx \frac{0.72}{BfC}
\]

Example:

- $B = 14$, $C_{min} = 13\, \text{pF}$, $f_s = 100\, \text{MHz}$
- $T_s/\tau \gg 19.4$, or $10 \tau \ll T_s/2 \rightarrow R \ll 40 \, \Omega$
Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of $\phi_1$)
- Finite $R_{sw} \rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time

$R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection & clock feedthrough

Non-Linear Switch On-Resistance

Switch $\rightarrow$ MOS operating in triode mode:

$$I_{D(\text{triode})} = \frac{\mu C_m W}{L} (V_{GS} - V_{TH} - \frac{V_{DS}}{2}) V_{DS}.$$  

$$\frac{1}{R_{ON}} = \frac{dI_{\text{triode}}}{dV_{DS}} \bigg|_{V_{in} \rightarrow 0}$$

$$R_{GW} = \frac{1}{\mu C_m \frac{W}{L} (V_{GS} - V_{th})} = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{th} - V_{in})}$$

Let us call $R$ @ $V_{th} = 0$, then $R_w = \frac{1}{\mu C_m \frac{W}{L} (V_{DD} - V_{in})}$

$$R_{GW} = \frac{R_w}{V_{in}} \frac{V_{DD}}{V_{DD} - V_{th}}$$

$$V_{GS} = \frac{\phi_1}{V_{DD} - V_{in}}$$
Sampling Distortion

Simulated 10-Bit ADC & Sampling Switch modeled:

$$v_{out} = v_{in} \left( I - e^{-\frac{\tau}{2t}} \left( \frac{v_{in}}{V_{dd} - V_{th}} \right) \right)$$

$$T/2 = 5 \tau$$
$$V_{dd} - V_{th} = 2V$$
$$V_{FS} = 1V$$

→ Results in:
$$HD2 = -41 dBFS$$ &
$$HD3 = -51.4 dBFS$$

Sampling Distortion

Doubling sampling time (or ½ time constant)
Results in:

HD2 improved from -41dBFS to -70dBFS ~30dB

HD3 improved from -51.4dBFS to -76.3dBFS ~25dB

Allowing enough time for the sampling network settling → Reduces distortion due to switch R non-linear behavior to a tolerable level

10bit ADC
$$T/2 = 10 \tau$$
$$V_{dd} - V_{th} = 2V$$
$$V_{FS} = 1V$$
Sampling Distortion

Effect of Supply Voltage

- Effect of higher supply voltage on sampling distortion
  \[ \text{HD3 decreased by} \left( \frac{V_{DD1}}{V_{DD2}} \right)^2 \]
  \[ \text{HD2 decreased by} \left( \frac{V_{DD1}}{V_{DD2}} \right) \]

- 10bit ADC & \( T_s / 2 = 5 \tau \)
  \[ V_{DD} - V_{in} = 2V \] \[ V_{FS} = 1V \]

- 10bit ADC & \( T_s / 2 = 5 \tau \)
  \[ V_{DD} - V_{in} = 4V \] \[ V_{FS} = 1V \]

Sampling Distortion

- SFDR \( \rightarrow \) sensitive to sampling distortion - improve linearity by:
  - Larger \( V_{DD} / V_{FS} \)
  - Higher sampling bandwidth

- Solutions:
  - Overdesign\( \rightarrow \) Larger switches issue:
    \[ \rightarrow \text{Increased switch} \]
    \[ \rightarrow \text{Increased nonlinear} \]
    \[ \rightarrow \text{Junction cap.} \]
  - Maximize \( V_{PD} / V_{FS} \)
    \[ \rightarrow \text{Decreased dynamic range} \]
    \[ \rightarrow \text{if} V_{PD} \text{ const.} \]
  - Complementary switch
  - Constant & max. \(V_{GS} \neq f(V_{in})\)

- 10bit ADC \( T_s / \tau = 20 \)
  \[ V_{DD} - V_{in} = 2V \] \[ V_{FS} = 1V \]
Practical Sampling
Summary So Far!

- $kT/C$ noise
  
  $$C \geq 12k_B T \frac{2^{2B}}{V_{FS}^2}$$

- Finite $R_{sw}$ → limited bandwidth
  
  $$R \ll 0.72 \frac{Bf_C}{C}$$

- $g_{sw} = f(V_{in})$ → distortion
  
  $$g_{ON} = g_o \left(1 - \frac{V_{th}}{V_{DD} - V_{th}}\right) \text{ for } g_o = \mu C_{ox} \frac{W}{L} (V_{DD} - V_{th})$$

- Allowing long enough settling time → reduce distortion due to sw non-linear behavior

- Complementary n & p switch advantages:
  
  ✓ Increase in the overall conductance → lower time constant
  ✓ Linearize the switch conductance for the range $|V_{th}| < V_{in} < V_{DD} - |V_{th}|$
Complementary Switch Issues
Supply Voltage Evolution

- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly


Complementary Switch
Effect of Supply Voltage Scaling

- As supply voltage scales down input voltage range for constant $g_n$ shrinks
  $\rightarrow$ Complementary switch not effective when $V_{DD}$ becomes comparable to $2V_{th}$
Boosted & Constant $V_{GS}$ Sampling

- Gate voltage $V_{GS} =$ low
  - Device off
  - Beware of signal feedthrough due to parasitic capacitors
- Increase gate overdrive voltage as much as possible + keep $V_{GS}$ constant
  - Switch overdrive voltage independent of signal level
  - Error due to finite $R_{ON}$ linear (to 1st order)
  - Lower $R_{ON}$ → lower time constant

Constant $V_{GS}$ Sampling

- $V_{GS} =$ voltage @ the switch input terminal
Constant $V_{GS}$ Sampling Circuit

This Example: All device sizes: $W/L=10\mu/0.35\mu$
All capacitor size: 1pF (except for Chold)

Note: Each critical switch requires a separate clock booster


Clock Voltage Doubler

a) Start-up

b) Next clock phase
Clock Voltage Doubler

- Both C1 & C2 → charged to VDD after 1.5 clock cycle
- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

C1 & C2 Acquires charge

Both C1 & C2 charged to VDD after 1.5 clock cycle

Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

Clock period: 100ns

* R1 & R2 = 1GOhm
→ dummy resistors added for simulation only
Constant $V_{GS}$ Sampler: $\Phi$ Low

- Sampling switch M11 is OFF
- C3 charged to $\sim$VDD

Constant $V_{GS}$ Sampler: $\Phi$ High

- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant $V_{GS} = VDD$
- Mission accomplished!?
Constant $V_{GS}$ Sampling

Constant $V_{GS}$ Sampling?
Constant $V_{GS}$ Sampling?

- During the time period: $V_{in} < V_{out}$
  - $V_{GS} = \text{constant} = V_{DD}$
  - Larger $V_{GS} - V_{th}$ compared to no boost
  - $V_{GS} = \text{cte}$ and not a function of input voltage
  - Significant linearity improvement

- During the time period: $V_{in} > V_{out}$
  - $V_{GS} = V_{DD} - IR$
  - Larger $V_{GS} - V_{th}$ compared to no boost
  - $V_{GS}$ is a function of $IR$ and hence input voltage
  - Linearity improvement not as pronounced as for $V_{in} < V_{out}$

Boosted Clock Sampling
Complete Circuit

M7 & M13 for reliability

Remaining issues:
- $V_{GS}$ constant only for $V_{in} < V_{out}$
- Nonlinearity due to $V_{th}$ dependence of M11 on body-source voltage

Boosted Clock Sampling
Design Consideration

Choice of value for C3:

- C3 too large $\rightarrow$ large charging current $\rightarrow$ large dynamic power dissipation
- C3 too small
  $V_{\text{gate}} - V_{\text{s}} = \frac{V_{\text{DD}} \cdot C3}{C3 + Cx}$
  $\rightarrow$ Loss of $V_{\text{GS}}$ due to low ratio of $Cx/C3$
  Cx includes $C_{\text{GS}}$ of M11 plus all other parasitics caps….


Advanced Clock Boosting Technique


Two floating voltages sources generated and connected to Gate and S & D
Advanced Clock Boosting Technique

• clk → low
  – Capacitors C1a & C1b → charged to VDD
  – MS → off
  – Hold mode

Advanced Clock Boosting Technique

• clk → high
  – Top plate of C1a & C1b connected to gate of sampling switch
  – Bottom plate of C1a connected to $V_{IN}$
  – Bottom plate of C1b connected to $V_{OUT}$
  – $V_{GS}$ & $V_{GD}$ of MS both @ VDD & ac signal on G of MS → average of $V_{IN}$ & $V_{OUT}$
Advanced Clock Boosting Technique

- Gate tracks average of input and output, reduces effect of I-R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to $S$)
- Reported measured SFDR = 76.5dB at $f_{in}=200$MHz


Constant Conductance Switch

Constant Conductance Switch


M2 → Constant current
→ constant $g_{ds}$

M1 → replica of M2
& same VGS as M2
→ M1 also
constant $g_{ds}$

• Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC

• Also, opamp common-mode compliance for full input range required
Switch Off-Mode Feedthrough Cancellation

High-pass feedthrough paths past an open switch

Feedthrough cancellation with a dummy switch


Practical Sampling Issues

- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite $R_{sw}$ $\rightarrow$ limited bandwidth $\rightarrow$ finite acquisition time
- $R_{sw} = f(V_{in})$ $\rightarrow$ distortion
- Switch charge injection & clock feedthrough
Sampling Switch Charge Injection & Clock Feedthrough

Switching from Track to Hold

- First assume $V_i$ is a DC voltage
- When switch turns off $\Rightarrow$ offset voltage induced on $C_s$
- Why?

Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

- Channel $\Rightarrow$ distributed RC network formed between G,S, and D
- Channel to substrate junction capacitance $\Rightarrow$ distributed & voltage dependant
- Drain/Source junction capacitors to substrate $\Rightarrow$ voltage dependant
- Over-lap capacitance $C_{ov} = L_{ox}WxC_{ox}$ associated with G-S & G-D overlap
Switch Charge Injection
Slow Clock

- Slow clock $\rightarrow$ clock fall time $>>$ device speed
  $\rightarrow$ During the period $(t \rightarrow t_{off})$ current in channel discharges channel charge into low impedance signal source

- Only source of error $\rightarrow$ Clock feedthrough from $C_{ov}$ to $C_s$

Switch Clock Feedthrough
Slow Clock

$$
\Delta V = \frac{C_{ov}}{C_{ov} + C_s} (V_i + V_{ih} - V_L)
$$

$$
\approx \frac{C_{ov}}{C_s} (V_i + V_{ih} - V_L)
$$

$$
V_o = V_i + \Delta V
$$

$$
V_o = V_i (1 + \varepsilon) + V_{os}
$$

where $\varepsilon = \frac{C_{ov}}{C_i}$; $V_{os} = -\frac{C_{os}}{C_s} (V_{ih} - V_L)$
Switch Charge Injection & Clock Feedthrough
Slow Clock- Example

\[ C_{ov} = 0.1 \text{fF} / \mu \quad C_{ox} = 9 \text{fF} / \mu^2 \quad V_{th} = 0.4V \quad V_L = 0 \]
\[ \varepsilon = - \frac{C_{ov}}{C_{ox}} = - \frac{10 \mu \times 0.1 \text{fF} / \mu}{1 \text{pF}} = -1\% \]
Allowing \( \varepsilon = 1/2 \text{LSB} \rightarrow \text{ADC resolution} < \sim 9\text{bit} \)
\[ V_{os} = - \frac{C_{ov}}{C_s}(V_{th} - V_L) = -0.4 \text{mV} \]

Switch Charge Injection & Clock Feedthrough
Fast Clock

\[ Q_{ch} = \frac{1}{n+m} \]
\[ C_s = 1 \text{pF} \]

- Sudden gate voltage drop \( \rightarrow \) no gate voltage to establish current in channel
- Channel charge has no choice but to escape out towards S & D
Switch Charge Injection & Clock Feedthrough

Fast Clock

Clock Fall-Time \(<<\) Device Speed:

\[
\Delta V_o = -\frac{C_{ov}}{C_{ov} + C_s} (V_H - V_L) - \frac{1}{2} \times \frac{Q_{th}}{C_s}
\]

\[
\approx -\frac{C_{ov}}{C_{ov} + C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L}{C_s} \left( (V_H - V_i) - V_{th} \right)
\]

\[
V_o = V_i (1 + \varepsilon) + V_{os}
\]

where \(\varepsilon = \frac{1}{2} \times \frac{W C_{ox} L}{C_s} (V_H - V_{th})\)

\[
V_{os} = -\frac{C_{ox}}{C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{th})}{C_s}
\]

- For simplicity it is assumed channel charge divided equally between S & D
- Source of error \(\rightarrow\) channel charge transfer + clock feedthrough via \(C_{ov}\) to \(C_s\)

\[
\text{Example}
\]

\[
V_i V_G 10\mu/0.18\mu
\]

\[
M1 C_s=1\text{pF}
\]

\[
V_H V_L \quad t
\]

\[
V_o \quad \Delta V
\]

\[
t_{off}
\]

\[
C_{ov} = 0.1fF, \quad C_{ox} = 9fF, \quad V_{th} = 0.4V, \quad V_{DD} = 1.8V, \quad V_L = 0
\]

\[
\varepsilon = \frac{1}{2} \times \frac{10\mu x 0.18\mu x 9fF / \mu^2}{1pF} = 1.6\% \rightarrow \sim 5\text{-}bit
\]

\[
V_{os} = -\frac{C_{ox}}{C_s} (V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{th})}{C_s} = -1.8mV - 14.6mV = -16.4mV
\]
Switch Charge Injection & Clock Feedthrough

Example-Summary

Error function of:
→ Clock fall time
→ Input voltage level
→ Source impedance
→ Sampling capacitance size
→ Switch size

→ Clock fall/rise should be controlled not to be faster (sharper) than necessary

Switch Charge Injection

Error Reduction

• How do we reduce the error?
→ Reduce switch size to reduce channel charge?

\[ \Delta V_o = -\frac{I}{Q_{th}} \]

\[ \tau = R_{ON} C_i = \frac{C_i}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \]

(\text{note: } T_e = k \tau)

Consider the figure of merit (FOM):

\[ FOM = \frac{I}{\tau \times \Delta V_o} \times \frac{\mu C_{ox}}{C_i} \times 2 \times \frac{C_i}{WC_{ox} L \left((V_H - V_I - V_{th})\right)} \]

\[ \rightarrow FOM \propto \frac{\mu}{L^2} \]

☆ Reducing switch size increases \( \tau \) → increased distortion → not a viable solution
☆ Small \( \tau \) and small \( \Delta V \) → use minimum channel length (mandated by technology)
☆ For a given technology \( \tau \times \Delta V \) = constant
Sampling Switch Charge Injection & Clock Feedthrough

Summary

• Extra charge injected onto sampling capacitor @ switch device turn-off
  – Channel charge injection
  – Clock feedthrough to $C_s$ via $C_{ov}$

• Issues due to charge injection & clock feedthrough:
  – DC offset induced on hold $C$
  – Input dependant error voltage $\rightarrow$ distortion

• Solutions:
  – Slowing down clock edges as much as possible
  – Complementary switch?
  – Addition of dummy switches?
  – Bottom-plate sampling?