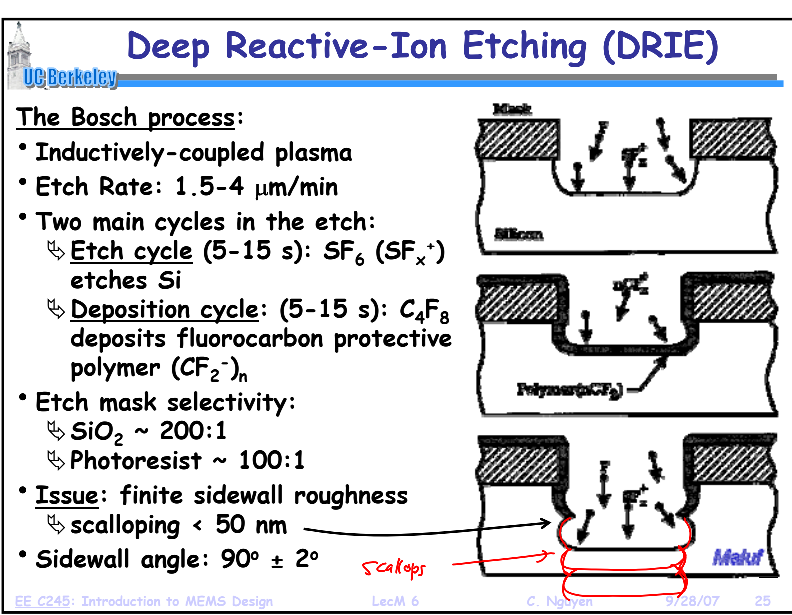

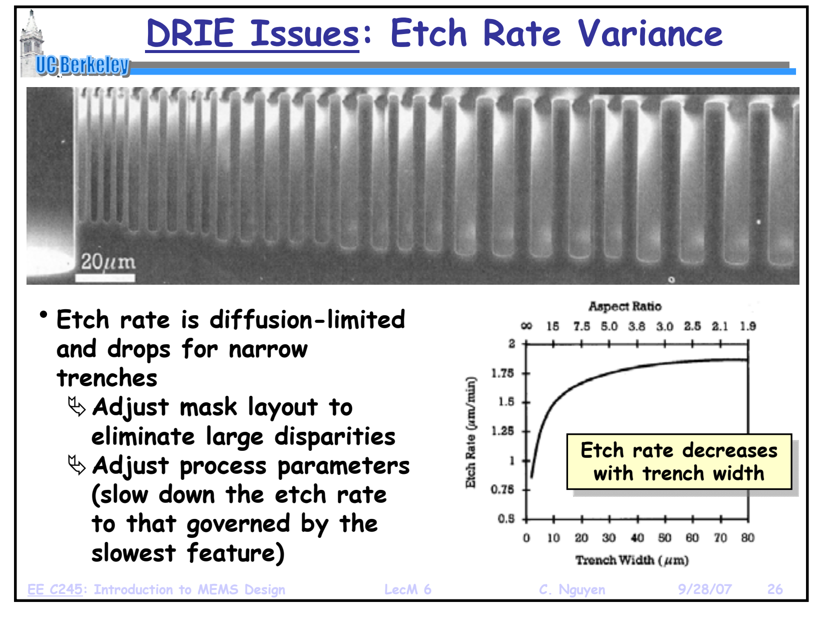

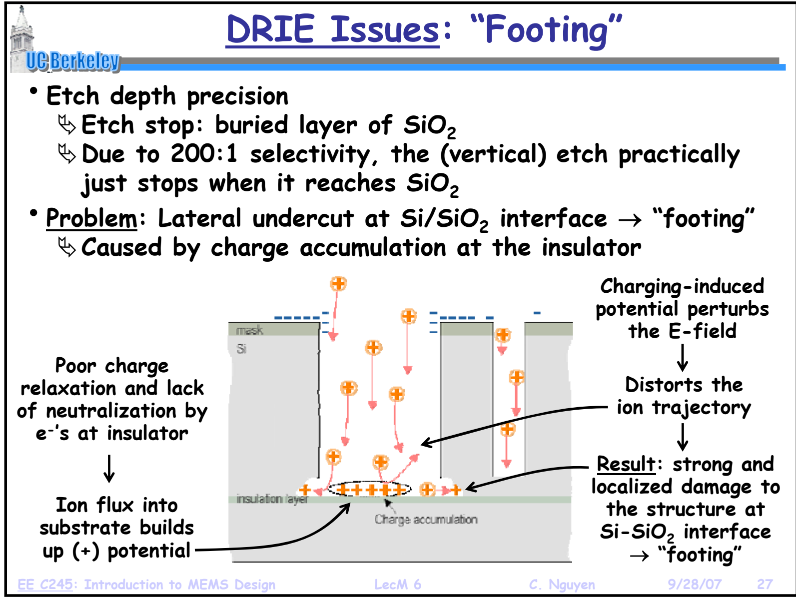

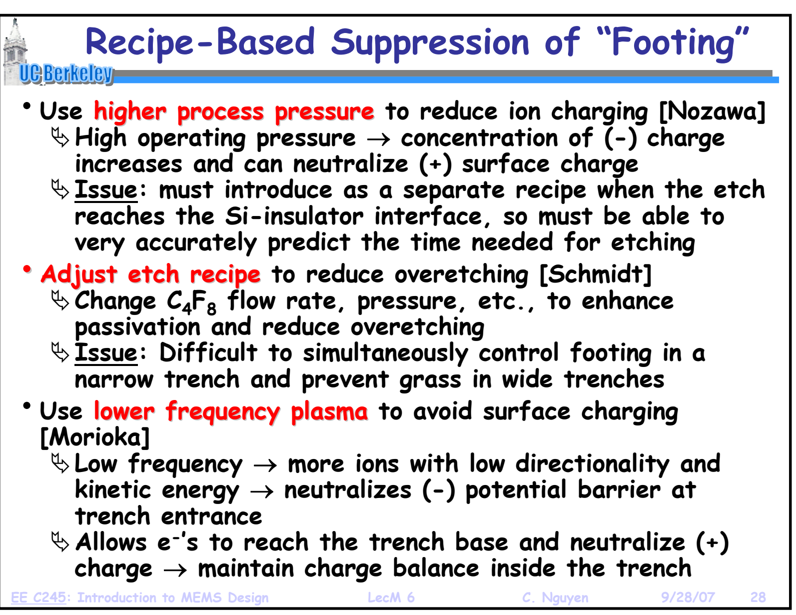

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Metal Interlayer to Prevent "Footing"

UC Berkeley

mask
Si
Metal interlayer (grounded to sub.)
Charge relaxation
Trench for metal definition
glass

Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial)
(b) Preparatory trenches
(c) Metal interlayer deposition
(d) Lift-off (remove PR)
(e) Anodic Bonding
(f) Silicon Thinning
(g) Photolithography 2
(h) DRIE
(i) Remove metal interlayer
(i) Metallize

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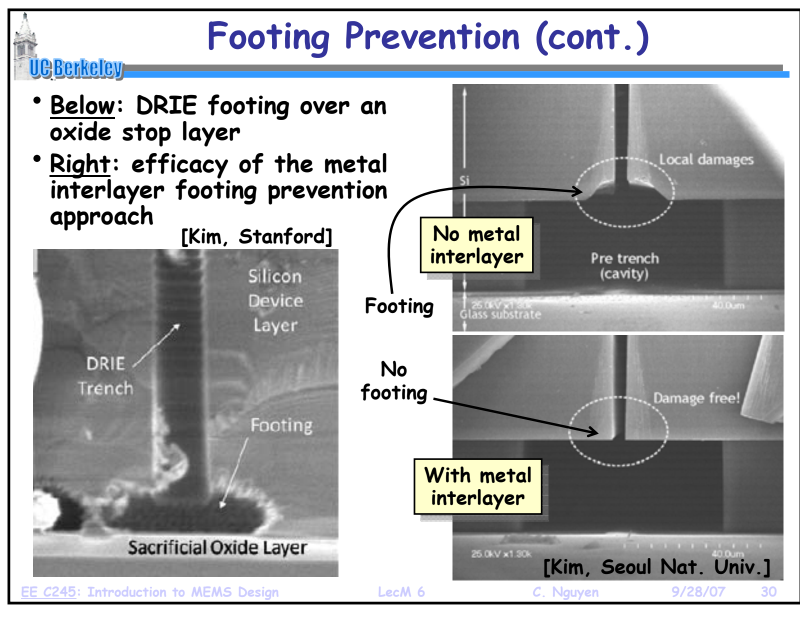

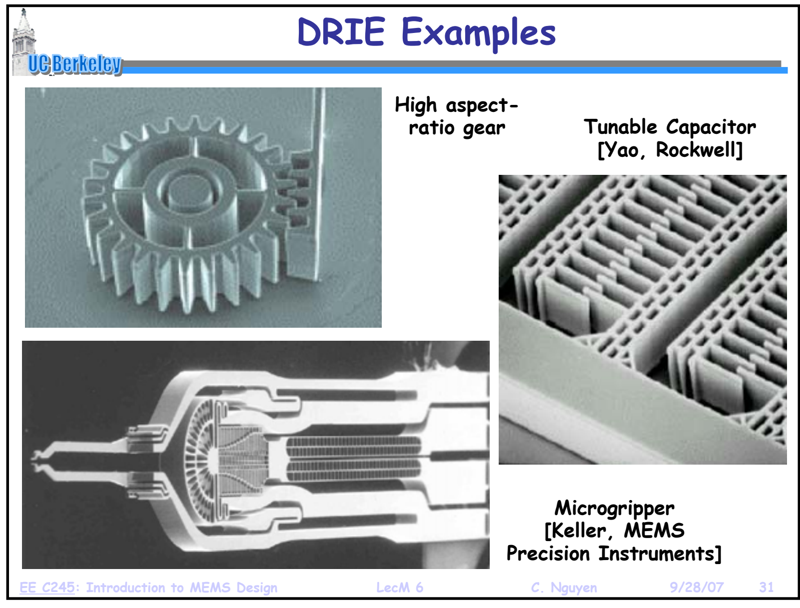

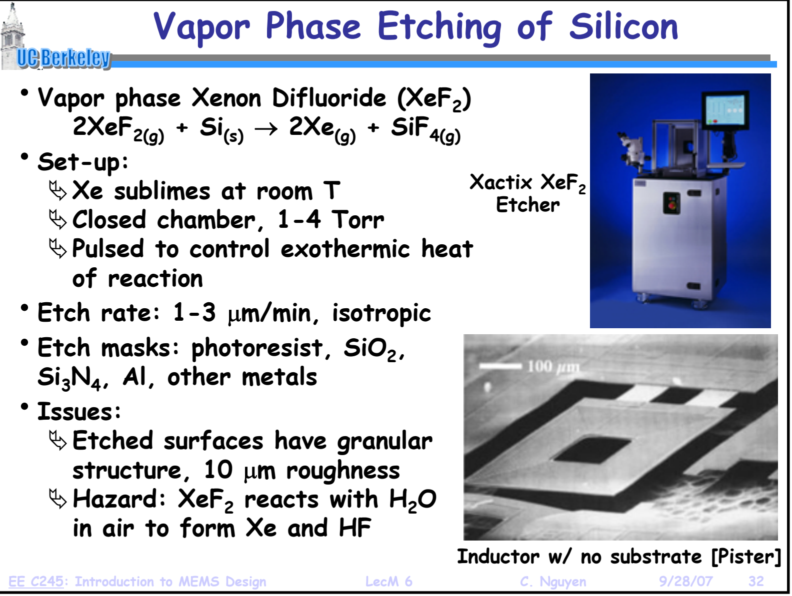

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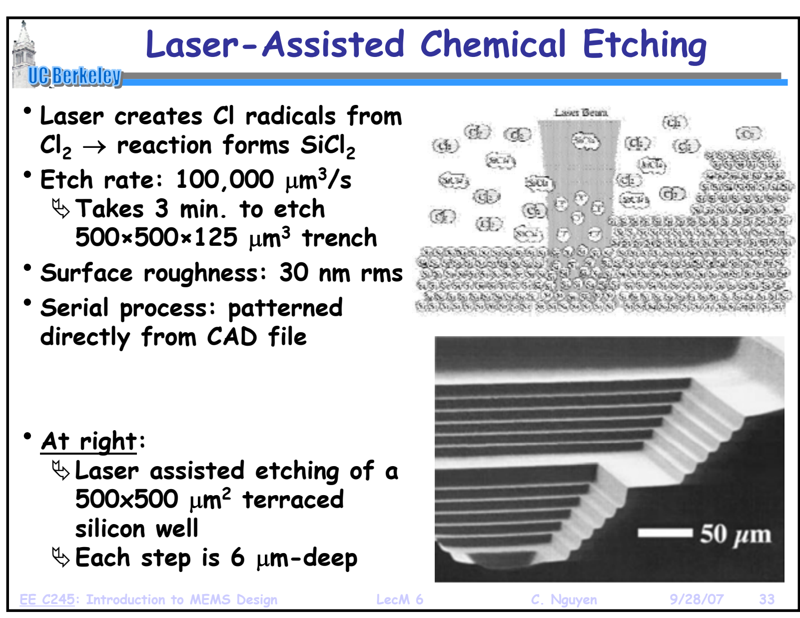

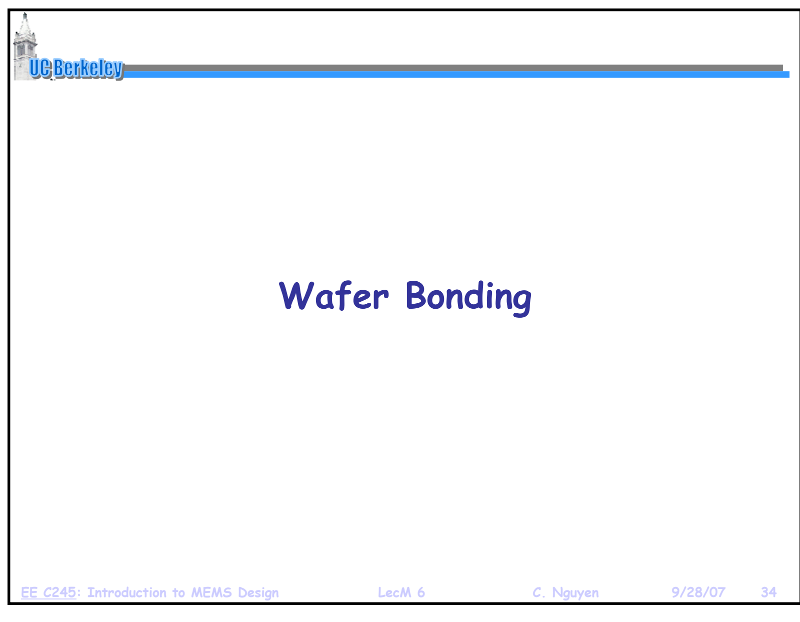

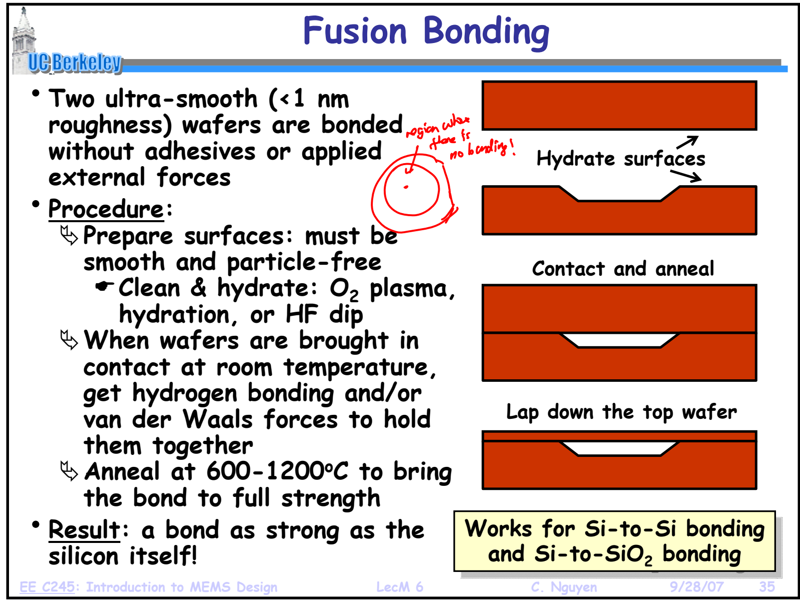

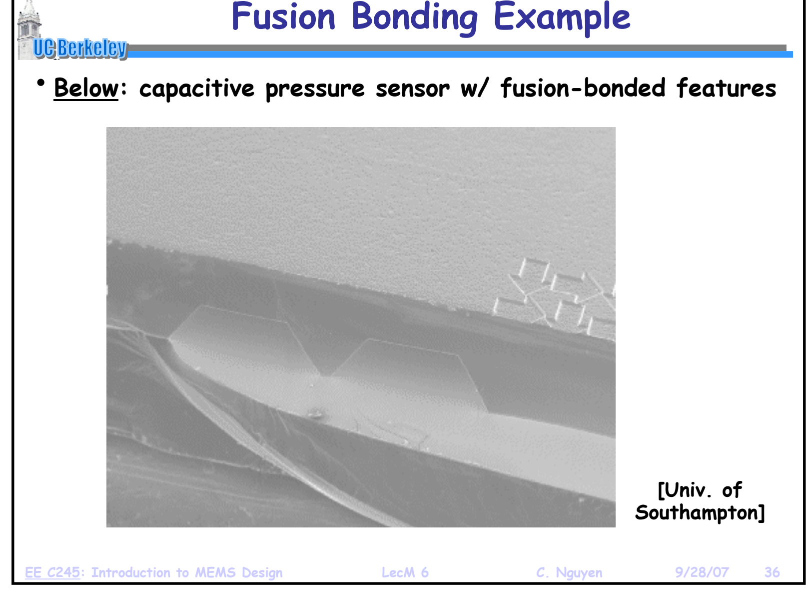

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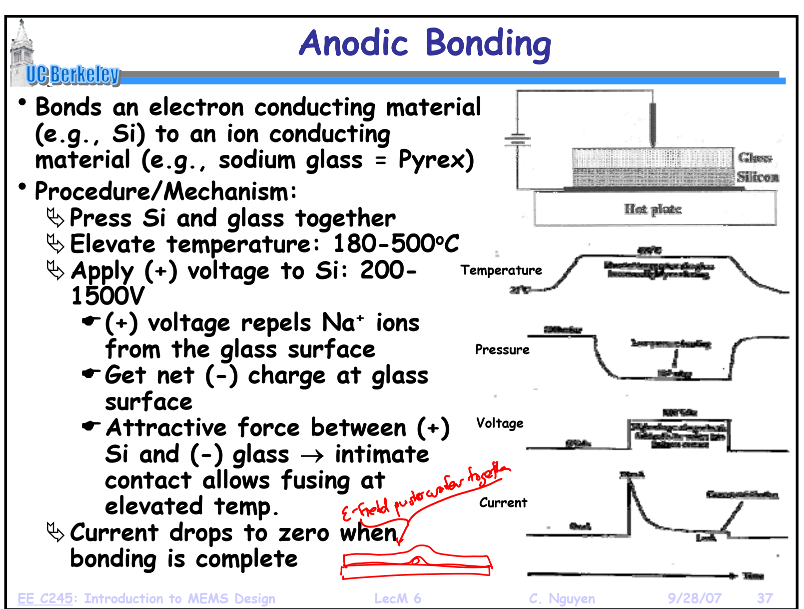
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Anodic Bonding
• Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
• Procedure/Mechanism:
Press Si and glass together
Elevate temperature: 180-500°C
Apply (+) voltage to Si: 200-1500V
(+) voltage repels Na+ ions from the glass surface
Get net (-) charge at glass surface
Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
Current drops to zero when bonding is complete
Glass
Silicon
Hot plate
Temperature
Pressure
Voltage
Current
Time
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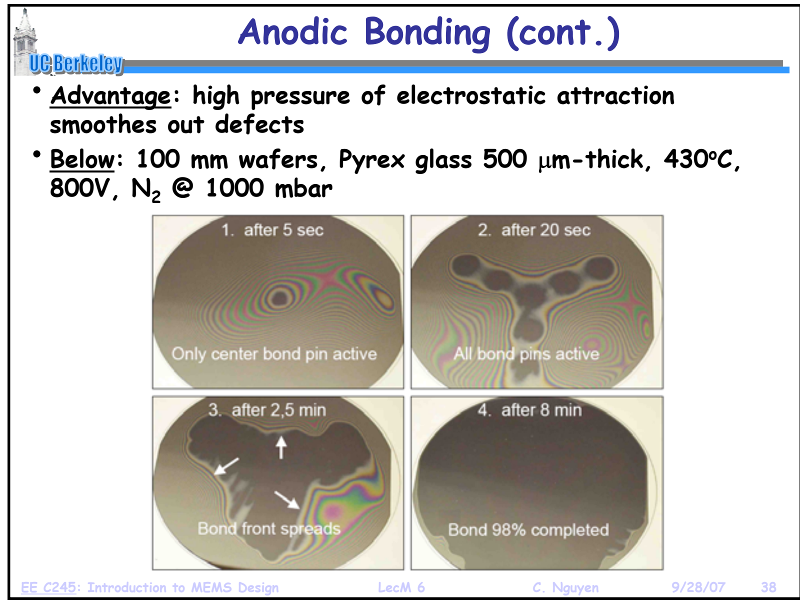
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Anodic Bonding (cont.)
• Advantage: high pressure of electrostatic attraction smoothes out defects
• Below: 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N2 @ 1000 mbar
1. after 5 sec
Only center bond pin active
2. after 20 sec
All bond pins active
3. after 2,5 min
Bond front spreads
4. after 8 min
Bond 98% completed
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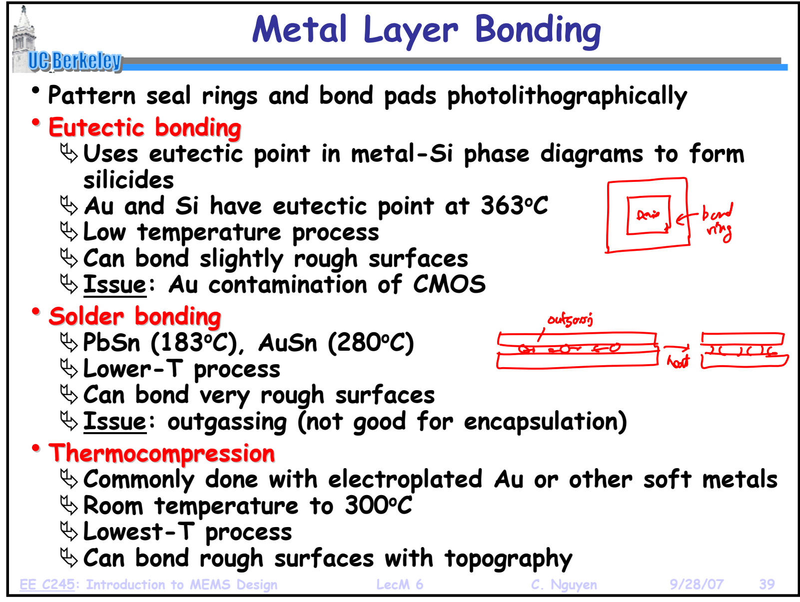
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Metal Layer Bonding
• Pattern seal rings and bond pads photolithographically
• Eutectic bonding
Uses eutectic point in metal-Si phase diagrams to form silicides
Au and Si have eutectic point at 363°C
Low temperature process
Can bond slightly rough surfaces
Issue: Au contamination of CMOS
• Solder bonding
PbSn (183°C), AuSn (280°C)
Lower-T process
Can bond very rough surfaces
Issue: outgassing (not good for encapsulation)
• Thermocompression
Commonly done with electroplated Au or other soft metals
Room temperature to 300°C
Lowest-T process
Can bond rough surfaces with topography
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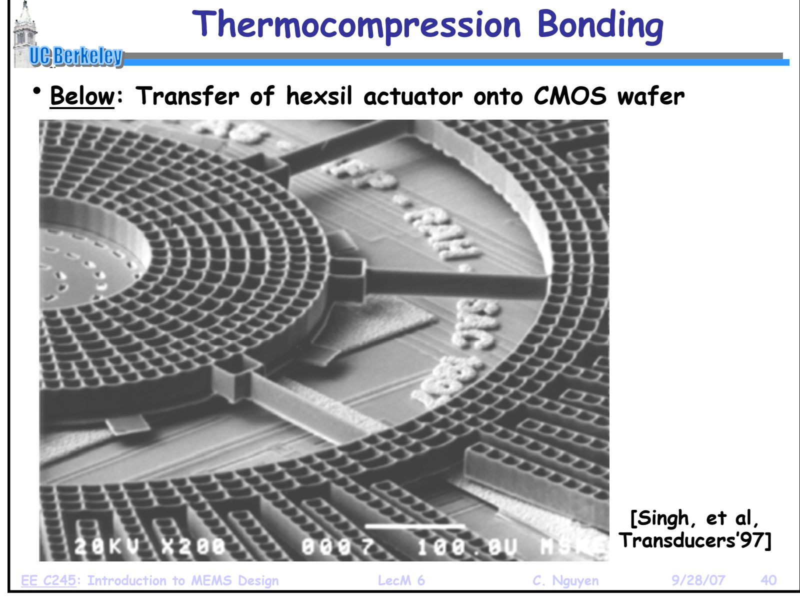
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Thermocompression Bonding
• Below: Transfer of hexsil actuator onto CMOS wafer
[Singh, et al, Transducers'97]
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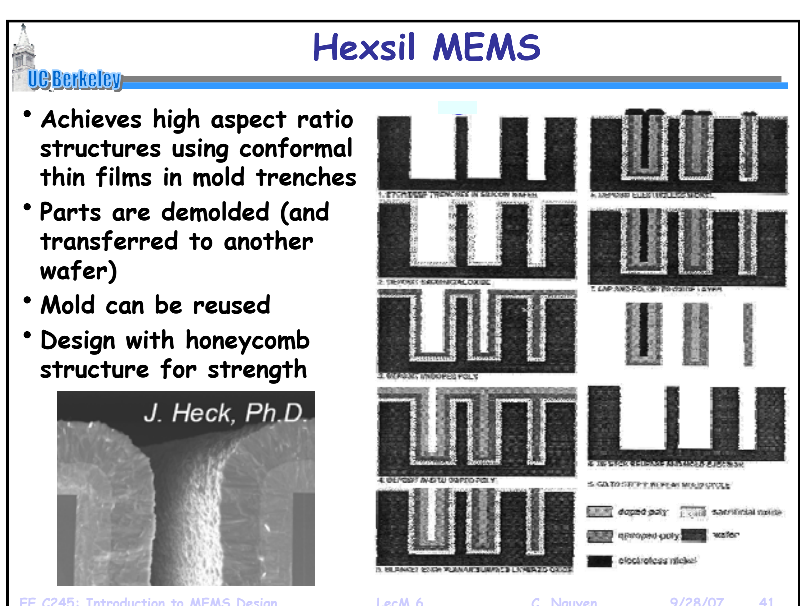

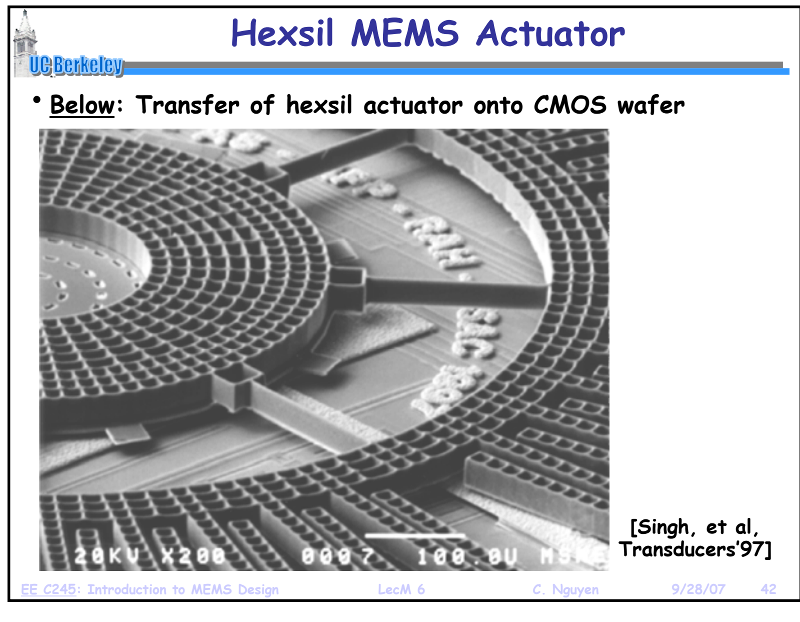

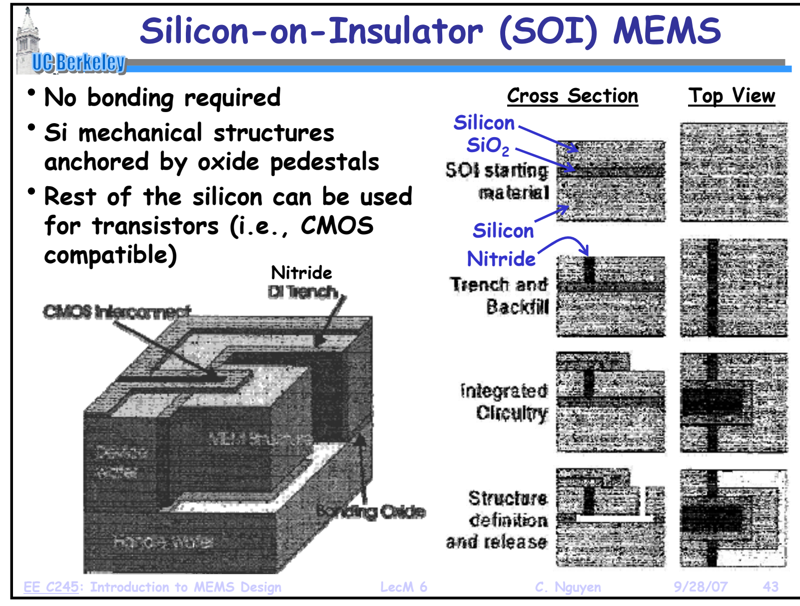

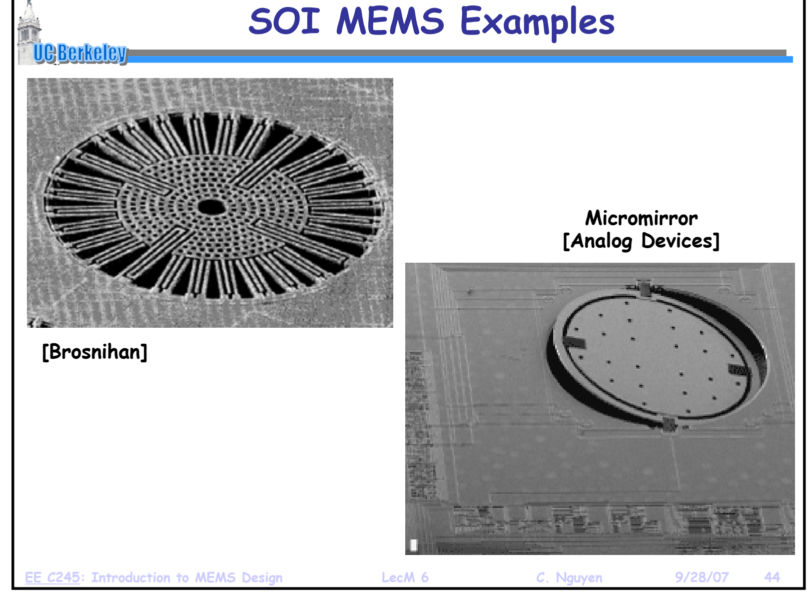

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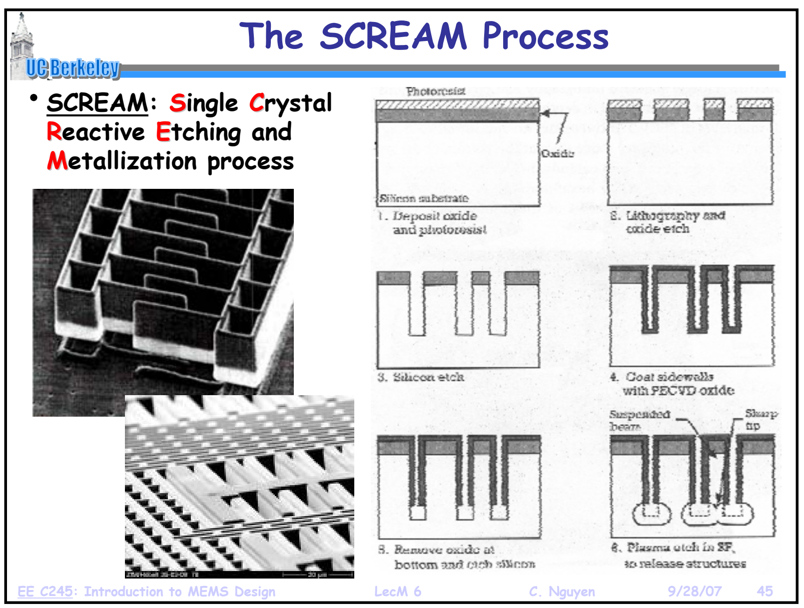

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