

Position-to-Voltage Conversion

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To sense position (i.e., displacement), use a capacitive load

Again, have port-to-port I/O symmetry:

Brute force approach:

$$\frac{N_o}{V_i}(s) = \frac{1}{R_x + \frac{1}{sC_x} + sL_x + \frac{1}{sC_D}}$$

$$\frac{N_o}{V_i}(s) = \frac{sC_x}{sR_xC_x + 1 + s^2L_xC_x + \frac{sC_x}{sC_D}} = \frac{C_x/C_D}{1 + C_x/C_D} \cdot \frac{1}{1 + \frac{sR_xC_x}{1 + C_x/C_D} + s^2 \frac{L_xC_x}{1 + C_x/C_D}}$$

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DC Gain Term

Low-Pass Biquad

$$\frac{N_o}{V_i}(s) = \frac{C_x/C_D}{1 + C_x/C_D} \frac{(\omega_0)^2}{s^2 + (\frac{\omega_0}{Q})s + (\omega_0)^2}$$

To maximize gain $\rightarrow 1$, need $C_D \ll C_x$. (must minimize C_D)

Note: Can we similar short-cut to the R case.

- Get DC response $\rightarrow C$'s dominate.
- Then:

$$\frac{N_o}{V_i}(s) = (\text{DC Gain}) \cdot \frac{1}{s} \cdot \text{LP}(s, \omega_0, Q) \cdot \omega_0^2 Q'$$

Voltage Representing Position

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Position Sensing Circuits

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Problems With Pure-C Position Sensing

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To sense position (i.e., displacement), use a capacitive load

Interconnect Bond Pad

$$\frac{N_o}{V_i}(s) = \frac{C_x/C_D}{1 + C_x/C_D} \cdot \frac{1}{s} \cdot \text{LP}(s, \omega_0, Q) \cdot \omega_0^2 Q'$$

Integration yields displacement.

To maximize gain, minimize C_D .

\Rightarrow Problem: parasitic capacitance

$$C_D \rightarrow C_D + C_{p_i} + C_{p_b}$$

\Rightarrow DC Gain: $\frac{C_x / (C_D + C_{p_i} + C_{p_b})}{1 + C_x / (C_D + C_{p_i} + C_{p_b})}$

Output will get smaller!

Remedy: Suppress C_p via use of op amps.

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The Op Amp Integrator Advantage

• The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p

$R_2 \gg \frac{1}{sC_2}$ (for biasing)

$R_0 = 0\Omega$

Can drive next stages R_i w/o interference to transfer function!

$N_0 = -i_o(R_2 \parallel \frac{1}{sC_2})$

$i_o \approx -\frac{N_i}{R_x} \frac{1}{sC_2}$

$\Rightarrow \frac{N_0}{N_s}(s) = -\frac{1}{R_x C_2 s}$

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Differential Position Sensing

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Differential Position Sensing

• Example: ADXL-50

Proof Mass

Sense Finger

Tethers with fixed ends

Applied Acceleration

Fixed Electrodes

Suspension Beam in Tension

capacitive divider

$C_1 \ll C_2$

$V_0 = -V_p + (2V_p) \frac{C_1}{C_1 + C_2}$

$= \frac{-V_p C_1 + 2V_p C_1}{C_1 + C_2} = V_p \frac{C_1 - C_2}{C_1 + C_2} = V_0$

Issue: Parasitic Capacitance!

$V_0 = \frac{C_1 - C_2}{C_1 + C_2 + C_p} V_p$

As before, C_p reduces gain!

Soln: use op amp!

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Buffer-Bootstrapped Position Sensing

Includes capacitance from interconnects, bond pads, and C_{gs} of the op amp

Unity Gain Buffer

C_{gd} = gate-to-drain capacitance of the input MOS transistor

Bootstrap the ground lines around the interconnect and bond pads

No voltage across C_p

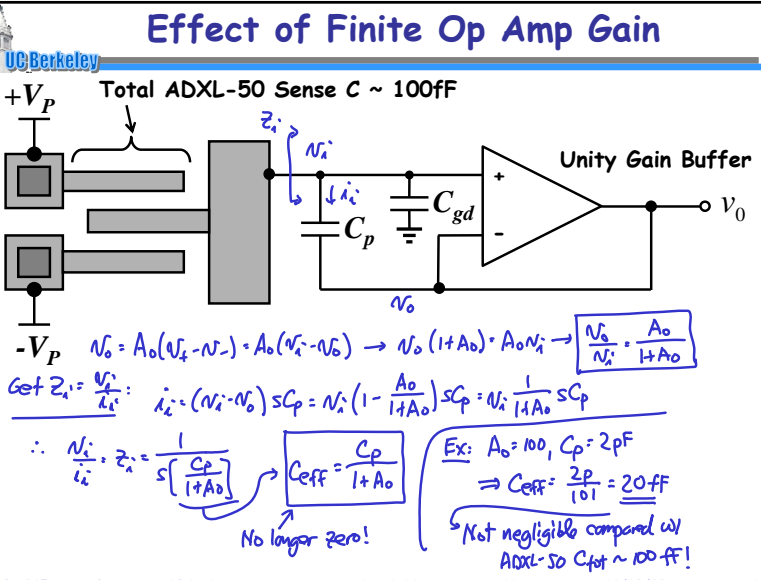
It's effectively not there!

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Effect of Finite Op Amp Gain

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Total ADXL-50 Sense $C \sim 100\text{fF}$



Unity Gain Buffer

V_0

$N_0 = A_0(N_i - N_-) = A_0(N_i - N_0) \rightarrow N_0(1 + A_0) = A_0 N_i \rightarrow \frac{N_0}{N_i} = \frac{A_0}{1 + A_0}$

Get $Z_i = \frac{V_0}{i_i}$: $i_i \cdot (N_i - N_0) sC_p = N_i \cdot \left(1 - \frac{A_0}{1 + A_0}\right) sC_p = N_i \cdot \frac{1}{1 + A_0} sC_p$

$\therefore \frac{N_0}{N_i} \cdot Z_i = \frac{1}{s} \left[\frac{C_p}{1 + A_0} \right] \rightarrow C_{\text{eff}} = \frac{C_p}{1 + A_0}$

No longer zero!

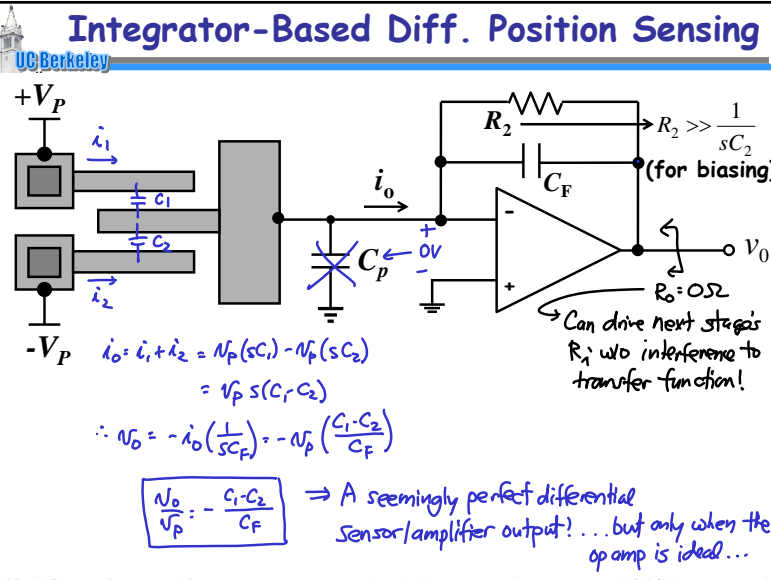
Ex: $A_0 = 100, C_p = 2\text{pF} \Rightarrow C_{\text{eff}} = \frac{2\text{pF}}{101} = 20\text{fF}$

Not negligible compared w/ ADXL-50 $C_{\text{tot}} \sim 100\text{fF}$!

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Integrator-Based Diff. Position Sensing

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$+V_P$

$-V_P$

i_0

V_0

$R_2 \gg \frac{1}{sC_2}$ (for biasing)

$R_0 = 0\Omega$

Can drive next stage's R_i w/o interference to transfer function!

$i_0 = i_1 + i_2 = N_p(sC_1) - N_p(sC_2) = N_p s(C_1 - C_2)$

$\therefore N_0 = -i_0 \left(\frac{1}{sC_F} \right) = -N_p \left(\frac{C_1 - C_2}{C_F} \right)$

$\frac{N_0}{V_P} = - \frac{C_1 - C_2}{C_F} \Rightarrow$ A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal ...

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