Surface Micromachining for Microelectromechanical Systems

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Invited Paper

Surface micromachining is characterized by the fabrication of micromechanical structures from deposited thin films. Originally employed for integrated circuits, films composed of materials such as low-pressure chemical-vapor-deposition polycrystalline silicon, silicon nitride, and silicon dioxides can be sequentially deposited and selectively removed to build or "machine" three-dimensional structures whose functionality typically requires that they be freed from the planar substrate. Although the process to accomplish this fabrication dates from the 1960's, its rapid extension over the past few years and its application to batch fabrication of micromechanisms and of monolithic microelectromechanical systems (MEMS) make a thorough review of surface micromachining appropriate at this time. Four central issues of consequence to the MEMS technologist are: i) the understanding and control of the material properties of microstructural films, such as polycrystalline silicon, ii) the release of the microstructure, for example, by wet etching silicon dioxide sacrificial films, followed by its drying and surface passivation, iii) the constraints defined by the combination of micromachining and integrated-circuit technologies when fabricating monolithic sensor devices, and iv) the methods, materials, and practices used when packaging the completed device. Last, recent developments of hinged structures for postrelease assembly, high-aspect-ratio fabrication of molded parts from deposited thin films, and the advent of deep anisotropic silicon etching hold promise to extend markedly the capabilities of surface-micromachining technologies.

Keywords*—*Integrated MEMS, MEMS, microelectromechanical systems, micropackaging, polysilicon micromachining, sacrificial release layer, stiction, surface micromachining.

I. Introduction

A. Historical Perspective

There has been activity in silicon-based micromachining since the early 1960's, when the integrated circuit (IC) technology was developed. During the 1960's–1970's, much of the research centered on anisotropic single-crystalline silicon etching. This technology demonstrated simple structures, with initial commercial products being pressure transducers. By the 1980's, improvements in thin-film deposition and increased understanding of the micromechanical properties of such films allowed thin-film microstructures to be formed by selective sacrificial etching. Some integration with metal–oxide–semiconductor (MOS) electronics was achieved during this period. Toward the latter half of the 1980's, researchers had demonstrated micromechanisms and electrostatic micromotors based on polycrystalline surface micromachining. Then, beginning in the 1990's, a significant influx of government research capital promoted the technological revolution that has brought us fully integrated complex microelectromechanical systems (MEMS) where sensors, actuators, and control functions are cofabricated in silicon using micromachining and IC processing.

Surface micromachining is based upon the process steps used repetitively to produce integrated circuits. It is therefore grounded in the use of photolithography to define patterns that are subsequently selectively subjected to chemical processing steps that either modify the properties of the silicon substrate or else define the geometries of overlying thin films deposited on the substrate. This sequence of steps was developed in the 1960's as the *planar process* to produce electronic IC devices. Because the devices are made in a batch process (e.g., many at a time) and interconnected as part of the fabrication sequence, they can be made very reliably and with precision even at very small dimensions (e.g., at present, feature sizes of 0.25–0.35 μm are possible in manufacturing). It is this capacity for miniaturization that has driven the industry to the point where today, technologists can realize multimillion-device integrated electronic chips no larger than 1–2 cm on a side.

The ability to make extraordinary, high-performance electronic systems using the IC process can be extended to engineering systems that require other than electronic

Manuscript received February 1, 1998; revised April 16, 1998. This work was supported by the Berkeley Sensor & Actuator Center, an NSF/Industry/University Cooperative Research Center.
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Publisher Item Identifier S 0018-9219(98)05087-7.

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devices as long as these other (usually mechanical) devices can be produced using steps like those developed for the planar process. Essentially, two basic methods have evolved for this purpose. One method builds the mechanical part by anisotropically etching or "machining" the bulk silicon substrate—it is therefore called *substrate* or *bulk micromachining*. A second technique, the subject of this paper, uses deposited films to make the mechanical parts extending above the surface of the silicon substrate; this technique is called *surface micromachining*.

To make a mechanical part from the deposited layer material, an underlying "sacrificial layer" is dissolved, thus "freeing" the element except where it is retained by an attachment to the silicon surface. This concept was demonstrated in the mid-1960's by Nathanson and coworkers at Westinghouse Research Laboratory using a patterned metal-film cantilever beam as a "resonant gate" for a field-effect transistor (FET) [1]. The use of sacrificial layers to form thin-film microstructures has come to be known as "surface micromachining."[1] This innovative early work at Westinghouse was decades ahead of its time in several respects. Integration of MOS electronics with polysilicon surface microstructures has recently become a commercial technology for accelerometers [2]. The motivating application for the resonant gate transistor was integrated frequency references and filters, which is now a major MEMS research topic [3], [4]. Furthermore, the potential of this metal surface-micromachining process to fabricate rotary bearings and micromotors was soon recognized. R. Newcomb and his group at Stanford University began to develop a process for a magnetically actuated micromotor [5] that anticipated features of early micromotors demonstrated nearly 20 years later [6]–[10].

In the early 1980's, researchers at the University of California (UC) Berkeley first fabricated polycrystalline silicon (polysilicon) microstructures using a silicon dioxide sacrificial layer [11]–[13]. This surface-micromachining technique was applied to make polysilicon microstructures [14], [15]. Unlike the resonant gate transistor work on metal structures, polysilicon surface micromachining was quickly recognized as a promising technology and employed at both academic and industrial laboratories. The reasons for the greater receptiveness to this "second introduction" of surface micromachining are many. The IC industry in the intervening two decades had made great strides and provided a mature infrastructure for surface micromachining. A community of researchers in silicon microstructures began building in the early 1980's and established internationally recognized symposia in the United States, Japan, and Europe. The successful commercialization of silicon microstructures for pressure sensing provided credibility that real-world sensing needs could be addressed by micromechanical structures. The successful operation of surface-micromachined polysilicon electrostatic micromotors [9], [10] stimulated government and industrial funding for research in silicon MEMS. That practical applications for rotary micromachines are only just now emerging [16] takes nothing away from the tremendous impact provided by their initial demonstration. Over the past several years, an ever increasing investment by Japan, the United States, and Europe has been made in micromechatronics, MEMS, and microsystems, respectively.

[1] "Surface micromachining" was suggested as a descriptive term by P. W. Barth, now of Hewlett-Packard Laboratories, in 1985.

Many now-used micromechanical fabrication processes and devices have evolved significantly from their primitive beginnings. For example, the salient features of what is now a major research thrust in microphotonics [17] have their foundation in research dating back to 1986. The development of pin joints and springs by Fan and Tai [18], followed by actuation by electrostatic forces [9], [19], the demonstration of comb-drive actuators [20] and of microvibromotors [21], and finally the innovative "foldout" of surface structures by Pister [22] all helped to build today's technology. These ideas combine to make it possible to build a three-dimensional (3-D) structure that can deploy into the path of an optical beam to interface with conventional fiber-optical hardware for the purpose of coupling alignment, switching, and scanning.

Technologies that merge different surface-micromachining processes with various electronic processes have been demonstrated in academia [13], [23], [24] and industry [2], [25]–[28]. Although these monolithic MEMS require complex fabrication processes, there are major incentives to integrating electronics and surface microstructures [29].

B. Overview

This paper identifies the key process steps of surface micromachining [24], [30] and provides an introduction to the literature describing the technology. Polysilicon is the primary microstructural material considered in this paper, although other materials are mentioned. The control of the mechanical properties of polysilicon has been studied extensively and is relatively well understood.

Other techniques involving the use of thin-film structural materials released by the removal of an underlying sacrificial layer have helped to extend conventional planar surface micromachining into the third dimension. By connecting polysilicon plates to the substrate and to each other with hinges, elaborate 3-D micromechanical structures can be assembled after release. Recently, another approach to 3-D microstructures has been demonstrated that uses the conformal deposition of polysilicon and sacrificial oxide films to fill deep trenches previously etched in the silicon substrate in a process called HexSil [31]. After release of the polysilicon structure from the substrate "mold," the latter can be used again. Structures having much larger dimensions, with thicknesses greater than 100 μm and lateral dimensions of more than 1 cm, are feasible using the HexSil molding technique. Wafer-to-wafer microstructural transfer processes have begun to show promise by pointing the way to batch-assembled 3-D fabrication.

Processes not related to straightforward surface micromachining, such as dry-release processes for tunneling-tip microinstruments [32], high-aspect-ratio silicon-on-

insulator inertial integrated sensor technology [33], buried-cavity dry-release technology [34], and various approaches to postprocessing of unmodified complementary MOS (CMOS) wafers [35], [36], or the dissolved-wafer process [37], do not lie within the necessarily limited scope of this review.

The MEMS community has long deliberated the pros and cons of a fully integrated technology (monolithic electronics and mechanical components) as compared to one having discrete electronics and sensor chips (the "two-chip" approach). Tradeoffs between front-end technology complexity to enhance device performance by minimizing parasitic capacitances and dual-chip packaging costs are not yet settled. The fundamental questions boil down to the signal-to-noise requirements and the cost of manufacture. A major decision facing the integrated MEMS technologist is when and how to integrate the electronics and micromechanical fabrication steps. Three perspectives will be illustrated: 1) post-CMOS implementation over the finished IC wafer, 2) interleaved CMOS/microstructure fabrication, and 3) pre-CMOS microstructure fabrication inside a planarized well. These examples all illustrate a monolithic process architecture approach.

Some problem areas for polysilicon as a MEMS material include residual stress, stress gradients through the film thickness, and statistical variations of the effective Young's modulus in this multicrystalline material. All can affect the mechanical behavior of polysilicon microstructures. The relatively coarse dimensional control possible with surface microstructures makes postfabrication adjustments necessary to control the frequency values of MEMS resonators, even if material properties are precisely known. Release of microstructures by selective etching is critical, often leading to problems with stiction—the sticking of structures to the substrate after rinsing and drying. Several "work-arounds" to this problem have been developed, any one of which can achieve high yields of free-standing microstructures. Stiction due to contact with adjacent surfaces after release remains a fundamental reliability question for surface-micromachined structures. Present strategies for alleviating postrelease stiction are outlined.

Last, an overview of die- and wafer-level packaging identifies an under-researched but increasingly important aspect of the surface-micromachined sensor technology. As the MEMS industry matures, packaging is becoming the dominant cost of products such as microaccelerometer and microgyroscope devices [38]. Inexpensive yet hermetic packaging schemes that are compatible with the fragile released mechanical components are not currently available. Wafer- and chip-level processing for MEMS involves more complications than are encountered in conventional IC's. Extreme care needs to be exercised with pick-and-place tooling and environmental conditions (e.g., humidity and particle contamination) as "freed" mechanical elements may be exposed to the environment. Several original equipment manufacturers have dedicated fabrication equipment designed to address some of these issues; however, more work needs to be done from both the technology and equipment support side to bring the next-generation packaging concepts to fruition. In the meantime, researchers have addressed this issue by using low-stress thin-film encapsulants [39], permeable thin films [40], molded and transferred polycrystalline capping structures [41], and dissolved wafer capping techniques [37], as well as conventional glass-silicon anodic bonding techniques [42], at times employing nonevaporable getter materials within the device cavity [43].

II. Surface Micromachining

A. Polysilicon and Silicon Dioxide

The review paper by Petersen in 1982 [44] led to widespread acceptance of micromachined silicon as a structural material. The basic mechanical properties of single-crystal silicon were collectively assembled in the paper, which also provided a number of examples of structures to illustrate the potential for MEMS. As has been described in the first section of this paper, in 1982, the first steps were being taken to establish thin-film polycrystalline silicon as a mechanical material [11]. Silicon in polycrystalline thin-film form has properties (e.g., Young's modulus, fracture strength, etc.) that typically differ from single-crystal values as a consequence of deposition variations, grain-size effects, and possibly other sources. Therefore, mechanical characterization can be significantly more challenging. Etch, oxidation, and other processing properties of polysilicon are likewise generally more varied and process dependent than are these properties in single-crystal material owing to aggregate variations in crystallite orientations.

The special value of polycrystalline silicon films for mechanical applications in surface micromachining, in particular its fairly straightforward incorporation into IC-derived processing, needs therefore to be balanced against the complications in characterizing it as described above. The IC industry has, however, thrived despite similar needs to characterize process-dependent materials; in fact, significant widespread efforts have gone into establishing polysilicon as an electrical design material [45]. Similar data are being assembled for the mechanical properties of polysilicon;[2] a great deal is already known, and significant practical commercial design has occurred. We can expect a continuing growth in applications of polysilicon as a mechanical material.

The early MEMS applications established single-crystal silicon as a robust mechanical material; its Young's modulus is directionally dependent and near that of stainless steel, and it has a Knoop hardness twice that of iron and very high tensile strength. Single-crystal silicon is nevertheless brittle and fractures without yielding [44]. Thin-film polycrystalline silicon maintains some of these attributes, with some exceptions. Lower comparative values for Young's modulus and inelastic deformation have been regularly observed. Polycrystalline silicon has shown a tighter spread in fracture-stress distribution than single-crystal silicon, where

[2] See http://www-bsac.eecs.berkeley.edu/polysilicon.html.

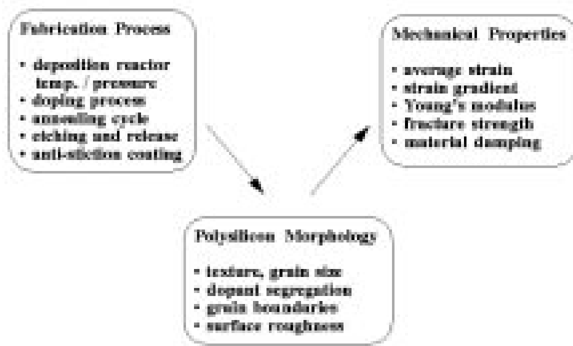


Fig. 1. Microstructural polysilicon mechanical property dependency on film morphology and fabrication process parameters.

fracture characteristics are determined by geometrical flaws such as microdefects [46], [47]. Polycrystalline silicon may not be as sensitive to these microgeometrical irregularities. As a result, industrially prepared polycrystalline silicon may prove to be more controllable than single-crystal material, and it has already demonstrated low coefficients of variation in a manufacturing environment [48] (e.g., 48 tests on five different sets of fabricated specimens yielded approximate values: Young's modulus $= 170 \pm 6$ GPa, Poisson's ratio $= 0.22 \pm 0.01$, and tensile strength $= 1.2 \pm 0.15$ GPa).

For mechanical use, polycrystalline silicon is typically deposited using gas-phase decomposition of silane in a low-pressure chemical-vapor-deposition (LPCVD) furnace at temperatures ranging 585–625°C. Phosphine or diborane can be added to the gas stream to form *in situ* doped films. Prior to its use as a micromechanical material, polysilicon was used for many years as the gate electrode material in MOSFET devices. This very important commercial application has led to an extensive infrastructure and knowledge base detailing its electrical properties as functions of deposition conditions and postdeposition treatments. Additionally, a very complete understanding of deposition parameters exists. The advent of the use of polysilicon as a mechanical material in the 1980's led to significant R&D and manufacturing implementation to characterize it mechanically at laboratories and companies around the world. While the MEMS technologist is primarily interested in material properties such as average strain, strain gradient, Young's modulus, fracture strength, and material damping, he must keep in mind that these parameters are functions of the film morphology, which is, in turn, dependent upon specifics of deposition and/or fabrication processing. Fig. 1 schematically illustrates these interdependencies.

To illustrate the fabrication process for a micromechanical polysilicon device, we consider the surface-micromachining steps used to produce a polysilicon lateral resonator [49], [50]. This basic process sequence is divided into four modules:

1) Substrate Passivation and Interconnect: After a blanket n^+ diffusion, to define the substrate ground plane, a silicon wafer is passivated with a layer of 0.15 μm LPCVD silicon nitride deposited over a layer of 0.5-μm-thick thermal SiO_2. Contact windows to the substrate ground plane are then opened to yield the cross section shown in Fig. 2(a). Deposition, definition, and patterning of an *in situ* phosphorus-doped polysilicon interconnection layer follows Fig. 2(b) to form a second electrode plane and an interconnection to the n^+ diffusion and the microstructure to be built above.

2) Sacrificial Layer Deposition and Patterning: A 2-μm-thick LPCVD sacrificial phosphosilicate glass (PSG) layer is deposited and patterned in two separate masking steps. The first is a timed etch to create "dimples" (mechanical standoffs), as shown in Fig. 2(c). The second masking step etches through the PSG layer in windows, which allow the formation of the anchors of the polysilicon structure, as shown in Fig. 2(d).

3) Structural Polysilicon Deposition, Doping, and Stress Anneal: The 2-μm-thick polysilicon structural layer is then deposited by LPCVD (undoped) at 610°C in Fig. 2(e). This layer is doped by depositing a 0.3-μm-thick PSG film [Fig. 2(f)] and then annealing at 1050°C in N_2 for one hour. This step causes the polysilicon to be doped symmetrically by simultaneous diffusions from both the top and the bottom PSG layers in order to achieve a uniform grain texture and avoid gradients in residual strain. If a strain gradient is present, it generates bending in the microstructure upon release. The top PSG layer is then stripped, and the structural polysilicon is then patterned by reactive-ion etching (RIE) in order to achieve the nearly vertical sidewalls illustrated in Fig. 2(g). An alternative is to implement an *in situ* phosphorus-doped polysilicon layer [23] or an ion-implanted and annealed film [25] to achieve a more conductive film.

4) Microstructure Release, Rinse, and Dry: In the last steps, the wafer is immersed in aqueous hydrofluoric acid (typically 10 : 1 diluted hydrofluoric acid (HF) or buffered HF) to dissolve the sacrificial PSG layer. The wafer is rinsed in deionized water and dried under an infrared lamp, or rinsed in deionized water, and then dried in a way to avoid its collapse and adhesion to the substrate—a phenomenon known as "stiction." The final cross section is shown in Fig. 2(h).

By repeating these basic sacrificial oxide and structural polysilicon fabrication steps while including provisions for anchor points and other structural features, one can build extremely complex structures. Examples of these are the Sandia National Laboratories five-level Sandia Ultra-Planar Multi-Level MEMS Technology (SUMMiT) [51], [52] and the Microelectronics Center of North Carolina (MCNC) Three-Level Multi-User MEMS Process (MUMPS).[3] MCNC offers the MUMPS program for a domestic prototyping and proof-of-concept foundry service. The five-level Sandia SUMMiT process (14 masks, 240 process steps) is the most complex polysilicon surface-micromachining technology reported to date. A distinguishing feature is the use of chemical-mechanical polishing

[3] See http://mems.mcnc.org/.

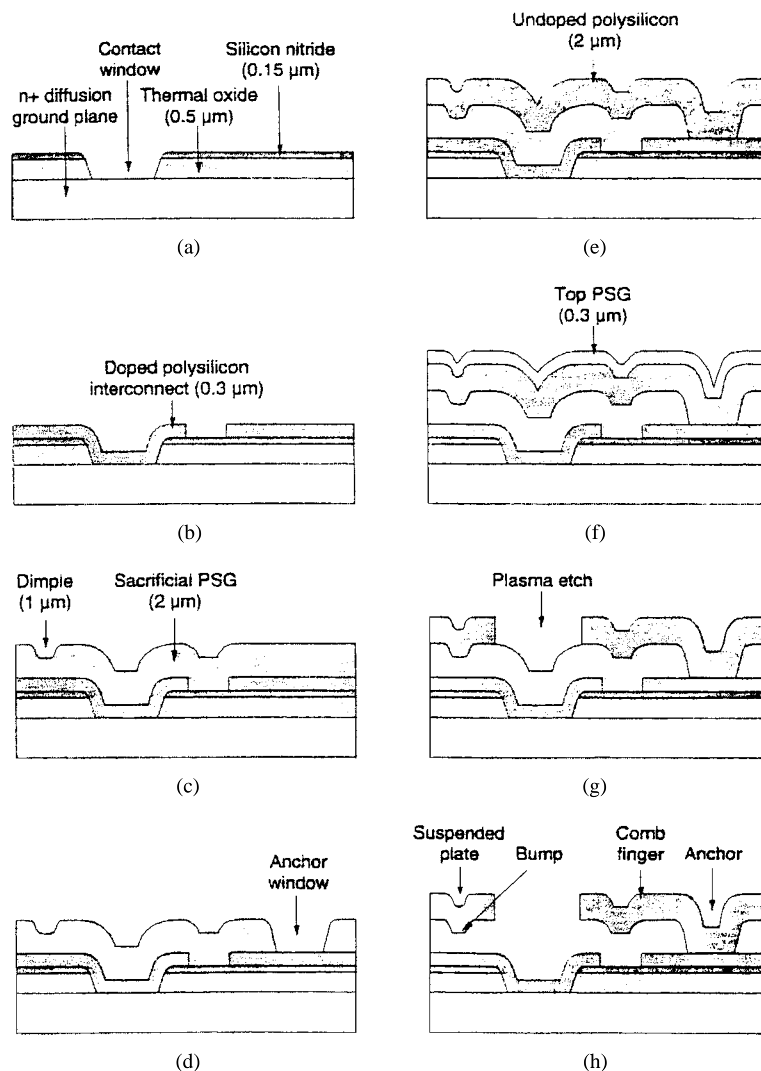


Fig. 2. Polysilicon surface-micromachining process sequence [49].

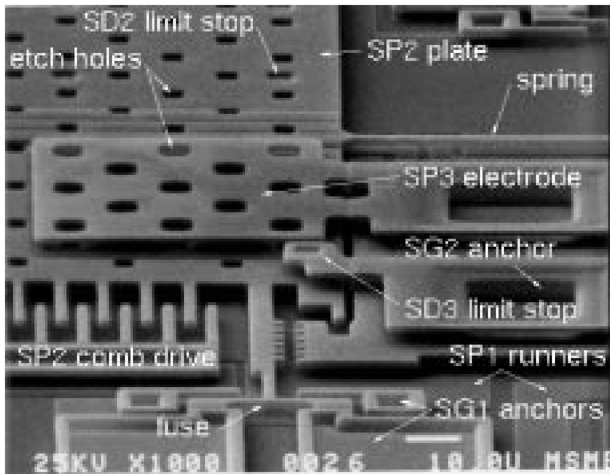
(CMP). Fig. 3 illustrates the detail and complexity made possible by these added technologies. Fig. 3(a) is a cross-sectional scanning-electron micrograph (SEM) of the five-level polysilicon architecture, formed by focused ion-beam milling through all the structural layers. Fig. 3(b) is an overhead SEM view of the salient structural features typical in UC Berkeley's three-level process. In this example, the freed plate is tethered in place with a meander spring incorporating fusible links. Not visible in Fig. 3(b) is monolithically integrated CMOS circuitry that was fabricated before the microstructures.

B. Fully Integrated Monolithic MEMS

Among the advantages of fully integrated MEMS that merge microstructures and microelectronics on a single substrate are reduced size and electronic noise. Size, system-power requirements, and noise sources can all be minimized. Final packaging and assembly can typically be simplified and conventional IC manufacturing yield-enhancement and cost-reduction techniques more readily implemented. With MEMS, an analogy can be made to microprocessor chips, which, when they were first produced, received criticism because of the compromises they demanded in fabrication technologies in order to combine former separately optimized special-purpose chip-fabrication techniques. The compromises that were made for microprocessor fabrication are now enormously justified by the phenomenal success of microprocessor chips. We can expect a similar scenario for MEMS. At the present time, however, there are often significant challenges to success with monolithic processing. These challenges include materials and process incompatibilities and the greater cost of special-purpose electronic processes compared with conventional digital CMOS. A hybrid approach with separate MEMS and electronic chips remains a competitive approach. Hybrid packaging of MEMS has been demonstrated using multichip modules [53] and flip-chip techniques.[3]

A number of examples of monolithically integrated MEMS have been described [23], [25], [54]. To achieve a monolithic MEMS technology, the designer can choose to place the sequence of processing steps for the mechanical structures as a block before, after, or intermediately

(a)



(b)

Fig. 3. (a) SEM cross-sectional image of the Sandia five-level process [52]. (b) SEM overhead image of the UC Berkeley three-level post-CMOS monolithically integrated process. CMOS circuitry not visible [23].

in the electrical-fabrication steps. If one has complete control over the production steps, these steps can even be interleaved within the overall process. When several layers of polysilicon are needed for the mechanical structures, problems in maintaining surface planarity make CMP a necessity [55].

If the circuits are processed before the mechanical parts, the circuit areas must be fully passivated to make them impervious to the release acid. One embodiment of this postcircuit structure fabrication concept is conceptually illustrated in Fig. 4, a cross section of the CMOS transistors and microstructure. This MEMS architecture would allow the sensor element to be fabricated directly on top of the circuit area, thereby minimizing the needed chip area [23]. The double-polysilicon, single-metal, N-well CMOS technology is fabricated as a baseline module. Transistor source, drain, and gate contacts require titanium silicide and titanium nitride barrier metallurgy. Buried circuit interconnects employ a tungsten refractory metallization making possible high-temperature postprocessing. CMOS passivation is done using densified LPCVD phosphosilicate glass and low-stress silicon-rich nitride. Circuit-to-structure interconnection is realized via the doped ground-plane polysilicon (SP1 layer) through the SNT contact shown. Microstructural fabrication then proceeds as previously described. Complexities associated with the high-temperature compatibility of the buried metallurgy make this technologically difficult. Recent manufacturing attempts using this buried metal post-CMOS MEMS technology have highlighted some of the difficulties associated with exposing interconnect metallization to elevated microstructural fabrication temperatures. These difficulties centered mainly around high metal-to-semiconductor contact resistance (particularly contacts to p-type silicon) and observed metal delamination [56].

Interleaving structural micromechanical and integrated circuit technologies is feasible, was demonstrated with n-channel MOS in 1984 [57], [58], and is currently being used in the Analog Devices BiMEMS technology to fabricate commercial integrated inertial devices for automobile applications [25]. As shown in Fig. 5, BiMEMS uses diffused n^+ runners as interconnections between the sensor and the circuitry. In contrast, other technologies use a "ground-plane" polysilicon layer for this purpose.

The insight that interference with the subsequent CMOS process could be nearly eliminated by burying the polysilicon and oxide layers in a sealed trench is the foundation of the Sandia Micromechanics Microsensors and CMOS technology (MM/CMOS) [54], which was used to fabricate a three-axis integrated accelerometer on a chip [59]. The MM/CMOS technology, illustrated in Fig. 6, can be summarized as follows:

i) a trench is etched into the bulk silicon using an anisotropic aqueous etchant;
ii) the double (or triple) polysilicon MEMS structure is defined in the trench;
iii) the trench is refilled with LPCVD oxide, planarized with CMP, and passivated with LPCVD nitride;
iv) standard CMOS fabrication is executed in areas adjacent to the MEMS area;
v) the CMOS is passivated, the trench area is reopened, and microstructures are released.

Circuit-to-structure electrical connection is achieved through the poly stud contact to the ground-plane polysilicon (MM Poly 0).

It is also worth noting that both the pre- and the post-CMOS methods enable modular, sequential foundry fabrication for the CMOS and the MEMS. This modularity is a distinct advantage in developing an integrated MEMS technology; however, careful attention is still needed to avoid process incompatibilities. Production of MEMS using conventional CMOS production has been demonstrated [60], but at this writing, the only high-volume commercial

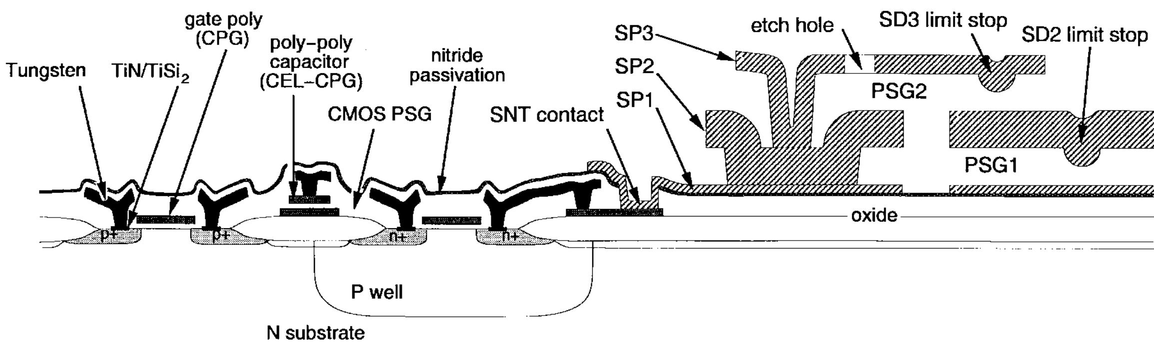


Fig. 4. Cross-sectional illustration of the UC Berkeley Modular Integration of CMOS and Micro-Structures technology. Post-IC MEMS fabrication requires using tungsten interconnect metallization. Electrical connections to the mechanical structure rely on poly-to-poly contacts at the SNT region [23].

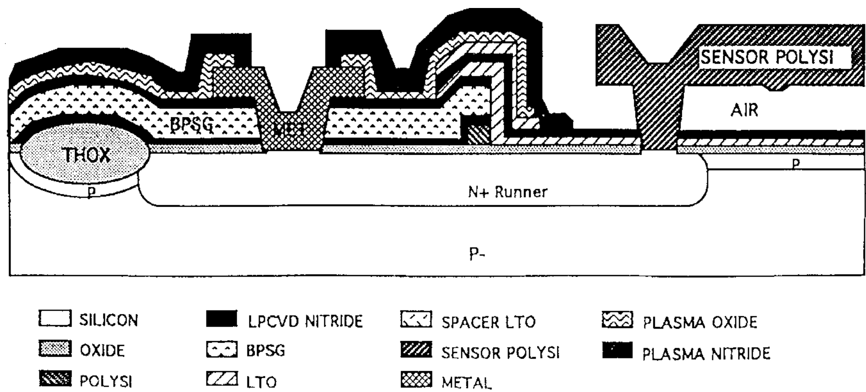


Fig. 5. Cross-section illustration of the Analog Devices BiMEMS integrated MEMS technology. Electrical connections to the structural device are made using the diffused n^+ runner [25].

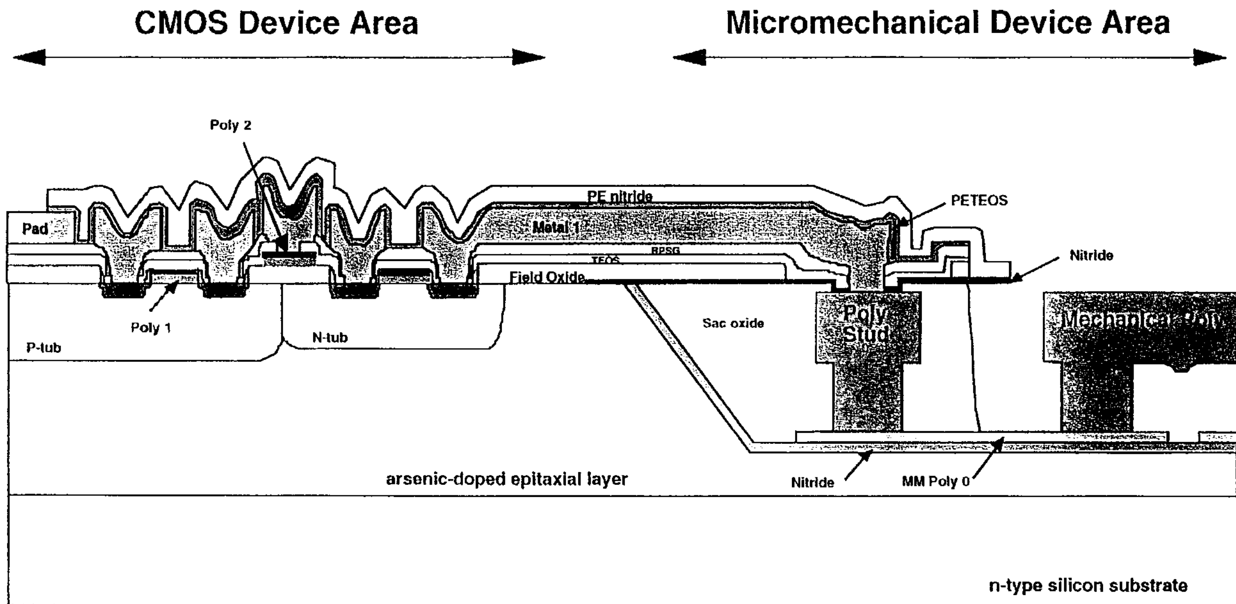


Fig. 6. Cross-section illustration of the Sandia MM/CMOS integrated MEMS technology. The mechanical structure fabricated prior to the electronics is embedded down inside a planarized well [54]. Electrical connections are made down through the poly stud and over via the MMPoly 0 layer.

monolithically integrated MEMS is the interleaved bipolar/CMOS BiMEMS technology at Analog Devices [61].

Alternatives to the conventional integration schemes exist. Another approach is based on a thick (e.g., 10 μm)

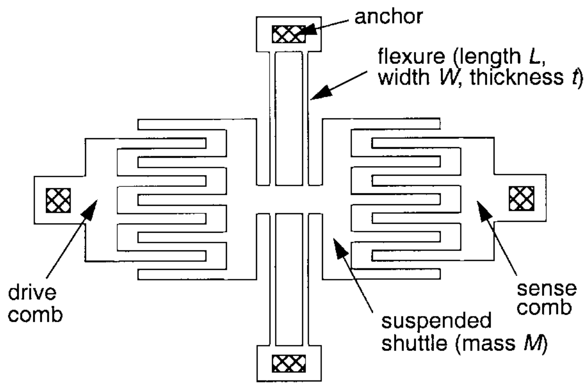


Fig. 7. Layout of a lateral resonator with "straight" flexures.

epitaxial polysilicon "epipoly" film [62]. This epitaxial polysilicon film can be used in conjunction with a bulk silicon release etch [63] or in a purely surface micromachining implementation with a deposited and defined sacrificial layer [64]. Location of the amorphous sacrificial layer determined where the deposited epitaxial silicon would become polycrystalline. Other regions, where the epitaxial deposition was onto single-crystal silicon, became the BiCMOS circuit area [64].

III. Manufacturability

Having reviewed a typical basic process sequence, we consider now design of a mechanical surface microstructure and the factors involved in predicting its mechanical properties. Fig. 7 shows the layout of a lateral resonator, which we will consider fabricating with the process illustrated in Fig. 2. Electrostatic force is applied to the suspended shuttle by applying both dc and ac voltages to the interdigitated comb drive. The resultant motion can be sensed capacitively by means of the sense comb. The flexures in this resonator are modeled as beams with guided end conditions [65]. Any residual stress σ_r in the polysilicon film generates an axial load on these flexures that affects the resonant frequency of the structure. An analytical approximation for the lateral resonant frequency can be found using Rayleigh's method [66]

$$f_o \approx \frac{1}{2\pi}\sqrt{\frac{4E_y t W^3}{ML^3} + \frac{24\sigma_r t W}{5ML}} \quad (1)$$

where E_Y is Young's modulus, L, W, and t are the length, width, and thickness of the flexures, respectively, and M is the mass of the suspended shuttle. Typical flexure dimensions are $L = 150$ μm and $W = t = 2$ μm. At these dimensions, assuming that there is also a slight tensile residual stress, the resonant frequency f_o is between 10 and 100 kHz.

For many applications, f_o is an important parameter of the structure, which must be tightly controlled. Although the effect of axial loads can be more accurately modeled by applying Timoshenko's analysis [67], the expression in (1) is more convenient for discussing the effect of the various material parameters (residual stress, Young's modulus, and density) and the microstructure dimensions on f_o.

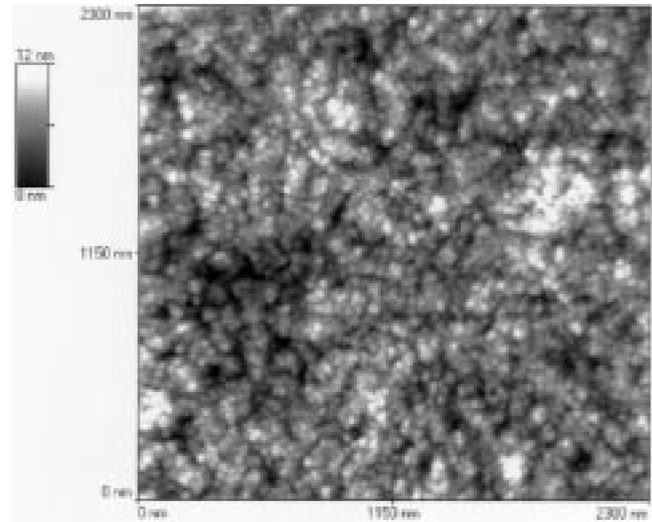


Fig. 8. AFM image of fine-grain polysilicon deposited at 590°C and annealed at 1000°C for 1 h. The average grain size of 25–35 nm and root mean square roughness of 2.8 nm was measured using an Si_3N_4 AFM tip in contact mode [120].

A. Material Properties

1) Residual Stress: Residual stress in polysilicon has been studied extensively, beginning shortly after its first use as a microstructural material in the early 1980's [68]–[70]. Films deposited at temperatures in the vicinity of 625°C have a columnar texture, which corresponds to a compressive average stress that can cause buckling in constrained structures such as the resonator suspension in Fig. 7. By folding the flexures [48], much stress is relieved and buckling is essentially eliminated; hence, folded designs are attractive as a way to design with nonzero residual stresses.

Several types of polysilicon have been used in MEMS designs. The fine-grained, undoped polysilicon developed by H. Guckel and his group at the University of Wisconsin is deposited at 575°C and then annealed to produce a low residual strain material [71], [72]. Conducting regions in this otherwise high-resistivity polysilicon are formed by ion implantation [73].

The basic correlation between residual strain and strain gradient and the texture of undoped and phosphorus-doped polysilicon is now reasonably well understood [74]–[77]. A low thermal-budget polysilicon suitable for post-CMOS integration strategies has been investigated at UC Berkeley [78]. By using a lower phosphine flow and a higher pressure than is used for MOS gate polysilicon and a deposition temperature of 585–590°C, an *in situ* doped and therefore low-resistivity polysilicon is deposited at a relatively rapid deposition rate. After rapid-thermal annealing (RTA) at 950°C, a low tensile residual stress with negligible gradient through the film thickness is produced [78]. This polysilicon material, followed by either RTA or furnace postdeposition anneals, has been used to fabricate flat cantilevers as long as 2 mm [79]. Fig. 8 is an atomic force microscope (AFM) image of this material over a 2.3 μm^2 area—showing the 25–35 nm diameter fine-grain structure.

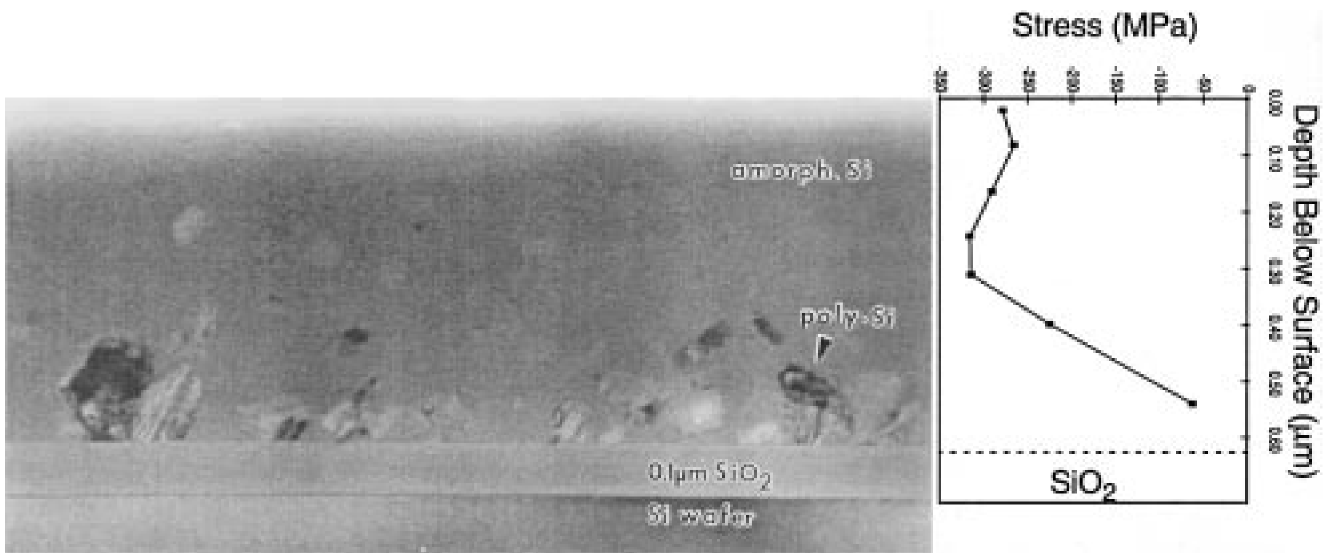


Fig. 9. TEM showing crystallographic inhomogeneity of an as-deposited polysilicon thin film. Crystalline phase near the SiO_2 layer gives way to an amorphous region further up. Measured and plotted through-film stress clearly shows the phase-dependent stress gradient. (Courtesy of P. Krulevitch, UC Berkeley.)

Residual stress can heavily influence the design of microstructures. As seen in (1), the stress term will dominate over the bending term for typical values of L/W. Such is the case for the Analog Devices XL-50 accelerometer [25]. Variations in σ_r for constrained structures lead directly to shifts in the resonant frequency, making it imperative to control stress (wafer to wafer and run to run) in MEMS processes. By folding the flexures, the resonant frequency becomes independent of σ_r, to first order. However, a penalty of using folded flexures is increased susceptibility to out-of-plane warpage from gradients in residual stress through the thickness of the polysilicon microstructure [80]. For the constrained structure in Fig. 7, a tensile residual stress will prevent significant warpage along the axis of the flexures. As-deposited polycrystalline films often have through-film crystallographic inhomogeneity, resulting in high stress gradients. Fig. 9 is a transmission electron micrograph (TEM) that shows as-deposited polycrystalline phase inhomogeneity and its effect on stress. Crystallographic-induced stress gradients, such as the one illustrated in Fig. 9, may be mitigated with postdeposition thermal anneals. Some researchers have used short (30–60 s) infrared-lamp rapid thermal processing anneals at 900°C [23] to alleviate the as-deposited stress of *in situ* phosphorus-doped polysilicon. Long furnace anneals at higher temperatures have also been used to drive dopants into undoped polysilicon films sandwiched between phosphorus-rich oxide layers [20] with good stress-reduction results. Others customize the deposition process rather than rely completely on postdeposition annealing [78]. Device design (e.g., structural anchor placement and/or geometry, folded-suspension design, and location with respect to inertial mass) can also play an important role in mitigating the effects of as-deposited stress gradients [81]. It is not easy to control the stress gradients in mechanical polycrystalline thin-films because it is a sensitive function of deposition and postdeposition process conditions.

2) Young's Modulus: The effective Young's modulus E_Y of polysilicon, since it consists of dispersed crystallites, varies with film texture. However, the observed spread in experimental values for E_Y is too wide to be explained by texture alone. Recent careful measurements with *in situ* phosphorus-doped polysilicon indicate that E_Y can range between 140 and 190 GPa for films deposited at 610°C with high phosphine flow and 585°C with lower phosphine flow [82]. Since (1) indicates that the resonant frequency is proportional to $E_Y^{1/2}$ for structures in which the residual stress term is unimportant (e.g., for those with "folded" suspensions), a polysilicon deposition and annealing process that yields a consistent Young's modulus is very desirable.

The grain size in polysilicon films is typically a large fraction of the film thickness, and these films are technically considered "multicrystalline" films [83]. Due to the small number of grains across a flexure, the effective Young's modulus should exhibit significant random spatial variability from sample to sample across a wafer. Analysis of a probabilistic model leads to a predicted variance of the effective beam modulus of 3% for an example cantilever beam having $L/W = 10$ and an average of three randomized grains in the beam thickness [83]. Typical polysilicon flexures have aspect ratios of $L/W > 50$, with width and thickness both around 2 μm and a grain size less than 0.5 μm. The random grain distribution will be averaged over a longer distance for these flexures, so that a tighter distribution of the effective modulus than was found for the simulated cantilever should be observed.

Recent work at UC Berkeley has measured Young's modulus variations for different conventional *in situ* doped LPCVD polysilicon process conditions (process varied

about nominal temperature and gas flow) and found $145 < E_Y < 195$ GPa for films receiving 30 min postdeposition anneals at 900°C [84]. These data are in close agreement with recent measurements by researchers at Johns Hopkins University on doped films (from MCNC), where the dopant was driven from an encapsulating PSG using 1-h furnace anneals at 1050°C. The high-temperature postdeposition dopant-drive anneal produced a low-stress polysilicon with $E_Y = 170$ MPa ±6 MPa (as previously cited) [47]. Research at the Technical University of Berlin on undoped films exposed to postdeposition anneals that ranged 600–1200°C resulted in $150 < E_Y < 170$ GPa [85].

3) Density: In (1), the density ρ of polysilicon enters through the mass M of the suspended shuttle. The density may vary for different microstructural polysilicon deposition and annealing processes, although this variation has not yet been reported.

B. Microstructure Dimensions

Variation in the microstructure dimensions strongly affects the resonant frequency, as seen in (1) of the structure in Fig. 7. The shuttle mass M is proportional to the thickness t of the polysilicon film and varies directly with lateral dimensions. Lateral dimension variations on M depend on the details of the layout and also are relatively small in percentage compared to the percentage variations in the flexural width W.

With this assumption, (1) for the case where residual stress is negligible reduces to

$$f_o \propto (W/L)^{3/2}. \quad (2)$$

In (2), thickness variation is disregarded because it affects M linearly. For the case where the residual stress term dominates in (1), the resonant frequency reduces to

$$f_o \propto (W/L)^{1/2}. \quad (3)$$

The width-to-length ratio W/L is affected by variations in the masking and etching of the microstructural polysilicon. Systematic lithography-to-etch variations can be eliminated by appropriately biasing the photolithographic masks. What remains is a variation Δ in the linear dimension of etched features, which includes the effect of nonvertical edge slopes that result in flexures with trapezoidal cross sections. For patterned and etched 2 μm-thick structural polysilicon, a reasonable estimate for this variation in a VLSI fabrication facility is $\Delta \approx 0.2$ mm (run to run).

From (2), the variation Δ in lateral dimensions will result in an uncertainty δf_o in the lateral resonant frequency of

$$\frac{\delta f_o}{f_o} \approx \frac{3}{2}\left(\frac{\Delta}{W}\right) \quad (4)$$

for the case where residual stress can be neglected. From (4), a nominal flexure width $W = 2\ \mu$m has an uncertainty in resonant frequency of $\delta f_o/f_o = 15\%$. For the stress-dominated case, (3) indicates that the uncertainty is

$$\frac{\delta f_o}{f_o} \approx \frac{1}{2}\left(\frac{\Delta}{W}\right). \quad (5)$$

The same 2-μm-wide flexure would lead to a 5% uncertainty in the resonant frequency for this case.

From (4) and (5), it is clear that dimensional uncertainties alone can lead to large variations in f_o, especially for the stress-free case. Some method of postfabrication trimming or adjustment is required if f_o is to be fixed exactly, even if all material properties are unvarying. Run-to-run variability in material properties in polysilicon or other surface microstructural films may not be nearly as significant as the dimensional uncertainties in their effect on f_o.

Polysilicon has been shown to be a low-loss, extremely stable mechanical material. Quality factors of 50 000–100 000 in vacuum are typical of polysilicon microresonators [4], [72], [73], [86]. Electrostatically driven polysilicon resonant structures encapsulated in thin-film vacuum chambers have been shown to possess short-term stability better than 0.02 Hz for $f_o = 625$ kHz [27]. Operation for more than three years with lower than 0.4 ppm long-term frequency variation demonstrates the suitability of polysilicon in precision-sensing applications [86].

C. Trimming

Relative inaccuracies and reproducibility of the lithography, etching, and deposition processes translate into a relatively poor micromachining tolerance of around ±5% (e.g., ±0.1 μm for the thickness and the width of a nominally 2 × 2 μm flexure). Conventional macromachining offers superior precision. For example, a precision lathe can machine a shaft of 0.025–1.00 inches in diameter to within ±0.5 mil, for a tolerance of ±2 to ±0.05%, respectively. Because of the lack of precision in micromachining, dimensional control and device performance characteristics will have a wide statistical distribution. Fine-tuning of final device performance can be achieved by postfabrication trimming of electrical and/or mechanical sensor elements or by electrically implementing tuning offsets.

Resonant frequencies can be adjusted by changing the anchor compliance by means of fusible links [87]. Alternatively, laser trimming can be used to modify the anchor or remove mass from the shuttle [88]. After release, the width of polysilicon flexures can be reduced by an isotropic plasma etch if the top and bottom surfaces are protected by an etch-resistant layer [89]. Electrical adjustment of the resonator frequency response is convenient for lateral structures, since an extra electrical port can be added without additional process complexity. For example, a vibrating-ring gyroscope uses lateral parallel-plate capacitors to null mechanical asymmetries in order to balance vibrational modes [90]; or the resonant frequency of a linear comb-drive is adjusted by applying an electrostatic force to a triangularly shaped array of interdigitated tuning comb-drives that engage the moving microstructure [91]. In some applications, such as accelerometers, the variation in mechanical properties of the sense element can be removed in the overall system calibration [92], [93]. Given the variety of options, cost-effective and stable means for trimming surface microstructures can be implemented.

D. Microstructure Release and Surface Passivation

The final step in the process sequence in Fig. 2 involves a wet etch of the sacrificial oxide in hydrofluoric acid. Recently, the basic understanding of this process has improved considerably [94], [95], and models have been developed to predict etching times. There are a variety of methods to prevent the surface-tension-induced collapse and stiction of surface microstructures during the final drying step. The released structures can be sublimation dried (e.g., freeze-dried [96]) using t-butyl alcohol [97] or methanol-water mixtures [98], dried with a supercritical CO_2 technique [99], or dried by evaporation with the meniscus shaped by small features added to the perimeter of the microstructure [100] or by coating the released microstructures with hydrophobic self-assembling monolayer (SAM) films prior to removal from the aqueous stage [101]. Alternatively, a portion of the oxide layer can be substituted by a spun-on polymer spacer after a partial etch of the oxide. After completion of the sacrificial-oxide etch, the polymer spacer prevents collapse during evaporative drying. Last, an isotropic oxygen plasma etches the polymer to release the structure [139], [140]. Other researchers experimented with the idea of using thin polysilicon fusible links as tethers to fix extremely compliant microstructures in place until after the release and dry steps—after which the links could be electrically blown [87].

The release of structures from within thin-film shells can involve long etch times, since access to the sacrificial layer is from channels located at the perimeter of the shell [72], [102], [103]. Thin polysilicon films (less than about 0.2 μm thick) have been found to be permeable to hydrofluoric acid when deposited on PSG [104], [105]. HF penetrates the thin polysilicon films through submicrometer defects, which allow transport of etch products, as well as subsequent rinsing with water and methanol and supercritical CO_2 drying. Incorporation of arrays of thin polysilicon etch-access windows into microshells allows large areas to be etched rapidly [40]. Sealing of the shell with further film depositions seals the defects in the thin polysilicon without significant deposition on surfaces inside the shell [40].

Capillary forces created by the menisci-forming liquid drying from underneath surface-micromachined structures can be much stronger than electrostatic or van der Waals forces. When any of these forces become greater than the normal restoring force of the compliant microstructure, the result can be the collapse and adhesion of that microstructure onto the substrate below—commonly referred to as "stiction." Fig. 10 illustrates how overwhelming the capillary force can be. An example, using the nominal dimensions and spring-constant parameters of the commercially available Analog Devices XL-50 inertial device (1.6 μm vertical separation gap and measured spring constant $kz = 4$ N/m) calculates the pulldown force required at $Fz = 6$ mN—easily attained by capillary attractive forces acting on the total released proof mass (e.g., ADXL-50 proof-mass area approximately 35K μm^2). Normally hydrophilic postrelease surfaces have concave meniscus

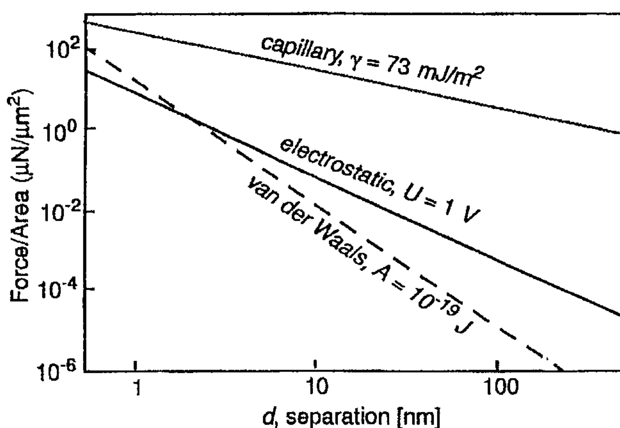


Fig. 10. Comparison of surface forces acting on a microstructural element during postrelease drying. The graph shows capillary force attraction to be greater than either electrostatic or van der Waals [120].

causing surface tension to pull down on the microstructure and are susceptible to capillary force induced stiction. Hydrophobic postrelease surfaces with convex meniscus drying are more desirable. Various approaches have been attempted to reduce the work of adhesion of polysilicon microstructures within the constraints of the fabrication and packaging processes [106], [107].

When capillary forces cause the microstructure to contact an adjacent surface after release, stiction may occur [108]. Many methods have been employed to minimize or eliminate the effects of capillary attraction. Earlier surface micromachines relied on standoff dimples microfabricated into a depression in the sacrificial glass under the structural polysilicon [e.g., refer to the "bump" in the suspended plate in Fig. 2(h)] or by roughening the underlying surface [109]. SAM coatings have been shown to reduce surface adhesion and to be effective at friction reduction in bearings as well [101]. An ammonium fluoride SAM process that results in a hydrogen-terminated extremely hydrophobic silicon surface has been shown to be effective in reducing postrelease stiction [110]. Surface-modification techniques of layers immediately underneath released polysilicon structural layers have been used to reduce stiction [111]. A two-step approach where 1) the HF rinse liquid was substituted with an ultraviolet polymerizing monomer to coat the microstructure and 2) fluorocarbon standoff bumps were deposited immediately prior to removal of the polymer coating also showed improved stiction results to beam lengths of 500 μm [112].

Fluorinated SAM coatings have also shown excellent promise as hydrophobic passivants for polysilicon microstructures in that they have demonstrated measured detachment lengths of 950 μm with extremely low work of adhesion values [113]. This work also observed an improvement of four orders of magnitude for in-use stiction. Diamond-like carbon is also attractive as a hard, low-adhesion surface for polysilicon surface microstructures [114]. Fluorinated-based SAM hydrophobic stiction-free surface passivations, which can survive the packaging tem-

perature cycle and extended device operating life tests, have been developed [79] and tested. Recent experimentation with gas-phased HF etching of tetraethoxysilane (TEOS) sacrificial layers has also emerged as a possible "stiction-robust" release process [116]. The release, drying, and passivation techniques that have become most manufacturably accepted are the sacrificial oxide etch in aqueous HF with the assistance of polymeric spacers, the supercritical CO_2 technique (in the case of an unassisted HF release), and the postrelease surface-coating SAM treatments. The former two are sufficient to prevent "release-induced" stiction; the latter is necessary to prevent "in-use" stiction.

The supercritical drying technique uses CO_2 as the supercritical fluid instead of other supercritical candidate fluids because of its relatively low supercritical pressure (1073 psi) and temperature (31.1°C). The steps involved in this release/drying process are:

i) release by immersion in aqueous HF;
ii) substrate and structure hydrophilic passivation by immersion in a sulfuric peroxide or hydrogen peroxide solution resulting in hydrophilic silicon surfaces;
iii) thorough deionized water rinses followed by a methanol soak to displace the water;
iv) methanol-soaked samples placed in the supercritical drying chamber for drying.

Once in the pressure vessel, the methanol is completely displaced by liquid CO_2 at 1200 psi. Drying takes place by passing from the liquid phase to the gas phase through the supercritical region, from position 1 to 2 to 3 in Fig. 11. First, the CO_2-pressurized vessel is heated until the liquid CO_2 makes the transition to the supercritical phase ($T > 31.1°C$). Venting the vessel to rapidly reduce the pressure isothermally above the CO_2 supercritical temperature results in dried "stiction-free" surfaces. Because the liquid-to-vapor transition occurs in the supercritical region, there are no attractive capillary forces to cause stiction during the drying phase. Supercritical CO_2 drying aids in preventing "release-induced" stiction only by the fact that the microstructures never contact during the drying step. Postdrying contact of hydrophilic surfaces will result in stiction—hence the ultimate need for SAM's.

SAM coatings have been used with polysilicon and metal surface-micromachined devices to prevent postrelease stiction and in-use stiction or experimentally as a lubricant [79], [101], [113], [116]. Some studies have been done to compare this technique with those previously considered standard [117]–[119]. SAM coatings are not only extremely hydrophobic (measured water contact angles of 114° are common) but also greatly reduce the work of adhesion as compared to normal hydrophilic surfaces. Typically, the SAM precursor is a long-chain hydrocarbon alkyl group with a chlorinated silicon head group. Small amounts of the SAM precursor are mixed in organic solvents (e.g., carbon tetrachloride, hexadecane, chloroform, iso-octane) used to treat the released microstructure containing substrate.

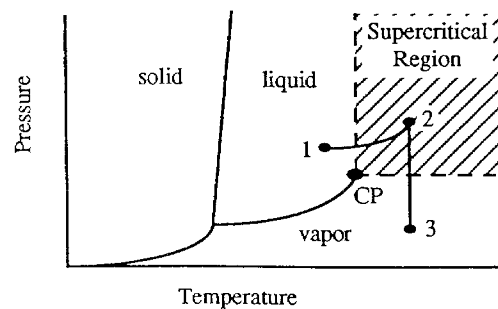


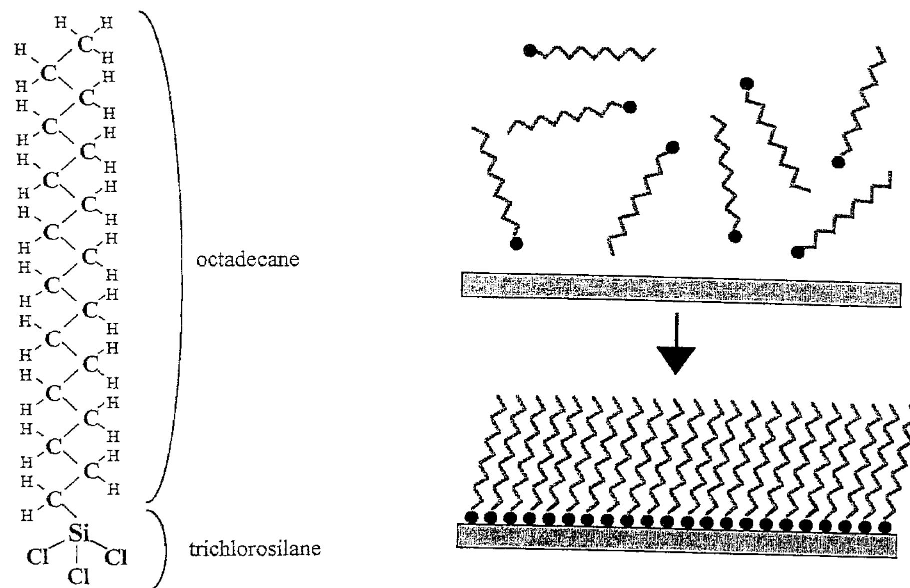
Fig. 11. Phase diagram of a supercritical fluid. 1) Exchange methanol with liquid CO_2 at 20°C and 1200 psi. 1–2) Close off vessel and heat liquid CO_2 to a supercritical fluid. There is no interface formed during this transition. 2–3) Vent vessel at a constant temperature above Tc. The CO_2 exists in gaseous form [99].

Early work with polysilicon micromotors [101] experimented with seven SAM precursors or differing alkyl chain lengths. Two, octadecyltrichlorosilane (OTS) and trifluoropropyl trichlorosilane (TFP), were found to be effective in improving the performance of flange-bearing polysilicon micromotors. Later work [113] improved on the OTS process by eliminating the need for using environmentally "unfriendly" carbon tetrachloride. It demonstrated that OTS could be used to prevent stiction of extremely compliant 1000-μm-long polysilicon beams and measured the comparative work of adhesion for this and other passivation treatments. This work was later extended [79] by switching to a perfluorodecyltrichlorosilane SAM precursor (FDTS), which required only iso-octane solvent, was simpler to use, demonstrated improved efficacy, and, more important, maintained microstructural in-use stiction performance at temperatures up to 400°C in nitrogen or air—a necessary condition should conventional hermetic IC packaging temperatures be required.

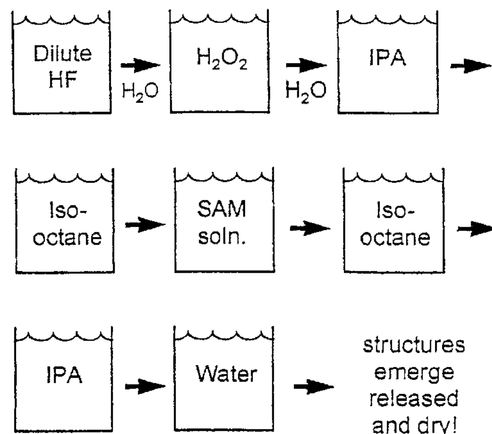
In principle, the SAM coating process involves four steps, as clearly described by Deng [101]:

i) hydration of the silicon substrate;
ii) hydrolysis of the chlorinated head group (e.g., trichlorosilane);
iii) covalent bonding of the SAM by the head group;
iv) cross linking again at the head group to form siloxane network at the surface.

A schematic representation of the application of this process as followed from the release step and using an OTS precursor is depicted in Fig. 12. In this process flow, the postrelease H_2O_2 soak hydrates all exposed silicon surfaces; the isopropyl alcohol and iso-octane organic rinses are designed to remove all traces of water, which would contaminate the SAM solution; reverse organic rinses remove any residual SAM precursor and the final pull being from a liquid with high surface energy (e.g., water). Hydrophobic SAM-passivated samples emerge released, dry, and ready for use.



(a)



(b)

Fig. 12. OTS SAM schematic representation. (a) OTS precursor molecule with chlorinated head group depicted covalently bonded to surface and cross linked to adjacent molecules. (b) Schematic representation of the necessary process steps [120].

IV. 3-D Surface Microstructures

Since surface microstructures are formed using the IC planar technology from deposited thin films, as shown in Fig. 2, they are typically laminar. However, LPCVD processes can be conformal and allow the deposition of sacrificial and structural films underneath the edges of previously etched features. An early example is the self-aligned micromotor flange bearing [9]. The fabrication of hinges for vertical assembly of MEMS was a major advance toward achieving 3-D microstructures [121]. Elastic joints of polyimide have also been demonstrated for postrelease assembly of 3-D polysilicon microstructures [122].

An emerging application for 3-D microstructures is as passive or active components on a silicon optical bench. The application of MEMS to optical systems is very promising; the new field has been called "microphotonics." Fig. 13 is an SEM of a Fresnel lens that has been surface micromachined in polysilicon and then erected using hinge

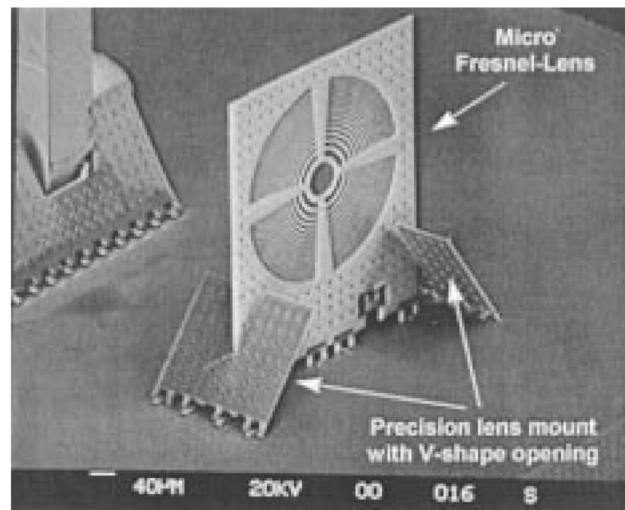


Fig. 13. SEM of a Fresnel lens [123].

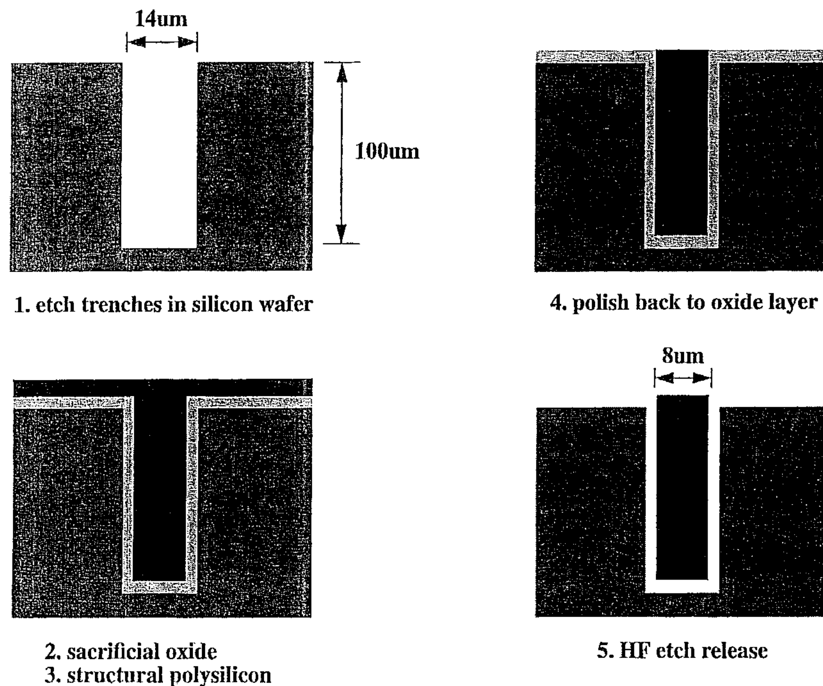
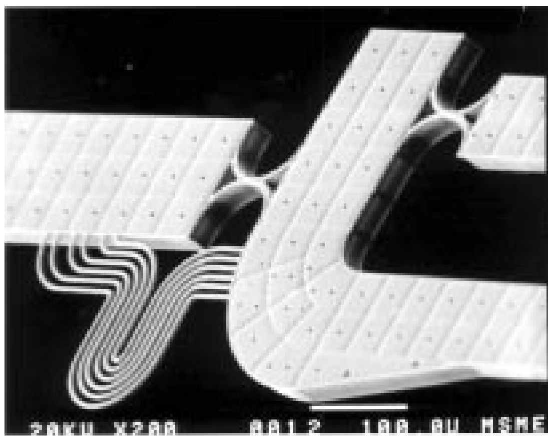


Fig. 14. Outline of HexSil process. 1) Deep silicon mold etch. 2) Sacrificial layer deposition. 3) Structural layer deposition. 4) Chemical-mechanical polish (optional). 5) Release and extract molded part.

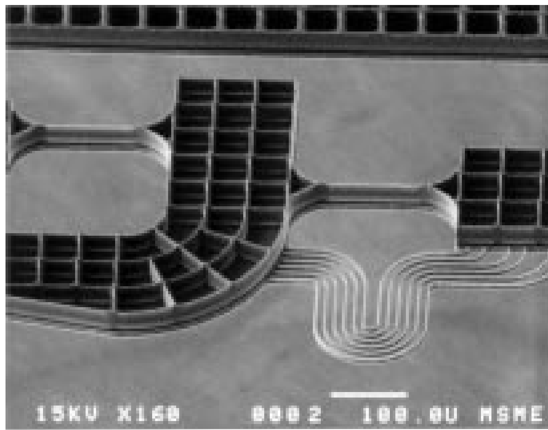
structures and locked in place by micromachined tabs, liberating the structure from the horizontal plane of the wafer [123]. Active alignment of 3-D lenses and mirrors is important for achieving low-cost, robust optical systems. Polysilicon surface microactuators can address this need, as has been demonstrated by linear vibromotors coupled to an aluminum-coated polysilicon mirror [124]. The comb-driven actuators, made using conventional surface micromachining, vibrate and impact the slider. Displacements of the slider are coupled through a hinged linkage to the mirror, which is elevated off the substrate. Vibromotors are a robust solution to mirror actuation, as they are resistant to sticking of the slider or the linkage. A more detailed description of the 3-D implementation of a surface-micromachined microphotonics technology can be found in this issue [17].

A different extension of surface micromachining is capable of making 3-D microstructures without hinges. The central idea is to use deep-etched patterns in the silicon wafer as molds for deposited films. Etching of a sacrificial film releases the microstructure from the mold, which can be reused. The molded structures are extracted and can be put into service either as independent devices or attached to another substrate as part of a more complex system. Fig. 14 is an outline of the fabrication sequence for the "HexSil" microparts [31]. Mold fabrication in step 1 uses deep RIE of the silicon wafer to form grooves with vertical sidewalls to depths of up to 100 μm. The mold could be fabricated using any machining technique; for example, diamond sawing of bonded wafers has been used to make parts nearly 1 mm in thickness. The thicknesses of the sacrificial oxide and structural polysilicon films are selected to completely fill the grooves in the wafer, as shown in steps 2 and 3 in Fig. 14. At this point, the polysilicon is removed from the surface of the wafer by lapping and polishing. Deposition and patterning of a second polysilicon layer forms cross linkages between the high-aspect-ratio molded polysilicon structures. An extended etch in concentrated HF is needed to remove the sacrificial oxide from the deep grooves. After etching the part is free of the mold, as shown in step 5, although it can be held in place by flexures etched in the second polysilicon layer. Fig. 14 shows that once the "HexSil" part is ejected from the mold, the silicon substrate mold can be recycled.

Fig. 15 is an SEM of a resulting polysilicon structure after release from the mold. Both top (a) and bottom (b) views are depicted to show the mold features. Appropriate design of surface and mold-fill regions can result in both rigid and flexible members simultaneously fabricated on one device. A characteristic feature of this molding process is that large-area structures are built from a rigid network of interconnected segments, the width and depth of which are defined by the groove dimensions. This molding concept can be applied to other materials that can be deposited conformally, such as electroless nickel [125], and LPCVD films such as silicon nitride and tungsten. Composite structures are possible if the outside layer can withstand the sacrificial etching process. Vapor-phase silicon etching using xenon



(a)



(b)

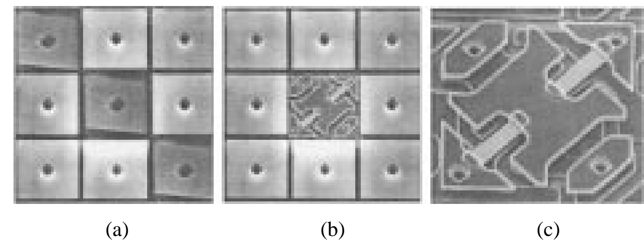
Fig. 15. HexSil molded polysilicon structure. (a) Surface polysilicon flex cable for interconnects between rotating rigid HexSil beams. (b) Bottom view of structure in (a), showing the molded honeycomb structure of the rigid beams. Mold depth was 45 mm [126].

difluoride [36] could also be very useful in selective etching of polysilicon sacrificial layers in a modified HexSil process.

Extending surface-micromachined designs into the third dimension has also been the motivation behind the sealed cavity, silicon fusion bonded, deep RIE process [127], the single-crystal reactive etching and metallization process [128], and the high-aspect-ratio silicon-on-insulator integrated technology with embedded interconnect and trench isolation process [33]. These technologies all rely on deep anisotropic silicon etching [129] and hope to improve the performance of surface-micromachined inertial instruments by achieving greater separation of modal frequencies, providing larger proof masses and increasing capacitive sensing elements. Details concerning implementation and recent developments of deep silicon etching for 3-D structures are reviewed in this issue [130].

V. Alternative Materials for Surface Micromachining

Surface micromachining has been done with a number of material suites in order to make use of various desirable



(a) (b) (c)

Fig. 16. Closeup photographs of aluminum mirrors on the surface of a DMD and the underlying substructure. View (a) shows nine mirrors with three mirrors tilted to the on position, $+10^{\circ}$. In View (b), the central mirror is removed to expose the underlying, hidden-hinge structure. View (c) shows a closeup view of the mirror substructure. (Figure details as described in [132].)

properties. Among those are controlled residual stress values, Young's moduli, film morphologies, stiffnesses, electrical conductivities, optical reflectivities, thermal budgets during deposition, etch properties, and ease of deposition.

Metals were actually the earliest focus [2]. where selective removal of metals was the technique employed for sacrificial release. The optical reflectivity of aluminum has been an attractive feature for the Texas Instruments (TI) deformable-mirror spatial light modulator [131], which forms the deformable mirror display (DMD) [28]. The DMD uses three layers of thin-film aluminum for the mirror and its suspension system. There are two air gaps between these layers formed when the sacrificial resist layer is removed. Fig. 16 shows a closeup of the aluminum mirrors and underlying structure. The very high conductance of aluminum was a critical feature in an MEMS design at the Berkeley Sensor & Actuator Center, UC Berkeley—a surface-micromachined, low-noise, voltage-controlled oscillator for tunable radio-frequency filters [133]. Aluminum structural layers had sheet resistances 100 times lower than that of equally thick phosphorus-doped polysilicon. Aluminum-film sacrificial-layer technologies require low process temperatures, allowing easy post-IC integration with CMOS, which is important for system performance. Other metals, including CVD tungsten [134], [135], electroplated nickel [136], copper, and nickel-iron [137] have also been used in surface-micromachined MEMS applications.

Different sacrificial materials have been used with surface-micromachined metal systems, including spin-on and vapor-deposited organics. These films can be removed using oxygen-plasma processing and cured to allow aluminum deposition and etching. Organic photoresist materials [133], polyimides [138], and parylene [139] have been employed to provide a dry plasma-release step in contrast to the aqueous acid release, used with polysilicon-film micromachining. Vapor-deposited parylene [139] was originally conceived to augment the aqueous hydrofluoric acid release etch of silicon dioxide in polysilicon micromechanical fabrication by providing a two-step process with pedestal standoff pillars that served to prevent stiction.

Silicon nitride, the mechanical material of choice for the deformable grating optical modulator fabricated at Stanford University [141], was selected because of the need for

very thin (e.g., 100–200 nm), stress-optimized, specular thin films. Amorphous silicon nitride did not have the crystallographic grain "roughness" characteristic of polysilicon, and as a result was smooth enough to allow for direct deposition of a reflecting layer. The as-deposited tensile stress of silicon nitride thin-films could also be readily adjusted lower by making the film silicon rich [140]. Recent research now clearly shows that high-temperature anneals in an oxidizing ambient can further lower the residual stress to near zero MPa [143]. Thermophysical and mechanical properties of as-deposited low-stress silicon nitride films had already been studied [144], [145].

Recently, researchers at Carnegie-Mellon have implemented laminated structures consisting of back-end CMOS silicon dioxide, silicon nitride, and aluminum layers as the freed mechanical "material" [146]. The novelty of this concept is the duality of function served by the metallization and dielectric layers, normally used only for electrical interconnect in the IC process. In the MEMS process, these layers also serve as movable mechanical elements. Release etching is executed using three maskless dry etching steps after completion of the CMOS process. Making use of material layers already present in conventional CMOS fabrication, and implementing them for MEMS applications by simply adding back-end etch steps, greatly simplifies electronics integration and foundry issues; the drawback is found in the mechanical limitations shown by the laminate materials. Other post-CMOS maskless-etch release steps have been tried using xenon difluoride, an isotropic and extremely selective gaseous silicon etchant, to free mechanical devices made of thermal silicon dioxide [147]. Although xenon difluoride etches the underlying silicon substrate, a procedure normally associated with "bulk" micromachining, its implementation as a release etch for structures formed in overlying films is a characteristic of surface micromachining.

Xenon difluoride can also be employed as a surface-micromachining release etch to remove selectively a polysilicon sacrificial layer. With this approach, metal layer micromachining could be realized without the need for organic sacrificial materials. Conversely some researchers have implemented a sacrificial aluminum etching process [148] to gain the advantage of process compatibility with conventional IC fabrication.

The Texas Instruments aluminum DMD technology demonstrates a remarkable density of mechanical and electrical integration. The TI technology is capable of fabricating 1.3 million movable mirrors in a 3.9 cm^2 mechanical active area. Texas Instruments reports a 95% die yield with <10 ppm defective pixel density and 0.5% per year in-use field failure rates [149].

VI. Micropackaging

The final MEMS packaging step can be the most costly taken to produce a product. Extreme care must be taken when handling MEMS with released mechanical structures during packaging because they are susceptible to contact damage and particulate contamination to which they may be exposed. The packaging for MEMS should be done in the same class-10 cleanroom in which the devices are fabricated. Customized packaging equipment has been specifically modified to handle MEMS in production [149].

Silicon-to-silicon fusion or glass-to-silicon anodic wafer bonding is used to form hermetic pressure-controlled sealed cavities either die by die or at the wafer level [150]. These techniques can be further improved where vacuum integrity within the cavity is necessary by using *in situ* nonevaporable getters activated once the cavity has been sealed [43].

The implementation of wafer-level packaging schemes to seal and protect micromechanical elements prior to dicing (sawing of wafer into individual die) is an important development. Early efforts to microencapsulate resonant silicon structures with wafer-level microfabricated vacuum shells showed promise [151]. These shell processes were later adapted to vacuum-encapsulated polysilicon MEMS devices [152]. Since then, a number of approaches have been demonstrated: for example, a sealed micropirani gauge [39] in which an LPCVD silicon nitride seal on a cavity was machined using surface micromachining. In the pirani-gauge project, the structural element was released using a wet etch that entered the cavity through strategically placed holes. The vacuum sealing occurred during a subsequent capping LPCVD nitride film deposition. This idea was later exploited to encapsulate and vacuum seal a polysilicon surface-micromachined resonator [102]. In both cases, electrical interconnect to the cavity-sealed structure was made through thin-film polysilicon electrical feedthroughs deposited under the silicon nitride. A novel encapsulation technique not requiring lithographically defined etch holes relies on the fact that very thin-film polysilicon is permeable to aqueous hydrofluoric acid [104]. By forming shells using etch-access permeable polysilicon windows, a similar evacuation and hermetic sealing could be realized [40]. Fig. 17 shows the basic fabrication steps used in LPCVD thin-film microcavity shell formation—in this case, an example combining both bulk and surface micromachining to form a larger cavity. Fig. 18 is an SEM of a released nitride encapsulated surface-micromachined polysilicon resonator.

Recent work combining molded polysilicon micromachining and wafer-to-wafer microstructure transfer using gold/silicon eutectic bonding has fabricated microshells on a donor substrate that can be transferred en masse onto micromechanical elements on a target substrate [41]. The released caps are fixed to the donor substrate by tethers that break away during the postbond wafer separation. Structural ribs can be designed into the molded polysilicon part to provide support across the cavity ceiling (refer to Fig. 19). Planarized multipinout feedthroughs are fabricated on the recipient wafer to provide electrical access once the cap is in place.

VII. Microassembly Processes

The polysilicon 3-D surface-micromachining processes described in the previous section require postrelease assembly or parts handling. In the case of HexSil, the

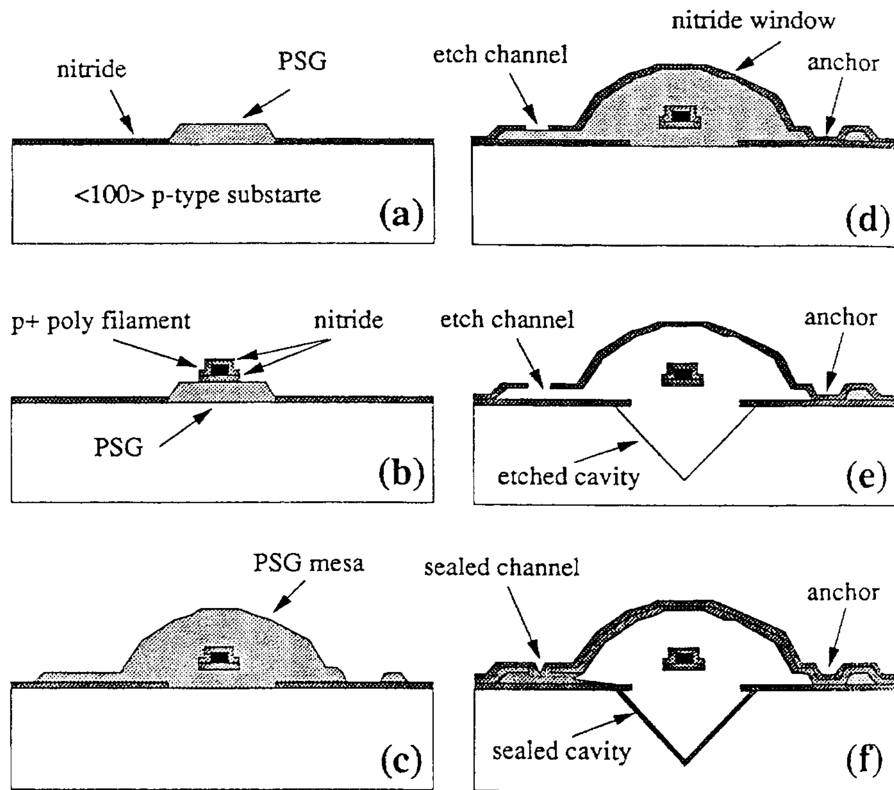


Fig. 17. Simplified wafer-level vacuum encapsulation fabrication process. (a) Initial spacer deposition. (b) Nitride-coated filament deposition and definition. (c) PSG mesa and etching channel definition. (d) Nitride window deposition and etch-hole definition. (e) PSG removal and bulk silicon groove etch (optional). (f) Etch holes sealed with additional nitride [37].

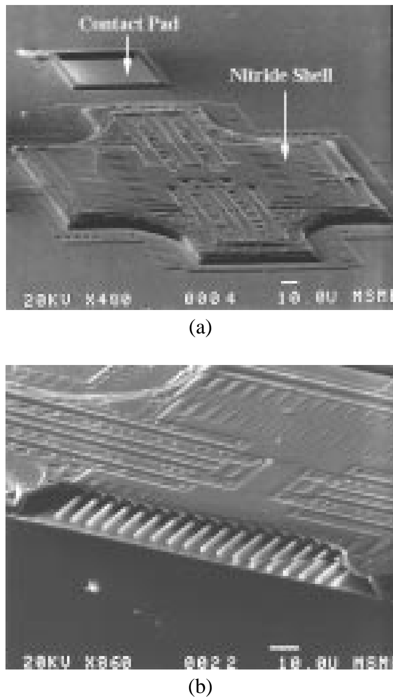


Fig. 18. LPCVD silicon nitride microshell encapsulation. (a) SEM of a vacuum-encapsulated lateral microresonator (shell height $= 12\ \mu$m). (b) Broken shell exposes released microstructure inside [102].

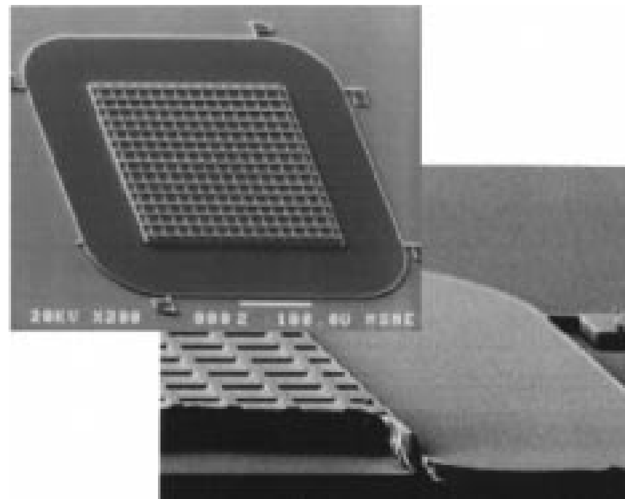


Fig. 19. HexSil fabricated vacuum cap. Above: SEM of vacuum cap after transfer; some tethers still partially attached; flange surrounding ribbed square is 100 μm wide. Below: Cleaved cross section of ribbed cap showing where microstructural device would be. Cap structure was transferred to the target wafer (shown) using a "massively parallel" wafer-to-wafer device transfer process [41].

final release yields parts with submillimeter dimensions that must then be incorporated into a 3-D microsystem. Research on techniques for self- or automated assembly of microstructures is under way [87], [126], [153]–[157], but much is yet to be learned. Given the known techniques for tailoring the surfaces of microstructures, it is plausible that the submillimeter-scale equivalent of chemical binding sites can be developed. As microassembly matures as a

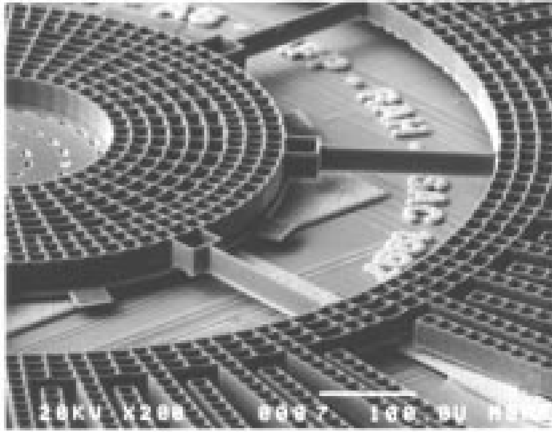


Fig. 20. Transfer of a high-aspect-ratio molded polysilicon microactuator onto CMOS chip realized using a conventional flip-chip technology with electroplated copper pads and indium bumps for a cold welded process. Microactuator is 35 μm high and 2.6 mm in diameter. Electrical interconnect to underlying electronics is achieved using a copper seed layer to a second aluminum metal contact (not shown). Broken polysilicon tether plates are visible at edges [158].

subdiscipline of MEMS technology, it should enable low-cost, sophisticated 3-D components for microphotonics, and many other applications.

An approach to microassembly based strongly on IC technologies is to bring flip-chip-like methods into use for MEMS devices [158]. Initial results indicate that this assembly technique could be appropriate for batch transfer of polysilicon surface-micromachined components as well as molded polysilicon HexSil structures. Fig. 20 shows a transferred/assembled molded polysilicon microactuator on top of and electrically connected to underlying CMOS circuitry. Whether by this or other methods, the advent of postfabrication assembly of microstructures raises the possibility for the separate fabrication of MEMS and CMOS while achieving performance comparable to monolithic technologies. These wafer-to-wafer microdevice transfer processes [41], [155], [158] have begun to blur differences between monolithic and hybrid integration strategies. The ability to build structures on one wafer and transfer them to another target wafer to implement functionality frees the MEMS designer from requiring process compatibility between the circuit and micromechanical fabrication and should prove to be an important development.

VIII. Conclusions

Surface micromachining has developed since the early 1980's from academic "proof-of-concept" demonstrations into a commercially important technology. Material properties are now understood sufficiently that polysilicon-based surface-micromachined MEMS are a commercial success. Integration of polysilicon microstructures with CMOS has made monolithic sensing systems feasible. In these sophisticated interface and control circuits, one can fully exploit simple mechanical elements [29]. These integrated technologies continue to evolve, with different options on how best to merge microstructure and electronic processes. Surface micromachining of metal films is also a maturing technology for both plated [90], [137], [159] and sputtered [131], [133] films, although the literature on material properties is much less extensive. Improved understanding of surface adhesion effects and methods to control them has resulted in a level of reliability normally associated with mature IC fabrication [149].

Greater emphasis is being placed on improved cost-effective packaging schemes for micromachined devices. These range from conventional hermetic packages to bonded wafer schemes to wafer-level encapsulation. Some devices require the additional requirement of long-term stable vacuum enclosures. It is expected that future technological advances will address the challenges of packaging surface-micromachined MEMS.

Academic research groups are now proving the feasibility of surface processes for elaborate 3-D microstructures. Although they are derivative of the basic sacrificial-layer etching concept, postrelease assembly is required. Techniques for self-assembly are critically needed in order to make these processes practical. In summary, after nearly two decades, the "second wave" of surface micromachining is still gathering momentum.

Acknowledgment

The authors are grateful to their colleagues and current and former graduate students, who have contributed much to the development of surface micromachining and its applications.

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