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EE C247B - ME C218 Introduction to MEMS Design Spring 2015

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Module 16: Sensing Non-Idealities & Integration

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Lecture Outline

- Reading: Senturia Chpt. 14, 15
- Lecture Topics:
 - ☞ Ideal Op Amps
 - ☞ Op Amp Non-Idealities
 - ☞ MEMS-Transistor Integration
 - Mixed
 - MEMS-First
 - MEMS-Last
 - ☞ Op Amp Non-Idealities (cont.)

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Ideal Operational Amplifiers

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Ideal Op Amp

- **Equivalent Circuit of an Ideal Op Amp:**

- **Properties of Ideal Op Amps:**

1. $R_{in} = \infty$ → 4. $i_+ = i_- = 0$
2. $R_0 = 0$
3. $A = \infty$ → 5. $v_+ = v_-$, assuming $v_0 = \text{finite}$ **Why?**

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Ideal Op Amp (cont)

Properties of Ideal Op Amps:

- $R_{in} = \infty \rightarrow 4. i_+ = i_- = 0$
- $R_0 = 0$
- $A = \infty \rightarrow 5. v_+ = v_-, \text{ assuming } v_0 = \text{finite}$

Why? Because for

$$\infty(v_+ - v_-) = v_0 = \text{finite}$$

$$\therefore v_+ - v_- = 0 \rightarrow v_+ = v_-$$

$$\frac{v_0}{\infty} \Rightarrow \text{virtual short circuit (virtual ground)}$$

Big assumption! ($v_0 = \text{finite}$)

How can we assume this? We can assume this only when there is an appropriate negative feedback path!

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Inverting Amplifier

- Verify that there is negative FB.
- $\therefore v_0 = \text{finite} \rightarrow v_+ = v_- \rightarrow$ node attached to (-) terminal is virtual ground.
- $i_- = 0 \therefore i_1 = i_2$

NOTE: Gain dependent only on R_1 & R_2 (external components), not on the op amp gain.

$$i_1 = \frac{v_i - 0}{R_1} = \frac{v_i}{R_1} = i_2$$

$$v_0 = 0 - i_2 R_2 = -i_2 R_2 \Rightarrow v_0 = -\left(\frac{v_i}{R_1}\right) R_2 = -\frac{R_2}{R_1} v_i \therefore \frac{v_0}{v_i} = -\frac{R_2}{R_1}$$

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Transresistance Amplifier

Take R_1 away

- Verify that there is neg. FB \rightarrow yes, since same FB as inverting amplifier
- Thus, $v_0 = \text{finite} \rightarrow v_+ = v_- \rightarrow$ (-) terminal is virtual ground
- $i_- = 0 \rightarrow i_1 = i_2$

An inverting amplifier is just a transresistance amplifier with an R_1 to convert voltage to current!

$$v_0 = -i_2 R_2 = -i_1 R_2 \Rightarrow \frac{v_0}{i_i} = -R_2$$

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Integrator-Based Diff. Position Sensing

$i_0 = i_1 + i_2 = N_P(sC_1) - N_P(sC_2) = N_P s(C_1 - C_2)$

$\therefore v_0 = -i_0 \left(\frac{1}{sC_F}\right) = -N_P \left(\frac{C_1 - C_2}{C_F}\right)$

$\frac{v_0}{v_P} = -\frac{C_1 - C_2}{C_F} \Rightarrow$ A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

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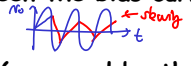
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Non-Ideal Operational Amplifiers

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Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they ...
 - ☞ Generate noise
 - ☞ Have finite gain, A_o
 - ☞ Have finite bandwidth, ω_b
 - ☞ Have finite input resistance, R_i
 - ☞ Have finite input capacitance, C_i
 - ☞ Have finite output resistance, R_o
 - ☞ Have an offset voltage V_{OS} between their (+) and (-) terminals
 - ☞ Have input bias currents
 - ☞ Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
 - ☞ Have finite slew rate 
 - ☞ Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

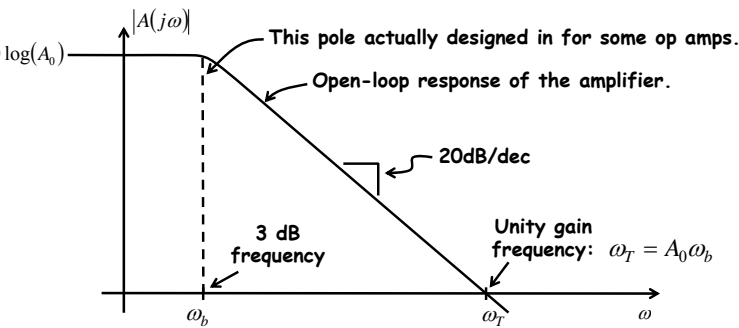
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Finite Op Amp Gain and Bandwidth

- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_o}{1 + \frac{s}{\omega_b}}$
 - ← Finite Gain
 - ← Finite Bandwidth
- For $\omega \gg \omega_b$:

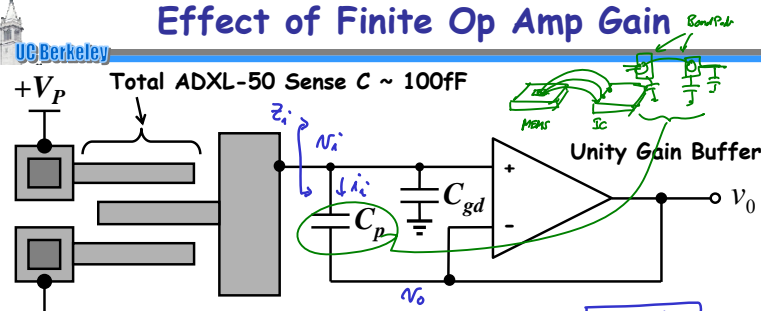
$$A(s) \approx \frac{A_o}{(s/\omega_b)} = \frac{A_o \omega_b}{s} = \frac{\omega_T}{s} \rightarrow \text{Integrator w/ time const. } 1/\omega_T$$



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Effect of Finite Op Amp Gain



Total ADXL-50 Sense C ~ 100fF

Unity Gain Buffer

$N_o = A_o(N_i - N_-) = A_o(N_i - N_o) \rightarrow N_o(1 + A_o) = A_o N_i \rightarrow \frac{N_o}{N_i} = \frac{A_o}{1 + A_o}$

Get $Z_i = \frac{N_i}{I_i}$: $I_i = (N_i - N_o) s C_p = N_i (1 - \frac{A_o}{1 + A_o}) s C_p = N_i \frac{1}{1 + A_o} s C_p$

$\therefore \frac{N_i}{I_i} = Z_i = \frac{1}{s \left[\frac{C_p}{1 + A_o} \right]}$ $C_{eff} = \frac{C_p}{1 + A_o}$

No larger zero!

Ex: $A_o = 100, C_p = 2pF$
 $\Rightarrow C_{eff} = \frac{2pF}{101} = 20fF$
 Not negligible compared w/ ADXL-50 $C_{tot} \sim 100fF!$

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Integration of MEMS and Transistors

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Integrate or Not?

- **Benefits:**
 - ↪ Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
 - ↪ Better reliability
 - ↪ Reduced size → lower cost?
 - ↪ Reduced packaging complexity → integration is a form of packaging → lower cost?
 - ↪ Higher integration density supports greater functionality
- **Challenges:**
 - ↪ Temperature ceilings imposed by the transistors or MEMS
 - ↪ Protecting one process from the other
 - ↪ Surface topography of MEMS
 - ↪ Material incompatibilities
 - ↪ Multiplication of yield losses (versus non-integrated)
 - ↪ Acceptance by transistor foundries

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250 nm CMOS Cross-Section

28 masks and a lot more complicated than MEMS!

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Merged MEMS/Transistor Technologies (Process Philosophy)

- MEMS-Last: Circuits → Pass./Prot. → μMechanics
- Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot.
- MEMS-First: μMechanics → Pass./Prot. → Circuits

Fully Integrated μMechanical Resonator Oscillator

- **Mixed:**
 - ↪ **problem:** multiple passivation/protection steps ⇒ large number of masks required
 - ↪ **problem:** custom process for each product
- **MEMS-first or MEMS-last:**
 - ↪ **adv.:** modularity ⇒ flexibility ⇒ less development time
 - ↪ **adv.:** low pass./protection complexity ⇒ fewer masks

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Analog Devices BiMEMS Process

- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

SILICON	LPCVD NITRIDE	SPACER LTO	PLASMA OXIDE
OXIDE	BPSG	SENSOR POLYSI	PLASMA NITRIDE
POLYSI	LTO	METAL	

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Analog Devices BiMEMS Process (cont)

- **Examples:**

Old \longrightarrow New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

- Can you list the advances in the process from old to new?

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Merged MEMS/Transistor Technologies (Process Philosophy)

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MEMS-First Integration

- **Modular technology** minimizes product updating effort
 - ↳ **Module 1:** micromachining process (planar technology)
 - ↳ **Module 2:** transistor process (planar IC technology)
- **Adv.:** (ideally) no changes needed to the transistor process
- **Adv.:** high temperature ceiling for some MEMS materials
- **Challenges:**
 - ↳ Reducing topography after MEMS processing so transistors can be processed
 - ↳ Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
 - ↳ Getting transistor foundries to accept pre-processed wafers

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MEMS-First Integration

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- Problem:** μ structural topography interferes with lithography
 ↳ difficult to apply photoresist for submicron circuits

- Soln.:** build μ mechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]

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MEMS-First Ex: Sandia's iMEMS

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- Used to demonstrate functional fully integrated oscillators
- Issues:**
 - ↳ lithography and etching may be difficult in trench → may limit dimensions (not good for RF MEMS)
 - ↳ μ mechanical material must stand up to IC temperatures (>1000°C) → problem for some metal materials
 - ↳ might be contamination issues for foundry IC's

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Bosch/Stanford MEMS-First Process

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- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

[Kim, Kenny Trans'05]

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Problems With MEMS-First

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- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
 ↳ Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
 ↳ thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

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UC Berkeley Foundry Acceptance of MEMS-First?

- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
 - ↳ Feature sizes on the nm scale for billions of devices
 - ↳ Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
 - ↳ Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon

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UC Berkeley Merged MEMS/Transistor Technologies (Process Philosophy)

The diagram shows three integration philosophies for a Fully Integrated μ Mechanical Resonator Oscillator:

- Post-Circuits:** Circuits → Pass./Prot. → μ Mechanics
- Mixed:** Circuits → Pass./Prot. → μ Mechanics → Pass./Prot. → Circuits
- Pre-Circuits:** μ Mechanics → Pass./Prot. → Circuits

- **Mixed:**
 - ↳ **problem:** multiple passivation/protection steps \Rightarrow large number of masks required
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- **MEMS-first or MEMS-last:**
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UC Berkeley MEMS-Last Integration

- **Modular technology** minimizes product updating effort
 - ↳ **Module 1:** transistor process (planar IC technology)
 - ↳ **Module 2:** micromachining process (planar technology)
- **Adv.:** foundry friendly
 - ↳ Virtually any foundry can be used \rightarrow can use the lowest cost transistor circuits (big advantage)
- **Adv.:** topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- **Issue:** limited thermal budget limits the set of usable structural materials
 - ↳ Metallization goes bad if temperature gets too high
 - ↳ Aluminum grows hillocks and spikes junctions if $T > 500^\circ\text{C}$
 - ↳ Copper diffusion can be an issue at high temperature
 - ↳ Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

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UC Berkeley Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
 - ↳ Polysilicon dep. $T \sim 600^\circ\text{C}$; nitride dep. $T \sim 835^\circ\text{C}$
 - ↳ 1100°C RTA stress anneal for 1 min.
 - ↳ metal and junctions must withstand temperatures $\sim 835^\circ\text{C}$
 - ↳ tungsten metallization used with TiSi_2 contact barriers
 - ↳ *in situ* doped structural polySi; rapid thermal annealing

The diagram shows a cross-section of the process layers on an n-substrate:

- Ground Plane Polysilicon
- Structural Polysilicon (Suspended Beams)
- Si_3N_4 layer
- TiSi_2 Contact Barrier
- Tungsten Interconnect
- Poly-to-Poly Capacitor
- Thermal SiO_2
- pwcl

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Surface Micromachining

The diagram illustrates the surface micromachining process in two stages. In the first stage, a silicon substrate with a p-well contains a layer of structural material (e.g., polysilicon, nickel) on top of a sacrificial oxide layer. A release etch barrier is also present. In the second stage, hydrofluoric acid release solution is used to remove the sacrificial oxide, leaving a free-standing resonator beam on the silicon substrate.

- Fabrication steps compatible with planar IC processing

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Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

The micrograph shows a single-chip Ckt/MEMS integration with various components labeled: Sustaining Amplifier, Input, Output Transducer, Shuttle, Folded-Beam Suspension, Anchors, and Wires. An inset shows an oscilloscope output waveform. The chip size is indicated as 300 μm.

- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

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Usable MEMS-Last Integration

- **Problem:** tungsten is not an accepted primary interconnect metal
- **Challenge:** retain conventional metallization
 - ↳ minimize post-CMOS processing temperatures
 - ↳ explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al, MEMS'99])
 - ↳ Limited set of usable structural materials → not the best situation, but workable

The diagram shows a cross-section of Usable MEMS-Last Integration. It features a silicon substrate with a p-well, a thermal oxide layer, and a circuit metal interconnect. A release etch barrier (e.g., PECVD nitride) is used to protect the circuit metal. A mechanics interconnect (e.g., polysilicon, nickel, etc.) is used to connect the circuit metal to a micromechanical resonator (e.g., polysilicon, nickel, etc.).

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Poly-SiGe MICS Process

- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
 - ↳ enabled by lower deposition temperature of SiGe ~450°C
 - ↳ Adv.: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

The diagram illustrates the Poly-SiGe MICS Process. It shows a 5-level metal foundry CMOS structure with a shielded interconnect to drive electrode and a shielded vertical signal path to gate of input transistor. The Poly-SiGe MEMS structure is integrated on top of the CMOS.

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Polysilicon Germanium

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- Deposition
 - ↳ LPCVD thermal decomposition of GeH_4 and SiH_4 or Si_2H_6
 - ↳ Rate $>50 \text{ \AA}/\text{min}$, $T < 475^\circ\text{C}$, $P = 300\text{-}600 \text{ mT}$
 - ↳ At higher [Ge]: rate \uparrow , $T \downarrow$
 - ↳ In-situ doping, ion implantation
- Dry Etching
 - ↳ Similar to poly-Si, use F, Cl, and Br^- containing plasmas
 - ↳ Rate $\sim 0.4 \mu\text{m}/\text{min}$
- Wet Etching
 - ↳ H_2O_2 @ 90°C : can get 4 orders of magnitude selectivity between $>80\%$ and $<60\%$ Ge content
 - ↳ Good release etchant

The top graph plots Deposition Rate (Å/min) on a log scale from 1 to 1000 against Ge Content (0 to 100) and Temperature (700 to 300 °C). It shows two regions: POLY-CRYSTALLINE and AMORPHOUS. The bottom graph plots Etch rate (Å/min) on a log scale from 0.001 to 10000 against Ge Content (0 to 100) for RCA-SC-1 (75°C) and Hydrogen peroxide (90°C).

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Poly-SiGe Mechanical Properties

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- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus $\sim 146 \text{ GPa}$ (for poly- $\text{Si}_{0.35}\text{Ge}_{0.65}$)
- Density $\sim 4280 \text{ kg/m}^3$
- Acoustic velocity $\sim 5840 \text{ m/s}$ (25% lower than polysilicon)
 - ↳ Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- $Q=30,000$ for n-type poly-Ge in vacuum

The SEM image shows a cross-section of a poly-SiGe layer. The stress-strain plot shows stress (MPa) from -800 to 800 on the x-axis and strain from -110 to +670 on the y-axis. Data points are provided for Krulvitch: poly-Si, Franke: 100% Ge, Franke: 79% Ge, Franke: 58% Ge, Franke: 41% Ge, and Franke: 26% Ge.

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UCB Poly-SiGe MICS Process

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- $2 \mu\text{m}$ standard CMOS process w/ Al metallization
- P-type poly- $\text{Si}_{0.35}\text{Ge}_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
 - ↳ Passivate CMOS w/ LTO @ 400°C
 - ↳ Open vias to interconnect runners
 - ↳ Deposit & pattern ground plane
 - ↳ RTA anneal to lower resistivity (550°C , 30s)

The diagram shows a cross-section of the process with layers: p+ Poly-SiGe, n+ Poly-Si, Al, SiO2, SiO2, SiO2, and N Substrate with P Well. A micrograph shows the resulting Transistor Circuits.

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ASIMPS Ckt/MEMS Integration Process

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- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF_3/O_2 oxide etch
- Structures released via a final SF_6 isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
 - ↳ Must design defensively against warping

The diagrams show the integration process with layers: metal-3, metal-2, metal-1, moveable microstructure, and anchored stator. A micrograph shows the Metal/insulator stack.

[G. Fedder, CMU]
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ASIMPS Ckt/MEMS Integration Process

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

[G. Fedder, CMU]

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Finite Op Amp Gain and Bandwidth

- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_0}{1 + \frac{s}{\omega_b}}$
 - ← Finite Gain
 - ← Finite Bandwidth
- For $\omega \gg \omega_b$: $A(s) \approx \frac{A_0}{(s/\omega_b)} = \frac{A_0\omega_b}{s} = \frac{\omega_T}{s}$
 - Integrator w/ time const. $1/\omega_T$

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Op Amp Non-Idealities

Op Amp Non-Idealities → R_i & R_o

Input resistance R_i and Output Resistance R_o :

With finite R_i and R_o , and finite gain and BW, the op amp equivalent circuit becomes:

⇒ Basically reduces down to a voltage-amplifier model

⇒ Add an output CO to model a single pole response, where

$$\omega_b = \frac{1}{R_o C_o}$$

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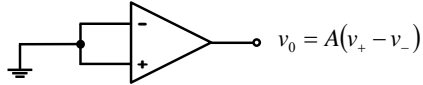
Back to Op Amp Non-Idealities

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Input Offset Voltage V_{OS}

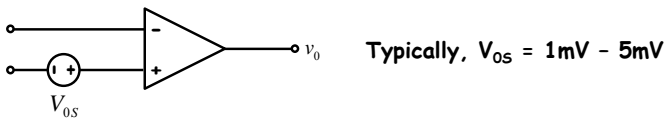
Input Offset Voltage, V_{OS} :



$v_o = A(v_+ - v_-)$

Ideal case: $v_o = 0$
Reality: $v_o \neq 0$ (usually, $v_o = L^+$ or L^- : it rails out!)

Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage V_{OS} .



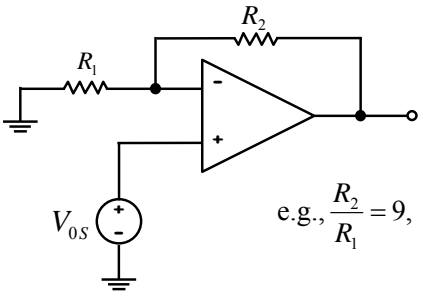
Typically, $V_{OS} = 1\text{mV} - 5\text{mV}$

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Effect of V_{OS} on Op Amp Circuits

Example: Non-Inverting Amplifier



$$v_o = V_{OS} \left(1 + \frac{R_2}{R_1} \right)$$

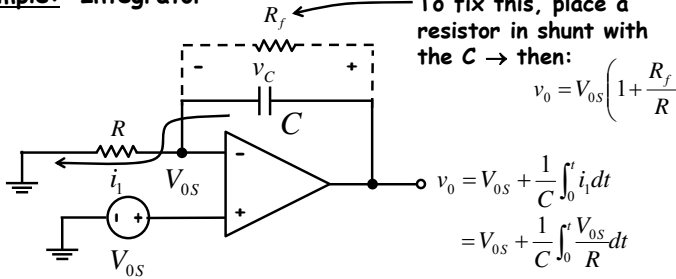
e.g., $\frac{R_2}{R_1} = 9$, $V_{OS} = 5\text{mV} \rightarrow v_o = 50\text{mV}$
 (not so bad ...)

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Effect of V_{OS} on Op Amp Circuits (cont.)

Example: Integrator



To fix this, place a resistor R_f in shunt with the $C \rightarrow$ then:

$$v_o = V_{OS} \left(1 + \frac{R_f}{R} \right)$$

$$v_o = V_{OS} + \frac{1}{C} \int_0^t i_1 dt$$

$$= V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt$$

$$= V_{OS} \left(1 + \frac{t}{RC} \right) + v_C|_{t=0}$$

Will continue to increase until op amp saturates

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