## Lecture 6: Process Modules & Surface Micromachining I

- Announcements:
- We will go 2 hours today
- HW#1 due tomorrow morning
- Lecture Modules 3 & 4 on Process Modules online
- Lecture Module 5 on Surface Micromachining online
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- Today:
- Senturia, Chpt. 3; Jaeger, Chpt. 2, 3, 6
  - ↳ Example MEMS fabrication processes
  - ↳ Photolithography
  - ↳ Etching
  - ↳ Oxidation
  - ↳ Film Deposition
  - ↳ Ion Implantation
  - ↳ Diffusion
- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: "Surface Micromachining for Microelectromechanical Systems"
- Lecture Topics:
  - ↳ Polysilicon surface micromachining
  - ↳ Stiction
  - ↳ Residual stress
  - ↳ Topography issues
  - ↳ Nickel metal surface micromachining
  - ↳ 3D "pop-up" MEMS
  - ↳ Foundry MEMS: the "MUMPS" process
  - ↳ The Sandia SUMMIT process
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- Last Time: started process modules

## Process Module Overview:

- Lecture Topics:
  - ↳ Photolithography
  - ↳ Etching
  - ↳ Oxidation
  - ↳ Film Deposition
  - ↳ Ion Implantation
  - ↳ Diffusion
- As stated earlier, this is now assumed knowledge
- I will gloss over this material to review it a bit, but will not go over it in detail
- You can watch my lectures from EE245, Spring 2012, on the Webcast Berkeley site for more in depth coverage: Lectures 6-8
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**Process Modules**

⇒ there are actually only a few basic modules used for processing

↓

Combination of these in the correct sequence yields an integrated circuit technology that provides transistors, MEMS, nanodevices, etc.

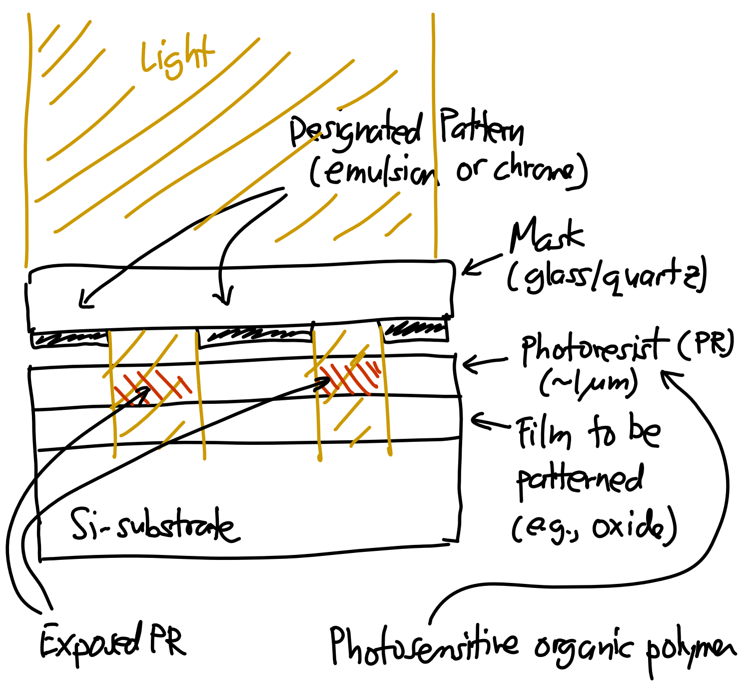
⇒ For each module, need to understand:

① Physics and engineering of each module in detail.

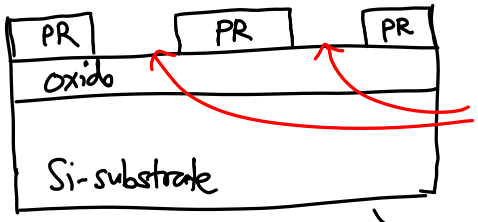
② Interactions between modules.

③ The effect of each module on the finished device.

## Photolithography



↓ Add developer (KOH)



Case: Positive Resist

exposed positive resist removes in developer

⇒ Now, the PR is patterned

⇒ Ready for the next step: Etching

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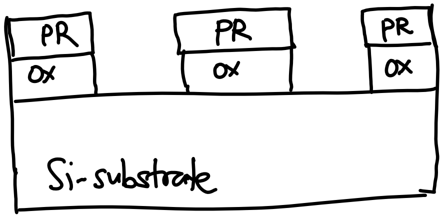
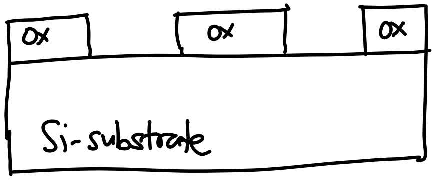
↓ Etch oxide (using dry or wet etchant)



⇒ PR protects underlying oxide from etching

↓ Acetone or PRS 3000 (to remove the PR)



oxide film now patterned

⇒ Above: collectively called a masking step

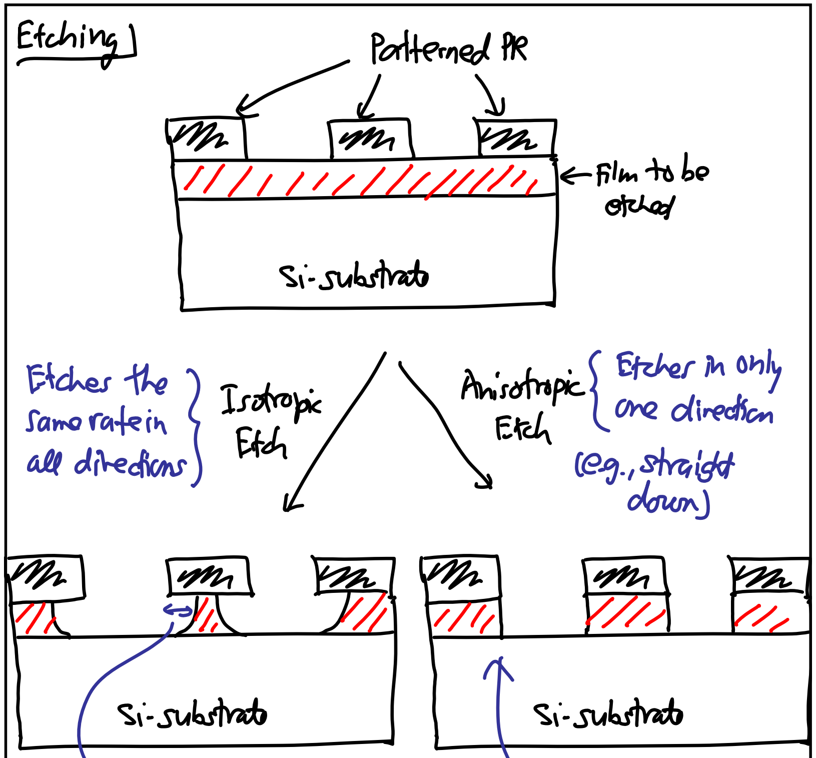
Usually gauge the cost & complexity of a given technology by the # masking steps!

Number of Masking Steps

NMOS: 4-6 masks
1990 CMOS: 8–11 masks
today's CMOS: >28 masks
Bipolar: 11–13 masks
BiCMOS: 20 masks

Combination of bipolar & CMOS (mainly for RF/wireless apps.)

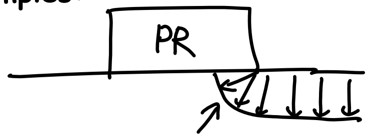
## Etching



undercutting → not desirable when resolution is important → very desirable in MEMS, when a structure must be released

no undercutting → best resolution!

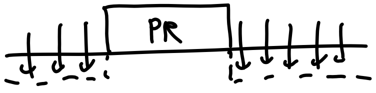
- Isotropic Etchant Examples:
  - ↳ Wet etchants
  - ↳ Dry plasma etch



get undercut & curved profile

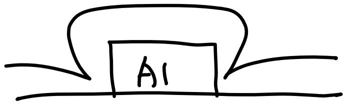
- Anistropic Etchant Examples:
  - ↳ Reactive ion etch
  - ↳ Ion milling

} Use ions under E-fields to give the etch more directionality.

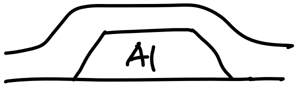


square profile & no undercut

- **Remarks**:
  - ↳ Wet etching is fairly cheap
  - ↳ Dry etching requires a plasma, so requires some expensive equipment
  - ↳ Don't always want straight sidewalls

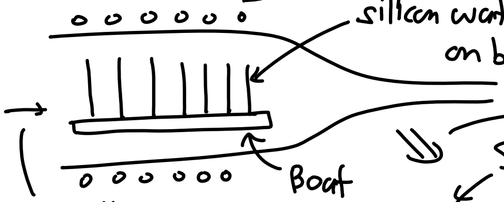


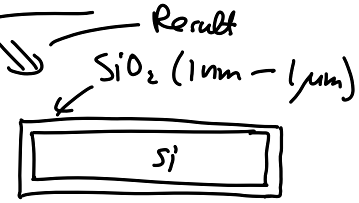
Too much topography → more difficult for subsequent films to conform



Sloped sidewalls allow better conformability

### Silicon Oxidation



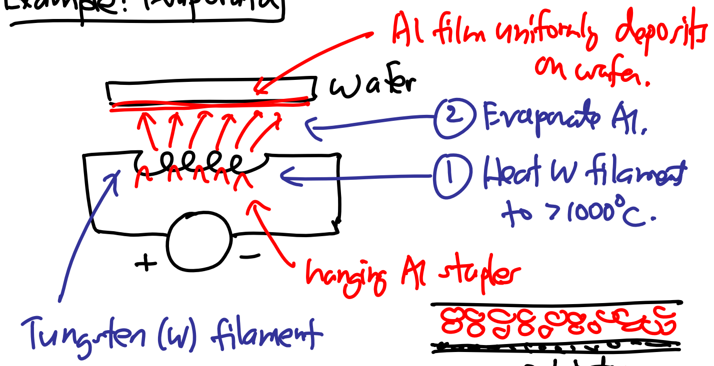


- **Remarks**:
  - Uniformity can be better than 2% across the wafer from lot to lot
  - Need to flow the $O_2$ fairly fast in order to minimize reactant losses from the first boat to the last one

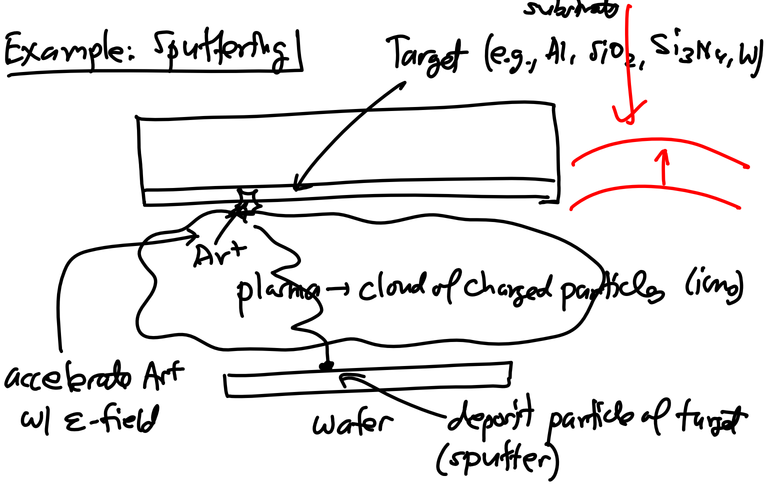
**Thin-Film Deposition**:

- For deposition of films like Al (and other metals), $SiO_2$, $Si_3N_4$, and polysilicon
- Deposition, not thermal growth

Example: Evaporation

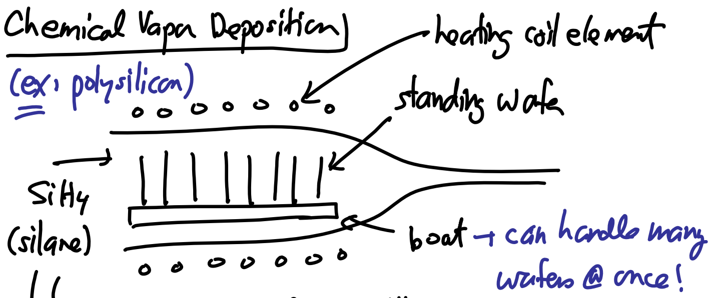


Example: Sputtering



- Also, have chemical vapor deposition (CVD)
  - Chemical reaction involved in deposition of a given thin film
  - High temperature, but not nearly as high as often required for thermal growth

Chemical Vapor Deposition (ex: polysilicon)



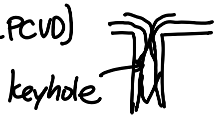
585°C – 600°C for polysilicon

chemically decomposes to deposit poly Si

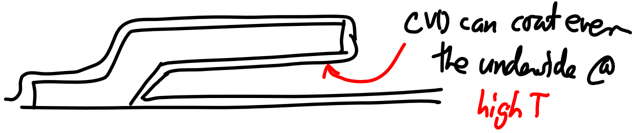
$$SiH_4 \xrightarrow{600°C} Si + 2H_2$$

600°C ← fairly high T

25-150 Pa ← low pressure (LPCVD)

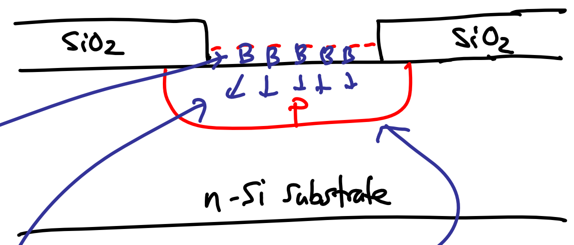


- **Remarks**:
  - Lot's of materials can be deposited in a similar manner: polysilicon, $SiO_2$, $Si_3N_4$, tungsten
  - Compared to sputtering, CVD is less expensive since one can coat many wafers at once; sputtering generally does it one at a time
  - For higher temperature, CVD films are much more conformal than sputtered films



- **Diffusion**:
- Process of introducing dopants into selected areas on an IC
- **Example**:

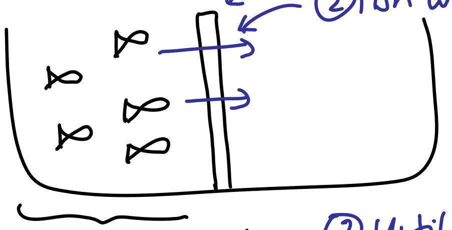
diborane gas → $B_2H_6 + O_2$ @ high temperature ~800°C — 1200°C



① Form borosilicate glass w/ high B concentration
② Boron diffuses in → this becomes p-type

⇒ diffusion requires:
① concentration gradient
② movement (velocity)

→ Example. Fish Tank



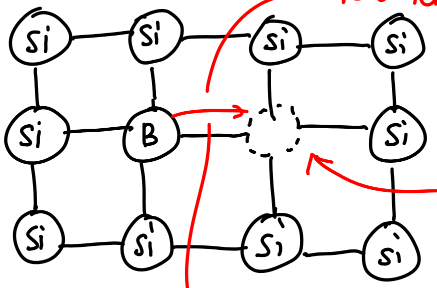
① When separator removed...
② Fish will go to the other side

highly concentrated

③ Until the concentration is the same on both sides

But they can't if they're dead!

It's similar for an impurity in silicon:



need temperature for this to happen

Need high T for this vacancy to exist.

Just one mechanism for diffusion → we'll look at others, too

Substitutional diffusion:
⇒ impurity moves along vacancies in the lattice
⇒ substitutes for a Si atom in the lattice

For movement to occur:
① Vacancies must exist.
② The B must have enough energy to move.

Both require high temperature!

→ must heat to induce diffusion of impurities in Si!

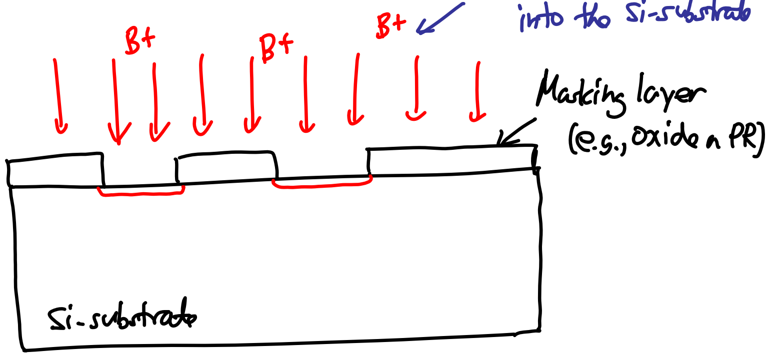
Definitions.

① Predeposition: diffusion w/ dopant source present
② Drive-in: diffusion in an inert ambient, e.g., $N_2$ w/ no dopant gases present

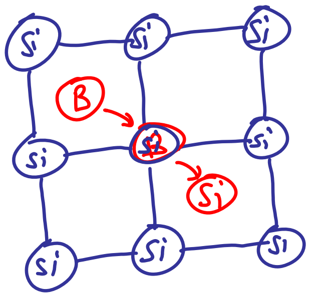
## Ion Implantation

⇒ a more accurate way to introduce dopants before drive-in

① Accelerate $B^+$ ions into the Si-substrate



② $B^+$ punches into the Si



③ Raise T to move the B into the lattice → only when it's in the lattice is it active & can contribute to the doping level

④ Keep T up to drive the dopants in to the desired depth.

**Advantages:**

① accurate dose
② change depth by setting ion energy
③ no need for high temperature

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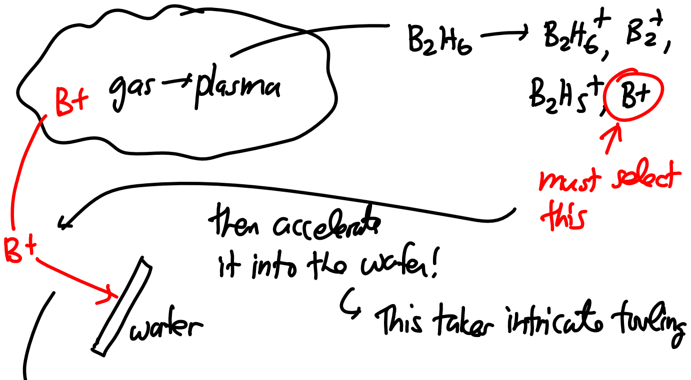
**Problem:** COST!

An ion implanter is quite a sophisticated piece of equipment! → and expensive! (> $1 million)



↳ This takes intricate tooling.

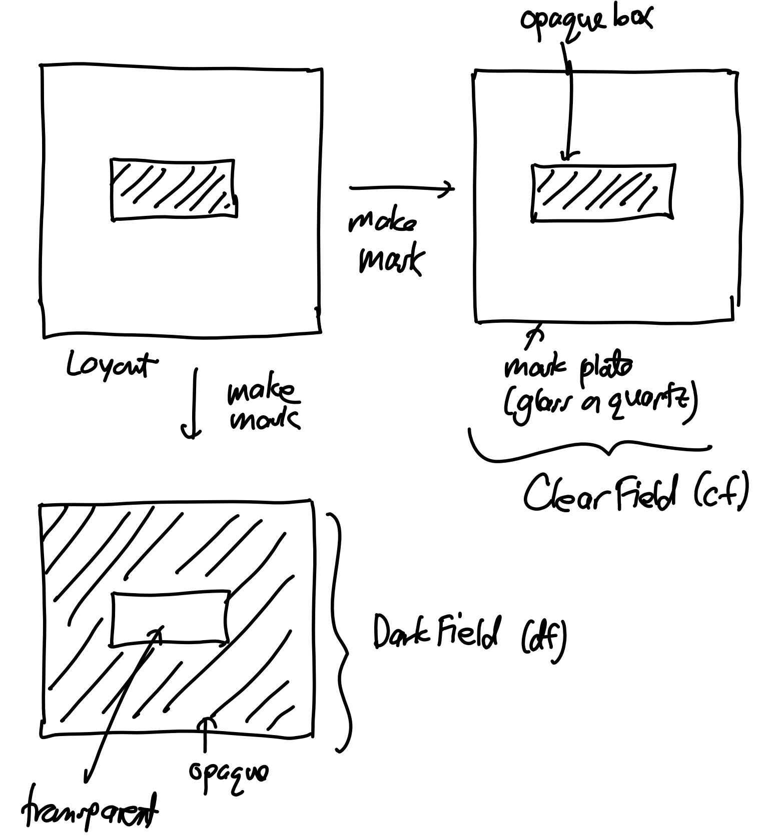
**Energy Range:** 20keV – 100keV

**Penetration Depth:** fraction of a μm

⇒ larger ions don't go as far as smaller (heavier ions penetrate shallower than smaller)

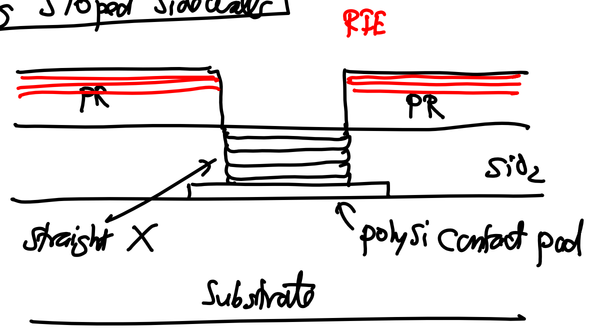
**Dose:** $10^{11}-10^{15}\ cm^{-2}$

## Clear Field & Dark Field Masks

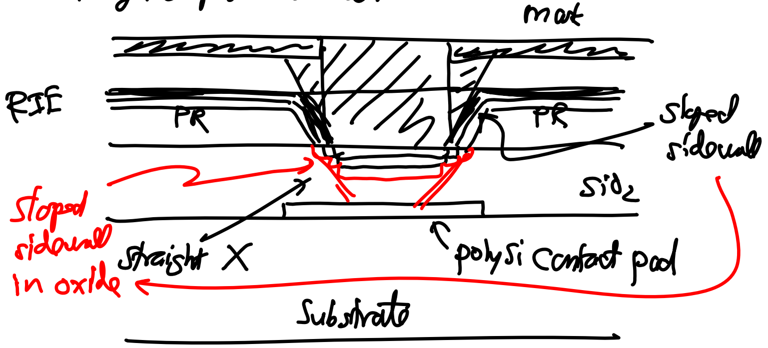


- **Straight or Sloped Sidewalls**:
- Often want sloped sidewalls in order to reduce the sharpness of corners
  - ↳ Easier to deposit over
  - ↳ Sharp corners concentrate stresses
  - ↳ High stress can weaken structures creating a reliabilty concern
  - ↳ High stress can dissipate energy, lowering Q
- When you want straight sidewalls (e.g., for lateral electrostatic drive), use a hard mask
  - ↳ PR can't last for thick structures
  - ↳ A hard mask suppresses angle transfer

## Etching Sloped Sidewalls



→ to get sloped sidewall:



What if we want straight sidewalls when the PR sidewalls are not straight?

RIE w/ $S^{polySi}_{ox}$ = large