PROBLEM SET #2

Issued: Tuesday, Feb. 9, 2016

Due: Friday, Feb. 19, 2016, 8:00 a.m. in the EE C247B homework box near 125 Cory.

This assignment is meant to insure that you have sufficient quantitative fabrication process module understanding to design or analyze a MEMS fabrication process flow. As mentioned in lecture, some of the details needed to do some of the problems herein were not explicitly covered in regular lecture, but are covered in Lecture modules 3 and 4, and in the recorded video lectures of past semesters that you can watch online. (You were given the whereabouts of these videos in class.)

Throughout this assignment following abbreviations are used:

NAME	ABB.	NAME	ABB.
Silicon	Si	Hydrofluoric Acid	HF
Silicon Dioxide	SiO_2	Photoresist	PR
Silicon Nitride	Si ₃ N ₄	Deep Ultraviolet	DUV
Poly-Crystalline Diamond	Polydiamond	Numerical Aperture	NA
Phosphosilicate Glass	PSG	Reactive Ion Etching	
Polysilicon	PolySi	Deep Reactive Ion Etching	DRIE

Table PS2

- 1. Consider the cross-section shown in Fig. PS2.1-1 of a polydiamond beam with angled sidewalls upon which a conformal SiO₂ film was deposited. The wafer will be placed into an RIE chamber. Assume that chemicals inside the chamber will etch the structure at the rates listed in Table PS2.1-1. Carefully draw cross-sections of the structure after
 - (a) 10 minutes of etching.
 - (**b**) 60 minutes of etching.

Note that it is only necessary to draw half of the structure due to symmetry. Please specify all angles and dimensions for each cross-section. Round all dimensions to the nearest 10nm.

MATERIAL	VERTICAL	LATERAL	UNIT
SiO ₂	50	10	nm/min
Polydiamond	10	0	nm/min
Si ₃ N ₄	30	0	nm/min
Si	100	0	nm/min

Table PS2.1-1





2. Consider a silicon wafer covered with an arbitrary thick film of PSG that has a phosphorous concentration much greater than the solid solubility limit of phosphorous in silicon. The wafer has an initial background dopant concentration of $N_A = 2x10^{15}$ cm⁻³. The wafer is to be placed in an annealing furnace and heated for one hour according to the temperature function given in Fig. PS2.2-1.



Fig. PS2.2-1

Recall that the diffusivity of a dopant atom in a material follows an Arrhenius dependence on temperature and is given by

$$D(T) = D_0 e^{\frac{-E_A}{k_B T}} \tag{1}$$

where D_0 is a constant in cm²/s, E_A is the activation energy in J, k_B is Boltzmann's constant, and T is the absolute temperature. Refer to Jaeger page 74 for the appropriate values of D_0 and E_A .

- (a) Find the value of T_{max} that gives a junction depth of 800nm. Recall that the junction depth is the depth at which $N_A = N_D$. You are advised to use a numerical program such as MATLAB or Mathematica to solve this problem. Refer to Jaeger page 75 for the solid solubility limit of phosphorous in silicon.
- (b) Calculate the sheet resistance due to the dopant profile calculated in part (a). Refer to Jaeger page 75 for the electrically active impurity concentration limit of phosphorous in silicon. Use the following expression for the mobility of electrons in silicon given in cm²/Vs [C. Hu, Modern Semiconductor Devices for Integrated Circuits. Prentice Hall: Upper Saddle River, NJ, 2010]:

$$\mu_n(x) = \frac{1318}{1 + \left[\frac{N_A + N_D(x)}{10^{17}}\right]^{0.85}} + 92$$
(2)

(c) Assuming a sheet resistance of $100\Omega/\Box$, what is the resistance between A and B shown in Fig. PS2.2-2. Do not spend too much time on this problem, an accuracy of $\pm 20\%$ is fine.



Fig. PS2.2-2

- **3.** You are given a wafer with the cross-section shown in Fig. PS2.3-1 and intend to release etch the structure, i.e. to leave only polysilicon structure atop the blanket SiO_2/Si_3N_4 layer. To perform the release, you need to do the following steps:
 - i. Etch polysilicon via RIE and stop on the sacrificial oxide layer.
 - ii. Remove PR.
 - iii. Dip the wafer in HF to etch the sacrificial oxide layer until polysilicon structures are fully released. Assume this etch is completely isotropic.

Assume that RIE etches are perfectly anisotropic and wet etches are perfectly isotropic.

Due to topography across the wafer, a given layer thickness might not be the same over the entire wafer. So when you etch a given layer, you must etch a bit longer than what you calculated from knowledge of thickness and etch rate to make sure all material is removed from unmasked areas. It is common practice to etch at least 20% longer than the calculated time, i.e. do a 20% overetch. Include this overetch in your calculations for this problem.



Fig. PS2.3-1

PARAMETER	PolySi RIE	PolySi DRIE	SiO2 WET ETCH	SiO ₂ DRY ETCH	UNIT
Etch Rate	0.5	1.5	0.3	0.3	µm/min
Selectivity Over PolySi	N/A	N/A	100:1	14:1	-
Selectivity Over Si ₃ N ₄	10:1	-	20:1	-	-
Selectivity Over SiO ₂	5:1	100:1	N/A	N/A	-
Selectivity Over PR	2:1	50:1	5:1	4:1	-

Table PS2.3-1

- (a) What is total etch time (including 20% overetch) to remove all the unprotected polysilicon? Draw the wafer cross-section immediately after step (i) using this etch time. Assume the RIE etch is completely anisotropic.
- (b) Suppose a 1µm SiO₂ hard mask layer is deposited atop the polysilicon film before PR deposition and patterning as shown in Fig. PS2.3-2. First dry etch the SiO₂ layer in RIE system, then follow with another RIE etch to define the polysilicon structure using the patterned SiO₂ layer as a hard mask. How long should the SiO₂ layer be dry etched (including a 20% overetch)? Draw the wafer cross-sections immediately after the SiO₂ etch step and after the polysilicon etch step. So that you are not affected by your part (a) result, assume an 8-minute polysilicon etch after etching the SiO₂ hard mask.



Fig. PS2.3-2

(c) After the polysilicon etch step in part (b), the structure is released in HF as indicated in step (iii) of the process flow. How long does it take to completely release the structure? Draw the wafer cross-section immediately after the release step. Assume the wet etch is completely isotropic.



Fig. PS2.3-3

(d) Assume now the sacrificial SiO₂ layer thickness is reduced to 50nm as shown in Fig. PS2.3-3. To avoid etching through the sacrificial SiO₂ to the polysilicon underneath, the high-selectivity BOSCH DRIE process is employed. What is total etch time (including 20%)

overetch) to completely remove the polysilicon layer? Is 50nm SiO₂ thick enough to protect the polysilicon below? How long does it take to completely release the structure?

- (e) What are the drawbacks of the BOSCH DRIE process?
- (f) For some micromechanical devices interconnect resistance degrades performance considerably. One way to mitigate this problem is to deposit a thick layer of interconnect polysilicon, i.e. $3\mu m$, which reduces the resistance. However, a thick interconnect layer introduces topography, even more so than seen in part (a).

Suppose you want to fabricate the micromechanical structure in part (a) with a 3μ m-thick interconnect layer. Suppose also that a chemical mechanical polishing (CMP) tool is now available. Design a process flow for this structure that avoids topography problems.