

Deep Reactive-Ion Etching (DRIE)

The Bosch process:

- Inductively-coupled plasma
- Etch Rate: 1.5-4 $\mu\text{m}/\text{min}$
- Two main cycles in the etch:
 - Etch cycle** (5-15 s): SF_6 (SF_x^+) etches Si
 - Deposition cycle**: (5-15 s): C_4F_8 deposits fluorocarbon protective polymer (CF_2^-)_n
- Etch mask selectivity:
 - $\text{SiO}_2 \sim 200:1$
 - Photoresist $\sim 100:1$
- Issue**: finite sidewall roughness
 - scalloping < 50 nm
- Sidewall angle: $90^\circ \pm 2^\circ$

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DRIE Issues: Etch Rate Variance

- Etch rate is diffusion-limited and drops for narrow trenches
 - Adjust mask layout to eliminate large disparities
 - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

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DRIE Issues: "Footing"

- Etch depth precision
 - Etch stop: buried layer of SiO_2
 - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- Problem**: Lateral undercut at Si/ SiO_2 interface \rightarrow "footing"
 - Caused by charge accumulation at the insulator

Charging-induced potential perturbs the E-field
 \rightarrow Distorts the ion trajectory
 \rightarrow Result: strong and localized damage to the structure at Si- SiO_2 interface \rightarrow "footing"

Poor charge relaxation and lack of neutralization by e⁻s at insulator
 \rightarrow Ion flux into substrate builds up (+) potential

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Recipe-Based Suppression of "Footing"

- Use **higher process pressure** to reduce ion charging [Nozawa]
 - High operating pressure \rightarrow concentration of (-) charge increases and can neutralize (+) surface charge
 - Issue**: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe** to reduce overetching [Schmidt]
 - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
 - Issue**: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
 - Low frequency \rightarrow more ions with low directionality and kinetic energy \rightarrow neutralizes (-) potential barrier at trench entrance
 - Allows e⁻s to reach the trench base and neutralize (+) charge \rightarrow maintain charge balance inside the trench

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Metal Interlayer to Prevent "Footing"

Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial) (f) Silicon Thinning
(b) Preparatory trenches (g) Photolithography 2
(c) Metal interlayer deposition (h) DRIE
(d) Lift-off (remove PR) (i) Remove metal interlayer
(e) Anodic Bonding (i) Metallize

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Footing Prevention (cont.)

- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach [Kim, Stanford]

Local damages
Pre trench (cavity)
Footing
No footing
Damage free!
With metal interlayer

[Kim, Stanford]
[Kim, Seoul Nat. Univ.]

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DRIE Examples

High aspect-ratio gear
Tunable Capacitor [Yao, Rockwell]

Microgripper [Keller, MEMS Precision Instruments]

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Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride (XeF_2)
 $2\text{XeF}_{2(g)} + \text{Si}_{(s)} \rightarrow 2\text{Xe}_{(g)} + \text{SiF}_{4(g)}$
- Set-up:
 - Xe sublimates at room T
 - Closed chamber, 1-4 Torr
 - Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 $\mu\text{m}/\text{min}$, isotropic
- Etch masks: photoresist, SiO_2 , Si_3N_4 , Al, other metals
- Issues:
 - Etched surfaces have granular structure, 10 μm roughness
 - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

Xactix XeF_2 Etcher

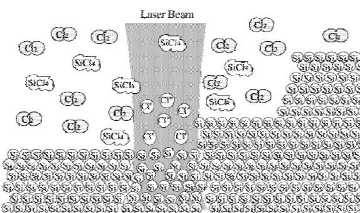
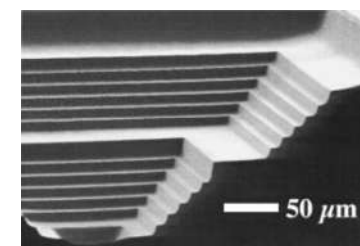
Inductor w/ no substrate [Pister]

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Laser-Assisted Chemical Etching

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- Laser creates Cl radicals from $\text{Cl}_2 \rightarrow$ reaction forms SiCl_2
- Ech rate: $100,000 \mu\text{m}^3/\text{s}$
 - Takes 3 min. to etch $500 \times 500 \times 125 \mu\text{m}^3$ trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file

- At right:**
 - Laser assisted etching of a $500 \times 500 \mu\text{m}^2$ terraced silicon well
 - Each step is $6 \mu\text{m}$ -deep

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Wafer Bonding

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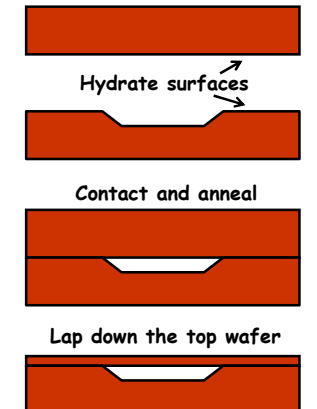
Wafer Bonding

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Fusion Bonding

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- Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces
- Procedure:**
 - Prepare surfaces: must be smooth and particle-free
 - Clean & hydrate: O_2 plasma, hydration, or HF dip
 - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
 - Anneal at $600\text{-}1200^\circ\text{C}$ to bring the bond to full strength
- Result:** a bond as strong as the silicon itself!



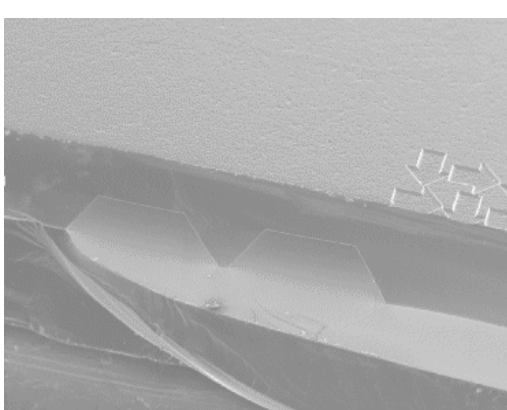
Works for Si-to-Si bonding and Si-to-SiO₂ bonding

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Fusion Bonding Example

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- Below:** capacitive pressure sensor w/ fusion-bonded features



[Univ. of Southampton]

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Anodic Bonding

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- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
 - Press Si and glass together
 - Elevate temperature: 180-500°C
 - Apply (+) voltage to Si: 200-1500V
 - (+) voltage repels Na⁺ ions from the glass surface
 - Get net (-) charge at glass surface
 - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
- Current drops to zero when bonding is complete

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Anodic Bonding (cont.)

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- Advantage:** high pressure of electrostatic attraction smooths out defects
- Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N₂ @ 1000 mbar

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Metal Layer Bonding

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- Pattern seal rings and bond pads photolithographically
- Eutectic bonding**
 - Uses eutectic point in metal-Si phase diagrams to form silicides
 - Au and Si have eutectic point at 363°C
 - Low temperature process
 - Can bond slightly rough surfaces
 - Issue:** Au contamination of CMOS
- Solder bonding**
 - PbSn (183°C), AuSn (280°C)
 - Lower-T process
 - Can bond very rough surfaces
 - Issue:** outgassing (not good for encapsulation)
- Thermocompression**
 - Commonly done with electroplated Au or other soft metals
 - Room temperature to 300°C
 - Lowest-T process
 - Can bond rough surfaces with topography

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Thermocompression Bonding

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- Below:** Transfer of hexsil actuator onto CMOS wafer

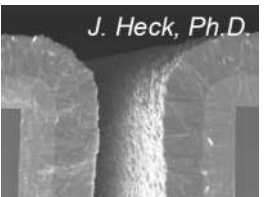
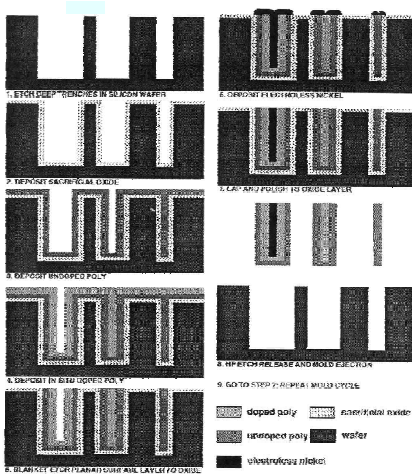
[Singh, et al, Transducers'97]

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Hexsil MEMS

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- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength

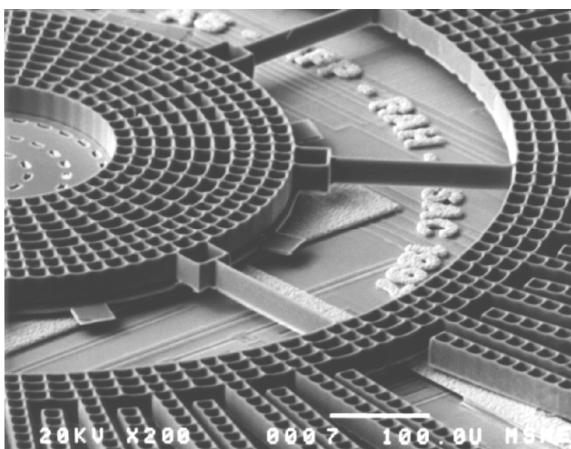



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Hexsil MEMS Actuator

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- Below:** Transfer of hexsil actuator onto CMOS wafer



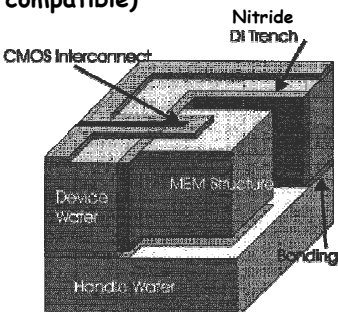
[Singh, et al, Transducers'97]

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Silicon-on-Insulator (SOI) MEMS

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- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)



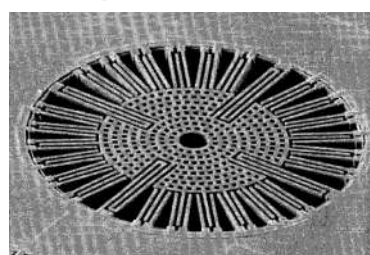
	Cross Section	Top View
Silicon		
SiO ₂		
SOI starting material		
Silicon Nitride		
Trench and Backfill		
Integrated Circuitry		
Structure definition and release		

Handwritten notes: A red box highlights 'Si' and 'Si Substrate' with an arrow pointing to the silicon layer in the cross-section. Another red arrow points to 'oxide' in the trench and backfill layer.

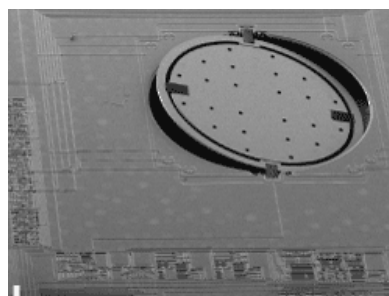
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SOI MEMS Examples

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[Brosnihan]



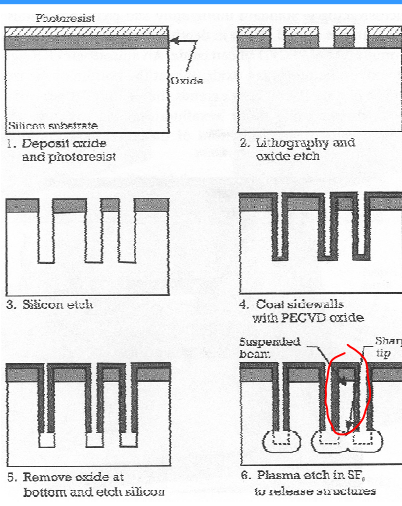
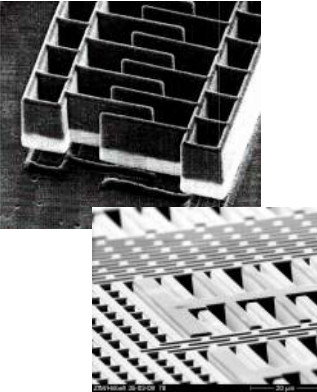
Micromirror [Analog Devices]

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The SCREAM Process

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- **SCREAM: Single Crystal Reactive Etching and Metallization process**



1. Deposit oxide and photoresist

2. Lithography and oxide etch

3. Silicon etch

4. Coat sidewalls with PECVD oxide

5. Remove oxide at bottom and etch silicon

6. Plasma etch in SF_6 to release structures

Suspended beam, Sharp tip

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