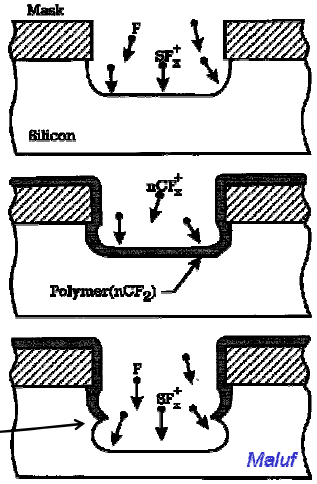
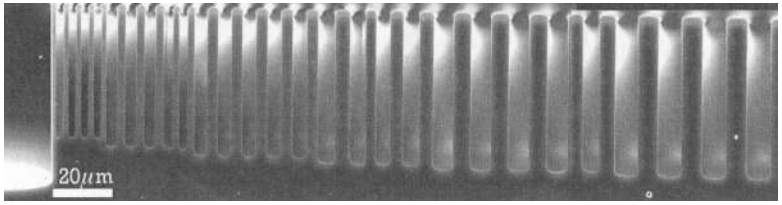
Deep Reactive-Ion Etching (DRIE)

The Bosch process:

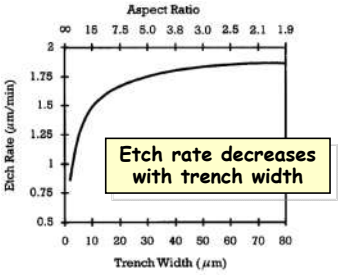
- Inductively-coupled plasma
- Etch Rate: 1.5-4 μm/min
- Two main cycles in the etch:
  - Etch cycle (5-15 s): SF_6 (SF_x^+) etches Si
  - Deposition cycle: (5-15 s): C_4F_8 deposits fluorocarbon protective polymer $(CF_2^-)_n$
- Etch mask selectivity:
  - SiO_2 ~ 200:1
  - Photoresist ~ 100:1
- Issue: finite sidewall roughness
  - scalloping < 50 nm
- Sidewall angle: 90° ± 2°



DRIE Issues: Etch Rate Variance

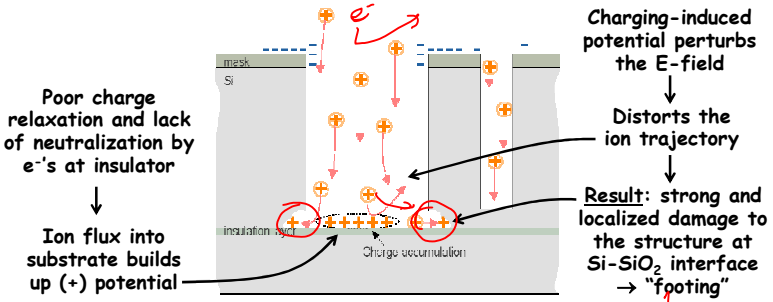


- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)



DRIE Issues: "Footing"

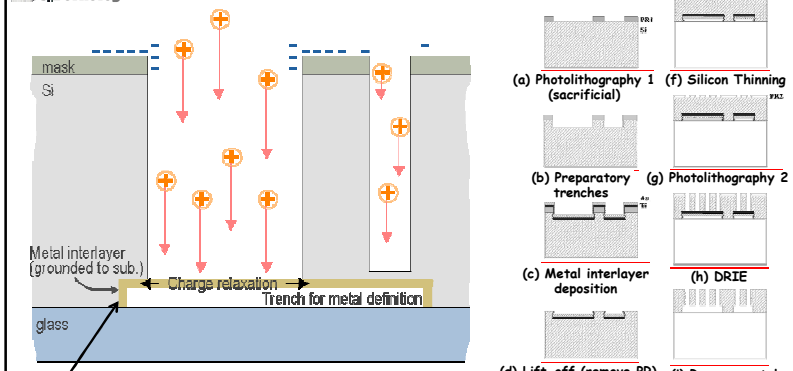
- Etch depth precision
  - Etch stop: buried layer of SiO_2
  - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- Problem: Lateral undercut at Si/SiO_2 interface → "footing"
  - Caused by charge accumulation at the insulator



Recipe-Based Suppression of "Footing"

- Use higher process pressure to reduce ion charging [Nozawa]
  - High operating pressure → concentration of (-) charge increases and can neutralize (+) surface charge
  - Issue: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe to reduce overetching [Schmidt]
  - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
  - Issue: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use lower frequency plasma to avoid surface charging [Morioka]
  - Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - Allows e⁻'s to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench

Metal Interlayer to Prevent "Footing"

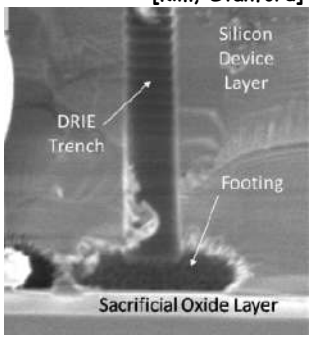


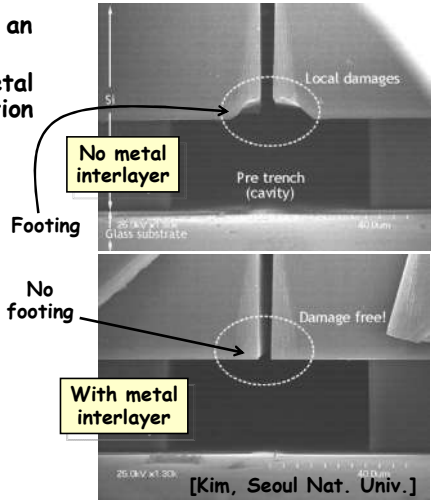
Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

Footing Prevention (cont.)

- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach

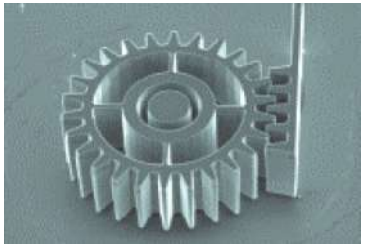
[Kim, Stanford]





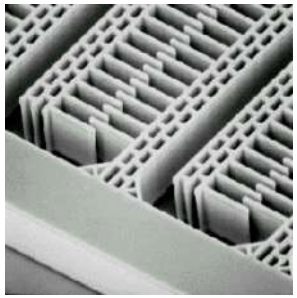
[Kim, Seoul Nat. Univ.]

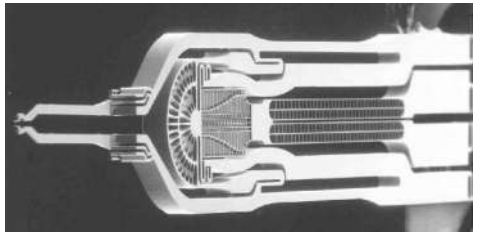
DRIE Examples



High aspect-ratio gear

Tunable Capacitor [Yao, Rockwell]



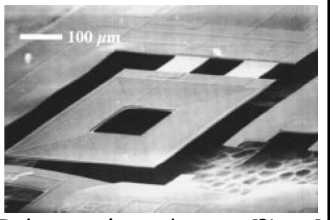


Microgripper [Keller, MEMS Precision Instruments]

Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride (XeF_2)
  $2XeF_{2(g)} + Si_{(s)} \rightarrow 2Xe_{(g)} + SiF_{4(g)}$
- Set-up:
  - Xe sublimes at room T
  - Closed chamber, 1-4 Torr
  - Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 μm/min, isotropic
- Etch masks: photoresist, SiO_2, Si_3N_4, Al, other metals
- Issues:
  - Etched surfaces have granular structure, 10 μm roughness
  - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

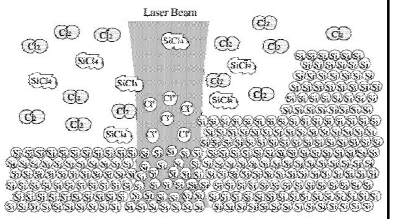
Xactix XeF_2 Etcher



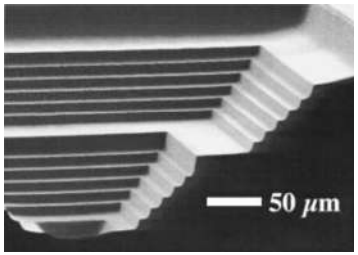
Inductor w/ no substrate [Pister]

Laser-Assisted Chemical Etching

- Laser creates Cl radicals from Cl_2 → reaction forms $SiCl_2$
- Etch rate: 100,000 μm³/s
  - Takes 3 min. to etch 500×500×125 μm³ trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file



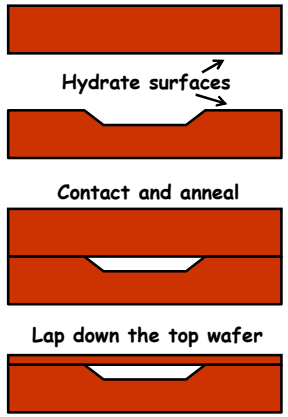
- At right:
  - Laser assisted etching of a 500x500 μm² terraced silicon well
  - Each step is 6 μm-deep



Wafer Bonding

Fusion Bonding

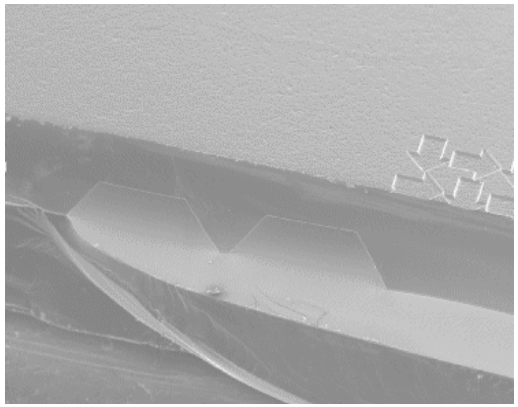
- Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces
- Procedure:
  - Prepare surfaces: must be smooth and particle-free
    - Clean & hydrate: O_2 plasma, hydration, or HF dip
  - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
  - Anneal at 600-1200°C to bring the bond to full strength
- Result: a bond as strong as the silicon itself!

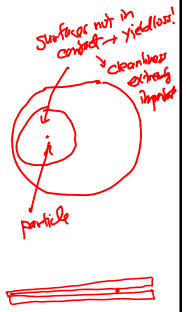


Works for Si-to-Si bonding and Si-to-SiO_2 bonding

Fusion Bonding Example

- Below: capacitive pressure sensor w/ fusion-bonded features

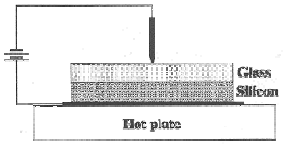


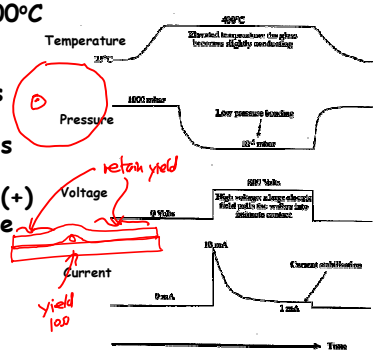


[Univ. of Southampton]

Anodic Bonding

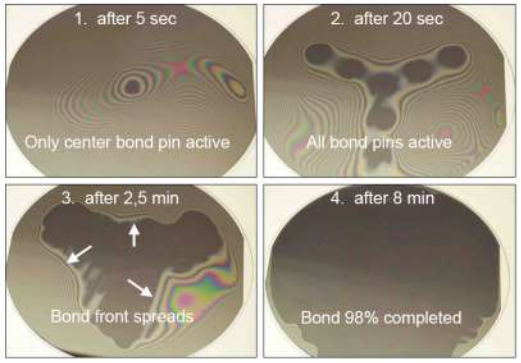
- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
  - Press Si and glass together
  - Elevate temperature: 180-500°C
  - Apply (+) voltage to Si: 200-1500V
    - (+) voltage repels Na^+ ions from the glass surface
    - Get net (-) charge at glass surface
    - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
  - Current drops to zero when bonding is complete





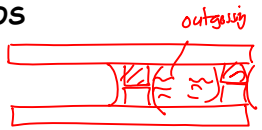
Anodic Bonding (cont.)

- Advantage: high pressure of electrostatic attraction smoothes out defects
- Below: 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N_2 @ 1000 mbar



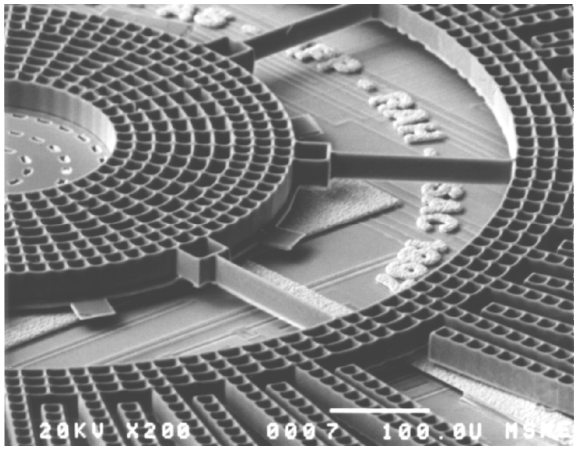
Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- Eutectic bonding
  - Uses eutectic point in metal-Si phase diagrams to form silicides
  - Au and Si have eutectic point at 363°C
  - Low temperature process
  - Can bond slightly rough surfaces
  - Issue: Au contamination of CMOS
- Solder bonding
  - PbSn (183°C), AuSn (280°C)
  - Lower-T process
  - Can bond very rough surfaces
  - Issue: outgassing (not good for encapsulation)
- Thermocompression
  - Commonly done with electroplated Au or other soft metals
  - Room temperature to 300°C
  - Lowest-T process
  - Can bond rough surfaces with topography



Thermocompression Bonding

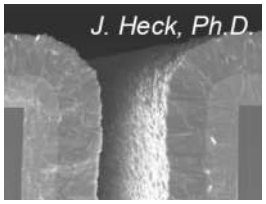
- Below: Transfer of hexsil actuator onto CMOS wafer

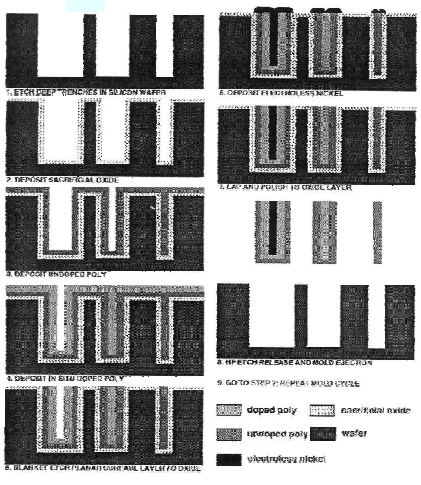


[Singh, et al, Transducers'97]

Hexsil MEMS

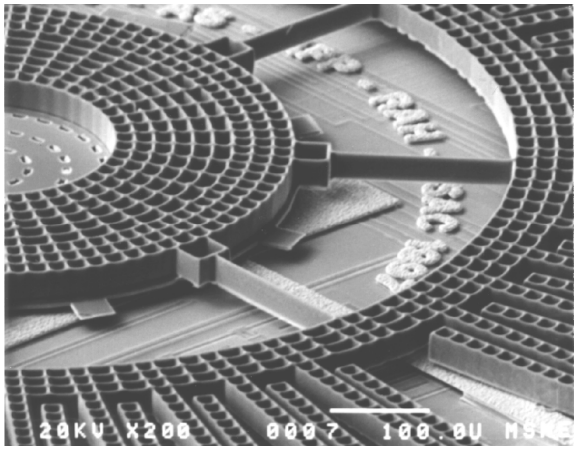
- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength





Hexsil MEMS Actuator

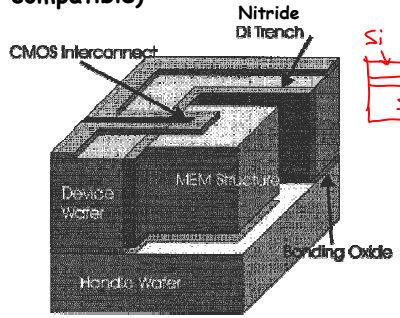
- Below: Transfer of hexsil actuator onto CMOS wafer

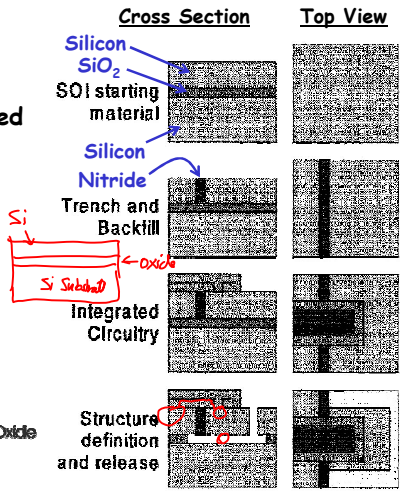


[Singh, et al, Transducers'97]

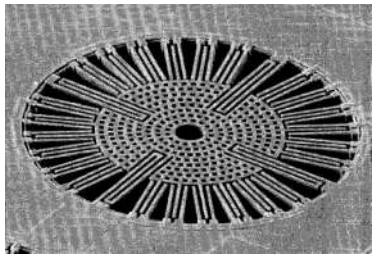
Silicon-on-Insulator (SOI) MEMS

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)



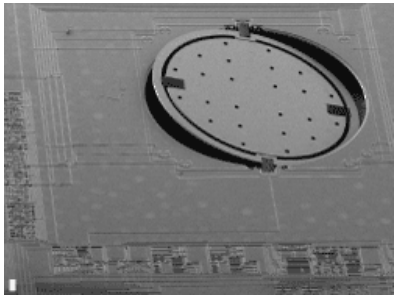


SOI MEMS Examples



[Brosnihan]

Micromirror
[Analog Devices]



The SCREAM Process

- SCREAM: Single Crystal Reactive Etching and Metallization process