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## EE C247B - ME C218 Introduction to MEMS Design Spring 2016

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Lecture Module 6: Bulk Micromachining

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## Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - ↪ Bulk Micromachining
  - ↪ Anisotropic Etching of Silicon
  - ↪ Boron-Doped Etch Stop
  - ↪ Electrochemical Etch Stop
  - ↪ Isotropic Etching of Silicon
  - ↪ Deep Reactive Ion Etching (DRIE)

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## Bulk Micromachining

- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - ↪ Isotropic vs. anisotropic
  - ↪ Reaction-limited
    - Etch rate dep. on temp.
  - ↪ Diffusion-limited
    - Etch rate dep. on mixing
    - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - ↪ Desired shape
  - ↪ Etch depth and uniformity
  - ↪ Surface roughness (e.g., sidewall roughness after etching)
  - ↪ Process compatibility (w/ existing layers)
  - ↪ Safety, cost, availability, environmental impact

	Wet etch	Plasma (dry) etch
Isotropic		
Anisotropic		

adsorption    surface reaction    desorption

*slowest step controls rate of reaction*

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## Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - ↪ Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm<sup>2</sup>)
  - ↪ Young's Modulus near that of stainless steel
  - ↪ {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - ↪ Mechanical properties uniform, no intrinsic stress
  - ↪ Mechanical integrity up to 500°C
  - ↪ Good thermal conductor
  - ↪ Low thermal expansion coefficient
  - ↪ High piezoresistivity

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### Anisotropic Etching of Silicon

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- Etching of Si w/ KOH
 
$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
- Crystal orientation dependent etch rates
  - {110}:{100}:{111}=600:400:1
  - {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
  - {111} plane has three of its bonds below the surface & only one dangling bond to react  $\rightarrow$  much slower E.R.
  - {111} forms protective oxide
  - {111} smoother than other crystal planes  $\rightarrow$  good for optical MEMS (mirrors)

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### Anisotropic Etching of Silicon

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- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - RIE using  $\text{SF}_6$
  - Remove PR in PRS2000
- Etch the silicon
  - Use 1:2 KOH:H<sub>2</sub>O (wt.), stirred bath @ 80°C
  - Etch Rates:
    - (100) Si  $\rightarrow$  1.4  $\mu\text{m}/\text{min}$
    - Si<sub>3</sub>N<sub>4</sub>  $\rightarrow$  ~ 0 nm/min
    - SiO<sub>2</sub>  $\rightarrow$  1-10 nm/min
    - Photoresist, Al  $\rightarrow$  fast
- Micromasking by H<sub>2</sub> bubbles leads to roughness
  - Stir well to displace bubbles
  - Can also use oxidizer for (111) surfaces
  - Or surfactant additives to suppress bubble formation

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### Silicon Wafers

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### Silicon Crystallography

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**Miller Indices (h k l):**

- Planes
  - Reciprocal of plane intercepts with axes
  - e.g., for (110), intercepts: (x,y,z) = (1,1, $\infty$ ); reciprocals: (1,1,0)  $\rightarrow$  (110)
  - (unique), {family}
- Directions
  - One endpoint of vector @ origin
  - [unique], <family>

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### Determining Angles Between Planes

• The angle between vectors  $[abc]$  and  $[xyz]$  is given by:

$$ax + by + cz = |(a, b, c)| \cdot |(x, y, z)| \cdot \cos \theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1} \left[ \frac{ax + by + cz}{|(a, b, c)| \cdot |(x, y, z)|} \right]$$

- For  $\{100\}$  and  $\{110\} \rightarrow 45^\circ$
- For  $\{100\}$  and  $\{111\} \rightarrow 54.74^\circ$
- For  $\{110\}$  and  $\{111\} \rightarrow 35.26^\circ, 90^\circ,$  and  $144.74^\circ$

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### Silicon Crystal Origami

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]

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### Undercutting Via Anisotropic Si Etching

- Concave corners bounded by  $\{111\}$  are not attacked
- ... but convex corners bounded by  $\{111\}$  are attacked
- Two  $\{111\}$  planes intersecting now present two dangling bonds  $\rightarrow$  no longer have just one dangling bond  $\rightarrow$  etch rate fast
- Result: can undercut regions around convex corners

[Ristic]

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### Corner Compensation

- Protect corners with "compensation" areas in layout
- Below: Mesa array for self-assembly structures [Smith 1995]

Mask pattern

Shaded regions are the desired result

Groove  $W_1$

$d = \text{Depth of groove}$

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**Other Anisotropic Silicon Etchants**

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - ↳ Etch rate (100) = 0.5-1.5 μm/min
  - ↳ Attacks Al
    - Si-doped Al safe & IC compatible
  - ↳ Etch ratio (100)/(111) = 10-35
  - ↳ Etch masks: SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub> ~ 0.05-0.25 nm/min
  - ↳ Boron doped etch stop, up to 40× slower
- EDP (115°C)
  - ↳ Carcinogenic, corrosive
  - ↳ Etch rate (100) = 0.75 μm/min
  - ↳ Al may be etched
  - ↳ R(100) > R(110) > R(111)
  - ↳ Etch ratio (100)/(111) = 35
  - ↳ Etch masks: SiO<sub>2</sub> ~ 0.2 nm/min, Si<sub>3</sub>N<sub>4</sub> ~ 0.1 nm/min
  - ↳ Boron doped etch stop, 50× slower

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**Boron-Doped Etch Stop**

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**Boron-Doped Etch Stop**

- Control etch depth precisely with boron doping (p++)
  - ↳ [B] > 10<sup>20</sup> cm<sup>-3</sup> reduces KOH etch rate by 20-100×
  - ↳ Can use gaseous or solid boron diffusion
  - ↳ Recall etch chemistry:
 
$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
  - ↳ At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH<sup>-</sup>
- **Result:**
  - ↳ Beams, suspended films
  - ↳ 1-20 μm layers possible

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**Ex: Micronozzle**

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

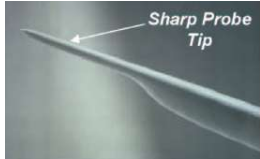
1. Pattern mask  
2. Etch circle in p++  
3. Mask front side  
4. Anisotropic etch

[Maluf]

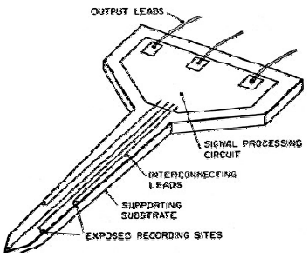
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**Ex: Microneedle**

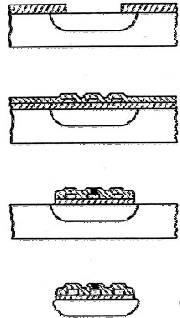
- Below: micro-neurostimulator
  - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan



Sharp Probe Tip



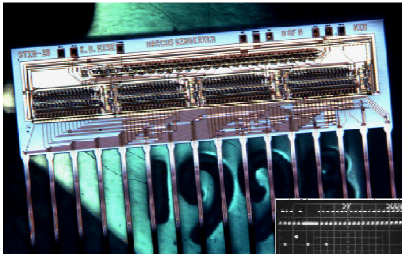
Multi-Channel Recording Array Structure



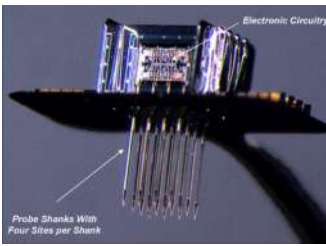
- Selectively diffuse p++ into substrate
- Deposit interconnect pattern and insulate conductors
- Pattern dielectric and metallize recording sites
- Dissolve away the wafer (no mask needed)

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**Ex: Microneedles (cont.)**



64-Site Multiplexed Stimulating Array



Probe Shanks With Four Sites per Shank

[Wise, U. of Michigan]

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400  $\mu\text{m}$  site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

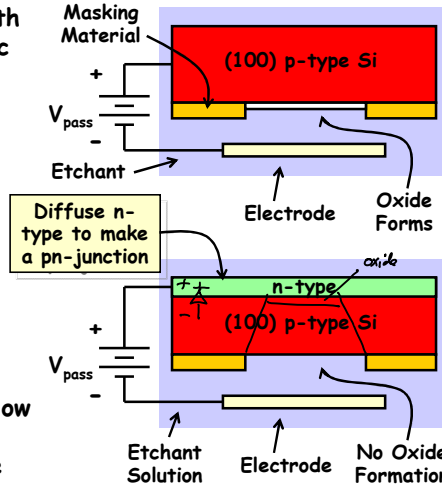
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**Electrochemical Etch Stop**

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**Electrochemical Etch Stop**

- When silicon is biased with a sufficiently large anodic potential relative to the etchant  $\rightarrow$  get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented  $\rightarrow$  no oxide growth, and etching can proceed
  - Can prevent current flow by adding a reverse-biased diode structure



Masking Material

(100) p-type Si

$V_{\text{pass}}$

Etchant

Electrode

Oxide Forms

Diffuse n-type to make a pn-junction

n-type

(100) p-type Si

$V_{\text{pass}}$

Etchant Solution

Electrode

No Oxide Formation

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### Electrochemical Etch Stop

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- Electrochemical etch stop
  - n-type epitaxial layer grown on p-type wafer forms p-n junction diode
  - $V_p > V_n \rightarrow$  electrical conduction (current flow)
  - $V_p < V_n \rightarrow$  reverse bias current (very little current flow)
- Passivation potential: potential at which thin  $\text{SiO}_2$  film forms
  - different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- Setup:
  - p-n diode in reverse bias
  - p-substrate floating  $\rightarrow$  etched
  - n-layer above passivation potential  $\rightarrow$  not etched

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### Electrochemical Etching of CMOS

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- N-type Si well with circuits suspended f/  $\text{SiO}_2$  support beam
- Thermally and electrically isolated
- If use TMAH etchant, doped (w/Si) Al bond pads safe

[Reay, et al. (1994)]  
[Kovacs Group, Stanford]

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### Ex: Bulk Micromachined Pressure Sensors

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- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection  $< 1 \mu\text{m}$

n-type epilayer, p-type substrate

*Deposit insulator*

*Diffuse piezoresistors*

*Deposit & pattern metal*

*Electrochemical etch of backside cavity*

*Anodic bonding of glass*

[Maluf]

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### Ex: Pressure Sensors

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- Below: catheter tip pressure sensor [Lucas NovaSensor]
  - Only  $150 \times 400 \times 900 \mu\text{m}^3$

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### Deep Reactive-Ion Etching (DRIE)

**The Bosch process:**

- Inductively-coupled plasma
- Etch Rate: 1.5-4  $\mu\text{m}/\text{min}$
- Two main cycles in the etch:
  - Etch cycle** (5-15 s):  $\text{SF}_6$  ( $\text{SF}_x^+$ ) etches Si
  - Deposition cycle**: (5-15 s):  $\text{C}_4\text{F}_8$  deposits fluorocarbon protective polymer ( $\text{CF}_2^-$ )<sub>n</sub>
- Etch mask selectivity:
  - $\text{SiO}_2 \sim 200:1$
  - Photoresist  $\sim 100:1$
- Issue**: finite sidewall roughness
  - scalloping < 50 nm
- Sidewall angle:  $90^\circ \pm 2^\circ$

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### DRIE Issues: Etch Rate Variance

- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

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### DRIE Issues: "Footing"

- Etch depth precision
  - Etch stop: buried layer of  $\text{SiO}_2$
  - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches  $\text{SiO}_2$
- Problem**: Lateral undercut at Si/ $\text{SiO}_2$  interface  $\rightarrow$  "footing"
  - Caused by charge accumulation at the insulator

Charging-induced potential perturbs the E-field  
 $\rightarrow$  Distorts the ion trajectory  
 $\rightarrow$  Result: strong and localized damage to the structure at Si- $\text{SiO}_2$  interface  $\rightarrow$  "footing"

Poor charge relaxation and lack of neutralization by e<sup>-</sup>s at insulator  
 $\rightarrow$  Ion flux into substrate builds up (+) potential

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### Recipe-Based Suppression of "Footing"

- Use **higher process pressure** to reduce ion charging [Nozawa]
  - High operating pressure  $\rightarrow$  concentration of (-) charge increases and can neutralize (+) surface charge
  - Issue**: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe** to reduce overetching [Schmidt]
  - Change  $\text{C}_4\text{F}_8$  flow rate, pressure, etc., to enhance passivation and reduce overetching
  - Issue**: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
  - Low frequency  $\rightarrow$  more ions with low directionality and kinetic energy  $\rightarrow$  neutralizes (-) potential barrier at trench entrance
  - Allows e<sup>-</sup>s to reach the trench base and neutralize (+) charge  $\rightarrow$  maintain charge balance inside the trench

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### Metal Interlayer to Prevent "Footing"

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mask  
Si  
Metal interlayer (grounded to sub.)  
glass

Charges relaxation  
Trench for metal definition

Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial)	(f) Silicon Thinning
(b) Preparatory trenches	(g) Photolithography 2
(c) Metal interlayer deposition	(h) DRIE
(d) Lift-off (remove PR)	(i) Remove metal interlayer
(e) Anodic Bonding	(j) Metallize

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### Footing Prevention (cont.)

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- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach

[Kim, Stanford]

No metal interlayer  
Local damages  
Pre trench (cavity)  
Glass substrate

Footing

No footing  
Damage free!  
With metal interlayer

DRIE Trench  
Footing  
Sacrificial Oxide Layer  
Silicon Device Layer

[Kim, Seoul Nat. Univ.]

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