

EE C247B - ME C218

Introduction to MEMS Design


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Lecture Module 14: Sensing Circuits

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Lecture Outline

- Reading: Senturia, Chpt. 14
- Lecture Topics:
 - ↳ Detection Circuits
 - Velocity Sensing
 - Position Sensing

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Velocity-to-Voltage Conversion

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- To convert velocity to a voltage, use a resistive load

Consider the mechanical device by itself first, w/ output shorted

Now, taking RL into account

Lx + Cx cancel @ resonance

Solve the problem @ resonance first, then multiply by H(s)

w/ altered Q

$$\frac{x}{F_{dl}}(s) = \frac{\omega_0 Q}{k} \Theta(s)$$

$$[F_{dl} = \eta_{e1} V_i] \Rightarrow \frac{x}{V_i}(s) = \eta_{e1} \frac{\omega_0 Q}{k} \Theta(s)$$

$$[i_0 = \eta_{e2} x] \Rightarrow \frac{i_0}{V_i}(s) = \eta_{e1} \eta_{e2} \frac{\omega_0 Q}{k} \Theta(s)$$

$$\frac{1}{R_{x12}} \Rightarrow \frac{\eta_{e1} \eta_{e2} Q}{m \omega_0} \Theta(s)$$

$$\frac{V_o}{V_i}(s) = \frac{R_L}{R_{x12} + R_L} \Theta(s)$$

$$\frac{i_0}{V_i}(s) = \frac{1}{R_{x12}} \Theta(s)$$

$$Q' = Q \left(\frac{R_{x12}}{R_{x12} + R_L} \right)$$

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Velocity-to-Voltage Conversion

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- To convert velocity to a voltage, use a resistive load

Since this structure has completely symmetrical I/O ports:

Cx & Lx cancel

Work @ resonance: (to simplify the analysis)

$$\frac{V_o}{V_i} = \frac{R_o}{R_x + R_o} \text{ (@ resonance)}$$

Then, generalize to off resonance:

$$\frac{V_o}{V_i} = \frac{R_o}{R_x + R_o} \Theta(s, Q'), \text{ where } Q' = Q \left(\frac{R_x}{R_x + R_o} \right)$$

Voltage Representing Velocity

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Velocity-to-Voltage Conversion

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- To convert velocity to a voltage, use a resistive load

cantilever

Since this structure has completely symmetrical I/O ports:

Brute force approach:

$$\frac{N_o}{V_i}(s) = \frac{R_D}{R_x + \frac{1}{sC_x} + sL_x + R_D} = \frac{sR_D C_x}{s^2 R_x C_x + 1 + s^2 L_x C_x + sR_D C_x} = \frac{\frac{R_D}{L_x C_x}}{s^2 + s \frac{R_x + R_D}{L_x} + \frac{1}{L_x C_x}}$$

$Q = \frac{\omega_0 L_x}{R_x} \rightarrow Q' = \frac{\omega_0 L_x}{R_x + R_D} \rightarrow \frac{R_x + R_D}{L_x} = \frac{\omega_0}{Q'}$

$$\frac{N_o}{V_i}(s) = \frac{R_D}{R_x + R_D} \frac{s(\omega_0/Q')}{s^2 + s(\omega_0/Q') + \omega_0^2} = \frac{R_D}{R_x + R_D} \mathcal{H}(s, Q')$$

$Q = Q' \left(\frac{R_x}{R_x + R_D} \right)$

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Position-to-Voltage Conversion

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- To sense position (i.e., displacement), use a capacitive load

Again, have port-to-port I/O symmetry:

cantilever

Brute force approach:


$$\frac{N_o}{V_i}(s) = \frac{\frac{1}{sC_D}}{R_x + \frac{1}{sC_x} + sL_x + \frac{1}{sC_D}} = \frac{C_x/C_D}{s^2 R_x C_x + 1 + s^2 L_x C_x + \frac{C_x}{C_D}}$$

$$= \frac{C_x/C_D}{1 + C_x/C_D} \frac{1}{s^2 + s \frac{R_x}{L_x} + \frac{(1 + C_x/C_D)}{L_x C_x}}$$

$\omega_0^2 = \frac{1}{L_x C_x} \rightarrow (\omega_0')^2 = \omega_0^2 (1 + C_x/C_D)$

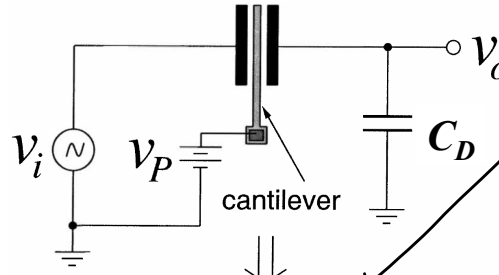
$Q' = \frac{\omega_0' L_x}{R_x} \rightarrow \frac{R_x}{L_x} = \frac{\omega_0'}{Q'}, Q' = Q \sqrt{1 + C_x/C_D}$ over \rightarrow

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Position-to-Voltage Conversion

• To sense position (i.e., displacement), use a capacitive load



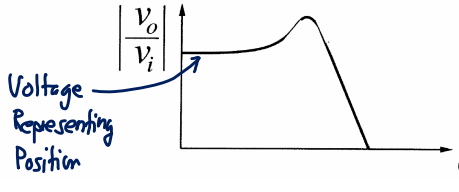
$$\frac{V_o}{V_i}(s) = \underbrace{\frac{C_x/C_D}{1 + C_x/C_D}}_{\text{DC Gain Term}} \underbrace{\frac{(\omega_0)^2}{s^2 + (\frac{\omega_0}{Q})s + (\omega_0)^2}}_{\text{Low-Pass Biquad}}$$

→ To maximize gain → 1, need $C_D \ll C_x$.
 (must minimize C_D)

Note: Can use similar short-cut to the R case.


- ① Get DC response → C's dominate.
- ② Then:

$$\frac{V_o}{V_i}(s) = (\text{DC Gain}) \cdot \frac{1}{s} \cdot \text{LP}(s, \omega_0, Q) \cdot \omega_0 Q$$



Voltage Representing Position

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Velocity Sensing Circuits

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Velocity-to-Voltage Conversion

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- To convert velocity to a voltage, use a resistive load

Since this structure has completely symmetrical I/O ports:

Work @ resonance: (to simplify the analysis)

$$\frac{N_0}{N_i} = \frac{R_0}{R_x + R_0} \text{ (@ resonance)}$$

Then, generalize to off resonance:

$$\frac{N_0}{N_i} = \frac{R_0}{R_x + R_0} \cdot \mathcal{H}(s, Q'), \text{ where } Q' = Q \left(\frac{R_x}{R_x + R_0} \right)$$

Voltage Representing Velocity

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Problems With Purely Resistive Sensing

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Now, we get: (approximately)

$$\frac{N_0}{N_i}(s) \sim \frac{R_0}{R_x + R_0} \cdot \frac{1}{1 + \frac{s}{\omega_p}} \cdot \mathcal{H}(s, \omega_b, Q')$$

Depend on both R_0 & C_p .

$$\omega_p = \frac{1}{(R_x || R_0) C_p}$$

Impact depends on where ω_p is relative to ω_b .

Includes C_o , line C, bond pad C, and next stage C

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Problems With Purely Resistive Sensing

• In general, the sensor output must be connected to the inputs of further signal conditioning circuits \rightarrow input R_i of these circuits can load R_D

These change w/ hook-up \rightarrow not good.

Problem: need a sensing circuit that is immune to parasitics or loading.

\rightarrow

Soln: use op amps.

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The TransR Amplifier Advantage

• The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p and R_i

• The zero output resistance of the (ideal) op amp can drive virtually anything

Virtual Ground \Rightarrow No voltage across C_p
 $\hookrightarrow C_p$ effectively isn't there!

$$V_0 = \frac{R_2}{R_x} \oplus(s) i_i$$

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Position Sensing Circuits

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Problems With Pure-C Position Sensing

- To sense position (i.e., displacement), use a capacitive load

$$\frac{V_o}{V_i}(s) = \frac{C_x/C_D}{1 + C_x/C_D} \cdot \frac{1}{s} \cdot H(s, \omega_0, Q) \cdot \omega_0^2 \theta'$$

Integration yields displacement.
 To maximize gain, minimize C_D .
 \Rightarrow Problem: parasitic capacitance
 $C_D \rightarrow C_b + C_{p_i} + C_{p_b}$
 \Rightarrow DC Gain: $\frac{C_x / (C_x C_{p_i} + C_{p_b})}{1 + C_x / (C_D + C_{p_i} + C_{p_b})}$
Remedy: Suppress C_p via use of op amps.

Output will get smaller!

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The Op Amp Integrator Advantage

• The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p

$N_o = -i_o (R_2 \parallel \frac{1}{sC_2})$
 $\approx -\frac{N_i}{R_x} \cdot \frac{1}{sC_2} \Rightarrow \frac{N_o}{N_i}(s) = -\frac{1}{R_x C_2} \frac{1}{s}$

$R_2 \gg \frac{1}{sC_2}$ (for biasing)
 $R_o = 0 \Omega$
 Can drive next stage's R_i w/o interference to transfer function!
 well defined \rightarrow good!

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Differential Position Sensing

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Differential Position Sensing

Example: ADXL-50

Capacitive divider

$$V_o = -V_p + (2V_p) \frac{C_1}{C_1 + C_2}$$

$$= \frac{-V_p C_1 - V_p C_2 + 2V_p C_1}{C_1 + C_2} = V_p \left(\frac{C_1 - C_2}{C_1 + C_2} \right) = V_o$$

Issue: Parasitic Capacitance

$$V_o = \frac{C_1 - C_2}{C_1 + C_2 + C_p} V_p$$

As before, C_p reduces gain \rightarrow Soln: Use op amp!

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Buffer-Bootstrapped Position Sensing

Includes capacitance from interconnects, bond pads, and C_{gs} of the op amp

C_{gd} = gate-to-drain capacitance of the input MOS transistor

- Bootstrap the ground lines around the interconnect and bond pads
 - \Rightarrow No voltage across C_p
 - \Rightarrow It's effectively not there!

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Effect of Finite Op Amp Gain

Total ADXL-50 Sense C ~ 100fF

Unity Gain Buffer

V_0

$N_0 = A_0(V_i - N_0) = A_0(N_i - N_0) \rightarrow N_0(1 + A_0) = A_0 N_i \rightarrow \frac{N_0}{N_i} = \frac{A_0}{1 + A_0}$

Get $Z_i = \frac{V_i}{i_i}$: $i_i = (N_i - N_0) s C_p = N_i \left(1 - \frac{A_0}{1 + A_0}\right) s C_p = N_i \frac{1}{1 + A_0} s C_p$

$\therefore \frac{N_i}{i_i} = Z_i = \frac{1}{s \left[\frac{C_p}{1 + A_0} \right]}$

$C_{eff} = \frac{C_p}{1 + A_0}$

No longer zero!

Ex: $A_0 = 100, C_p = 2 \text{ pF}$
 $\Rightarrow C_{eff} = \frac{2 \text{ pF}}{101} = \underline{\underline{20 \text{ fF}}}$

Not negligible compared w/ ADXL-50 $C_{tot} \sim 100 \text{ fF!}$

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Integrator-Based Diff. Position Sensing

Integrator-Based Diff. Position Sensing

(for biasing) $R_2 \gg \frac{1}{sC_2}$

$R_0 = 0 \Omega$

Can drive next stage's R_1 w/o interference to transfer function!

$i_0 = i_1 + i_2 = N_p(sC_1) - N_p(sC_2) = N_p s(C_1 - C_2)$

$\therefore N_0 = -i_0 \left(\frac{1}{sC_F} \right) = -N_p \left(\frac{C_1 - C_2}{C_F} \right)$

$\frac{N_0}{V_p} = - \frac{C_1 - C_2}{C_F} \Rightarrow$ A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

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