EE C247B – ME C218
Introduction to MEMS Design
Spring 2016

Prof. Clark T.-C. Nguyen

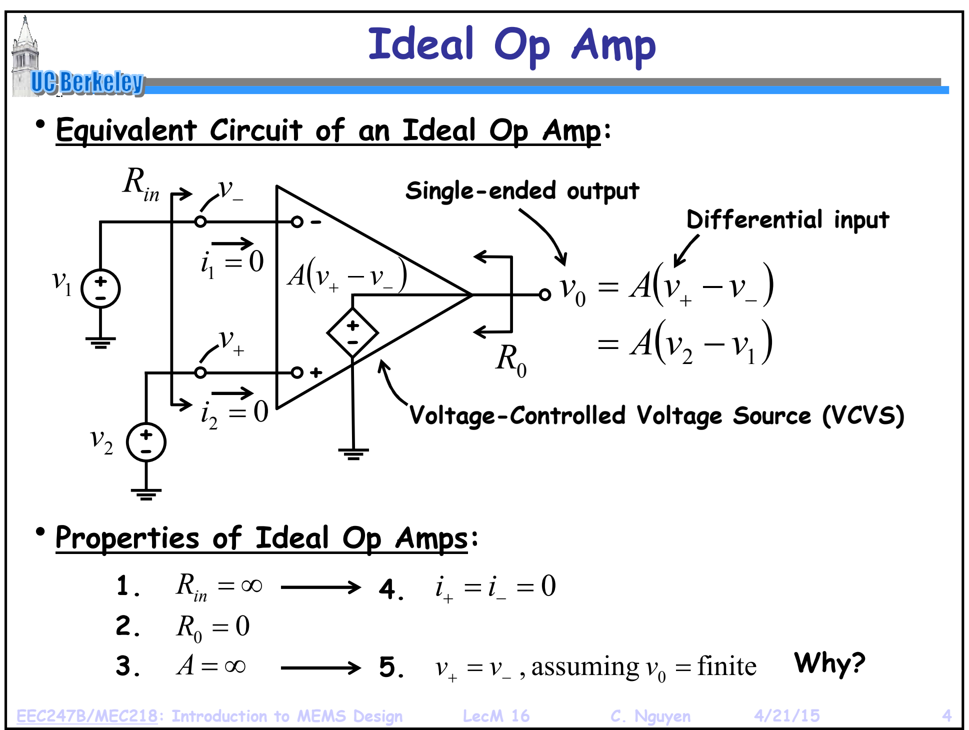
Dept. of Electrical Engineering & Computer Sciences
University of California at Berkeley
Berkeley, CA 94720

Module 16: Sensing Non-Idealities & Integration

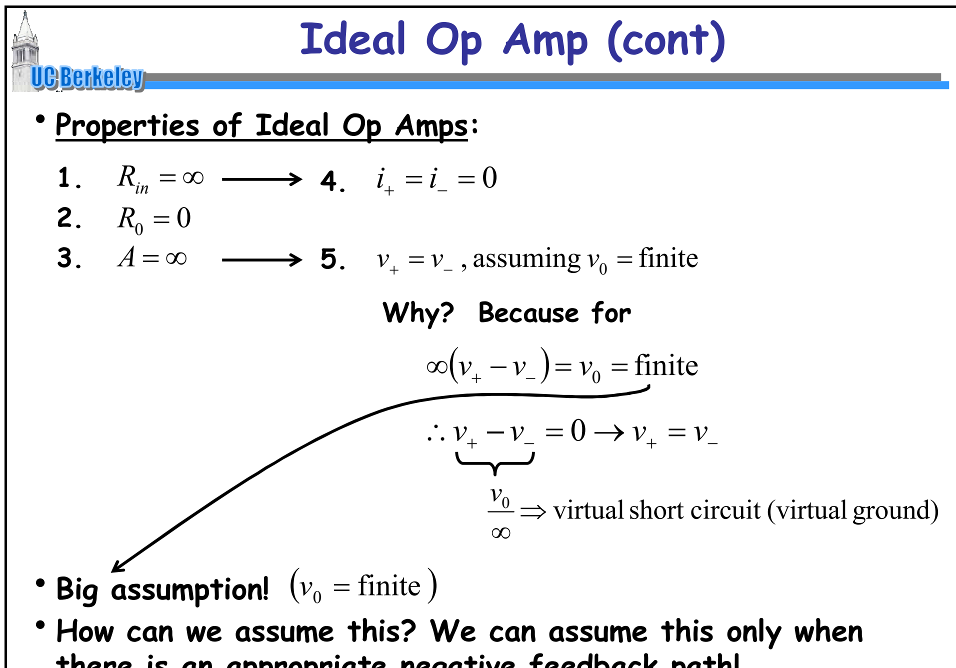
Lecture Outline

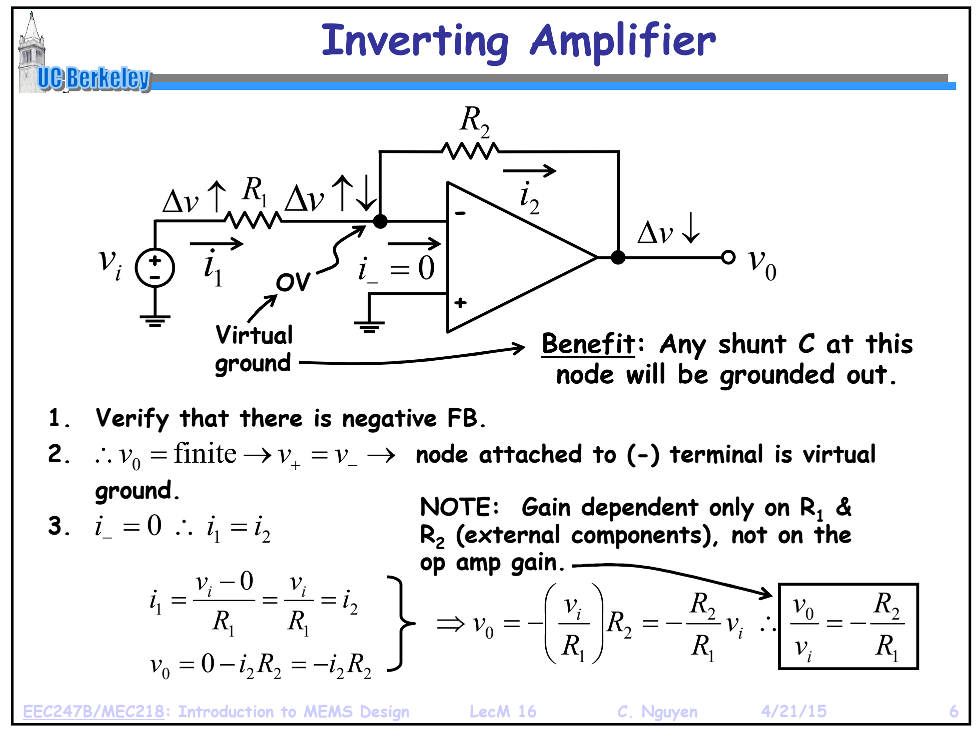
- Reading: Senturia Chpt. 14, 15
- Lecture Topics:
  - Ideal Op Amps
  - Op Amp Non-Idealities
  - MEMS-Transistor Integration
    - Mixed
    - MEMS-First
    - MEMS-Last
  - Op Amp Non-Idealities (cont.)

Copyright © 2016 Regents of the University of California

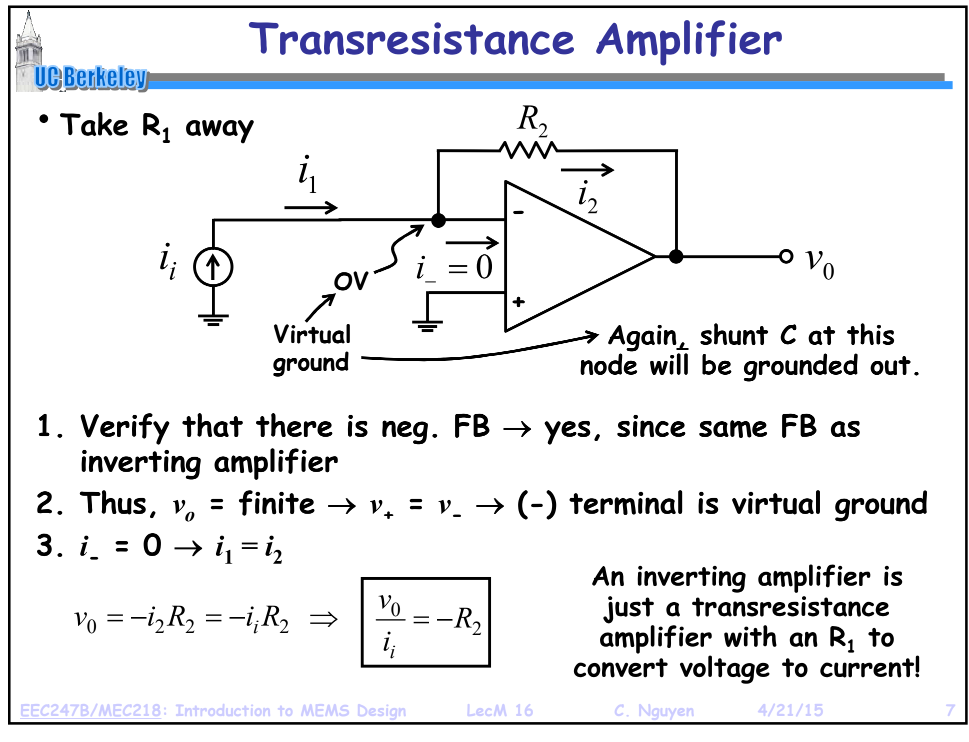


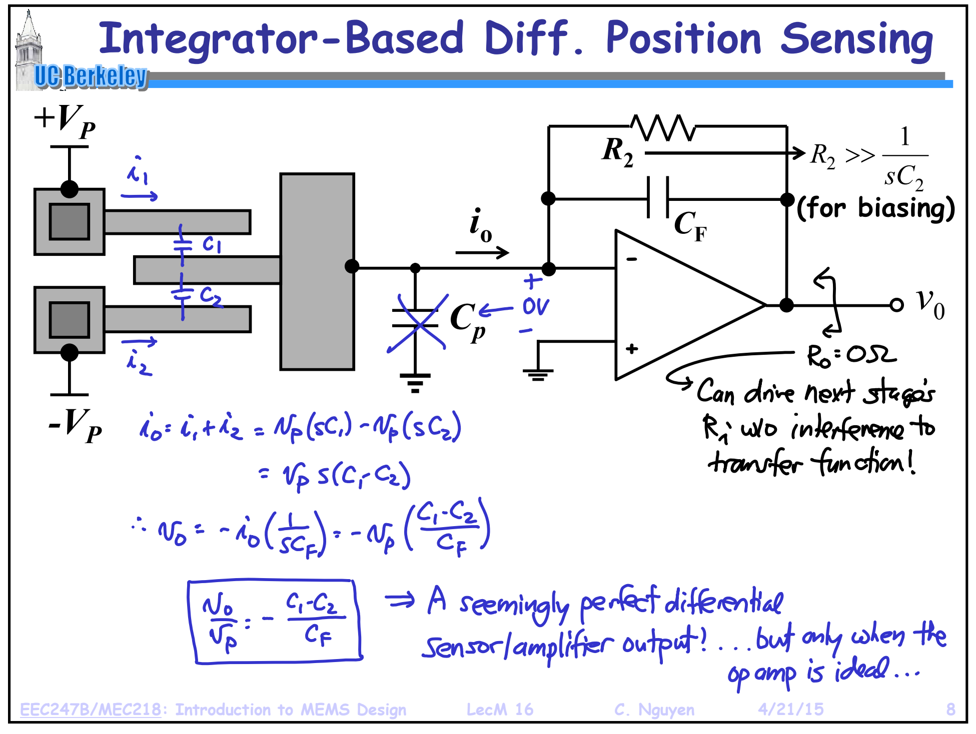
Copyright © 2016 Regents of the University of California



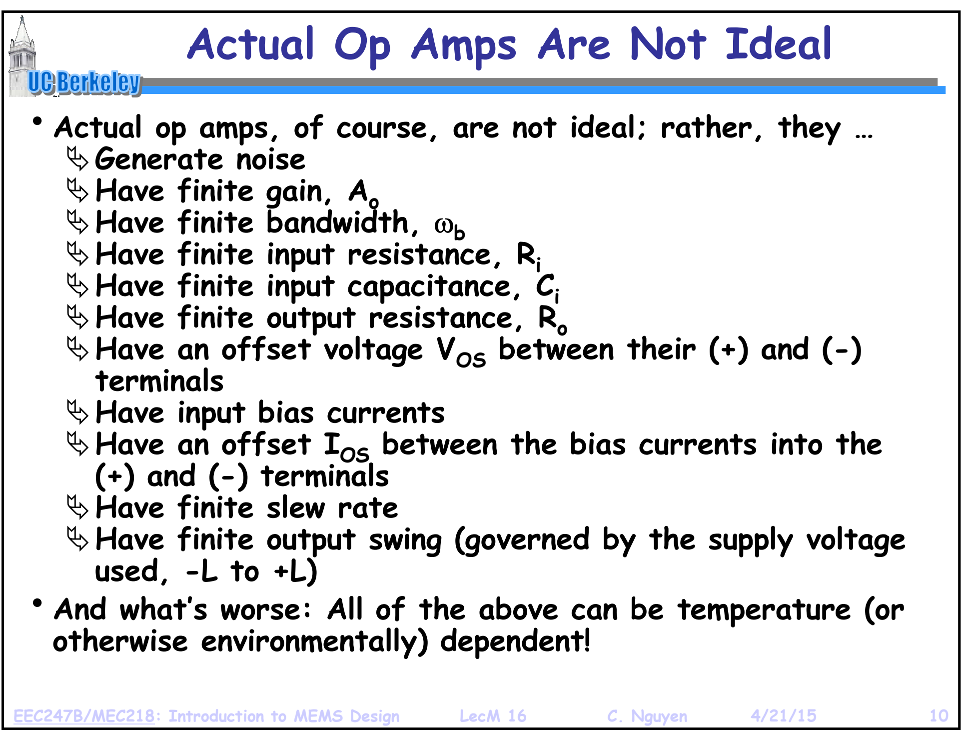


Copyright © 2016 Regents of the University of California

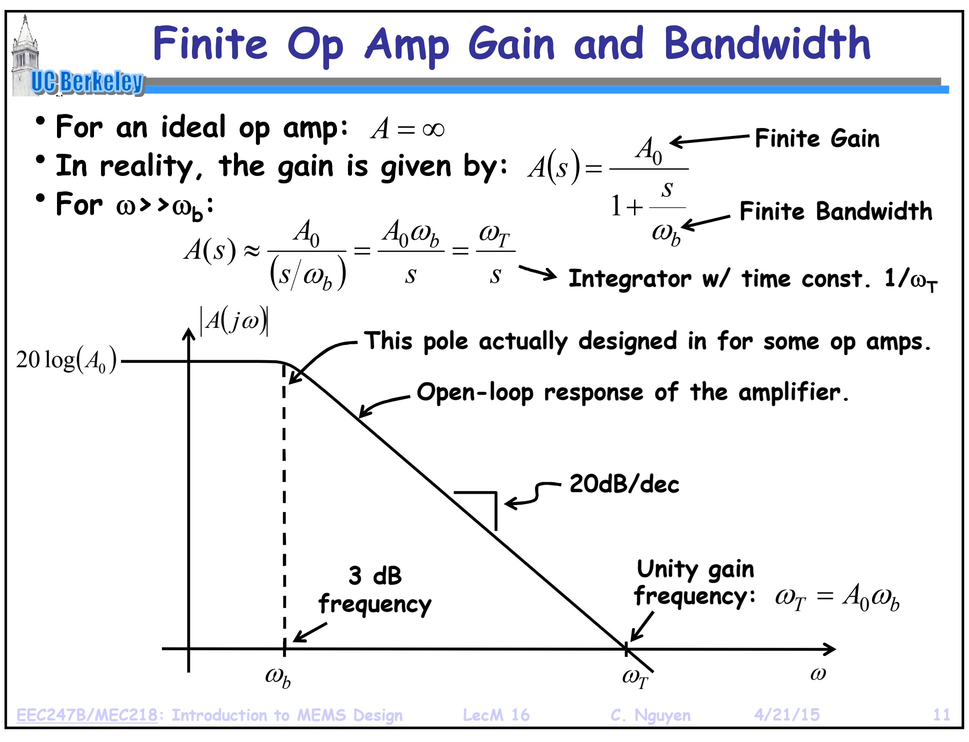


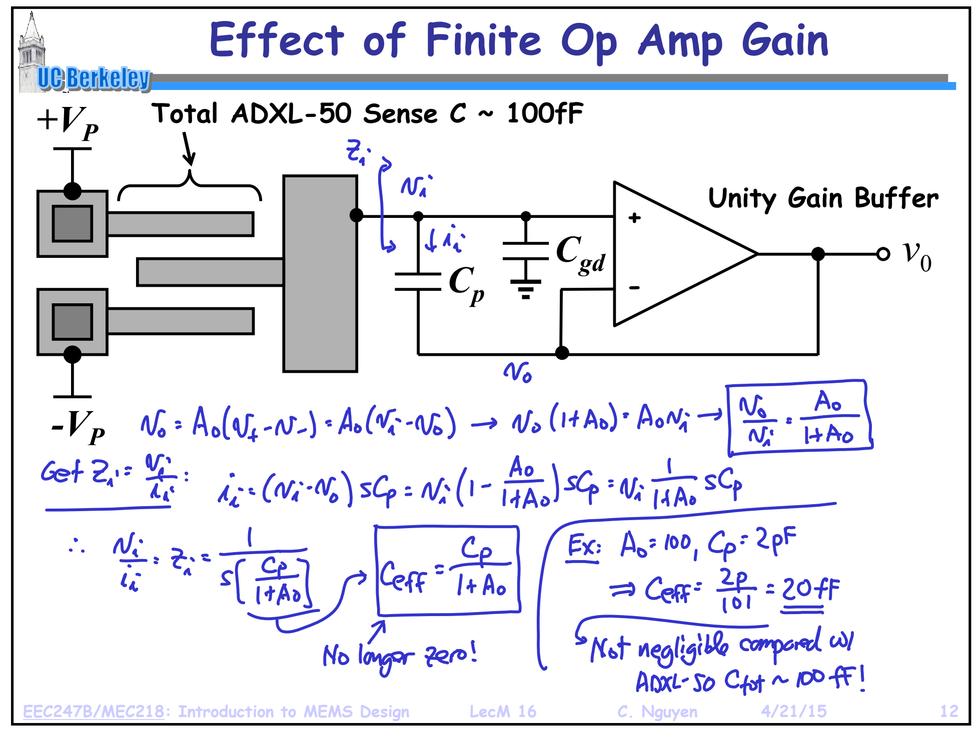


Copyright © 2016 Regents of the University of California

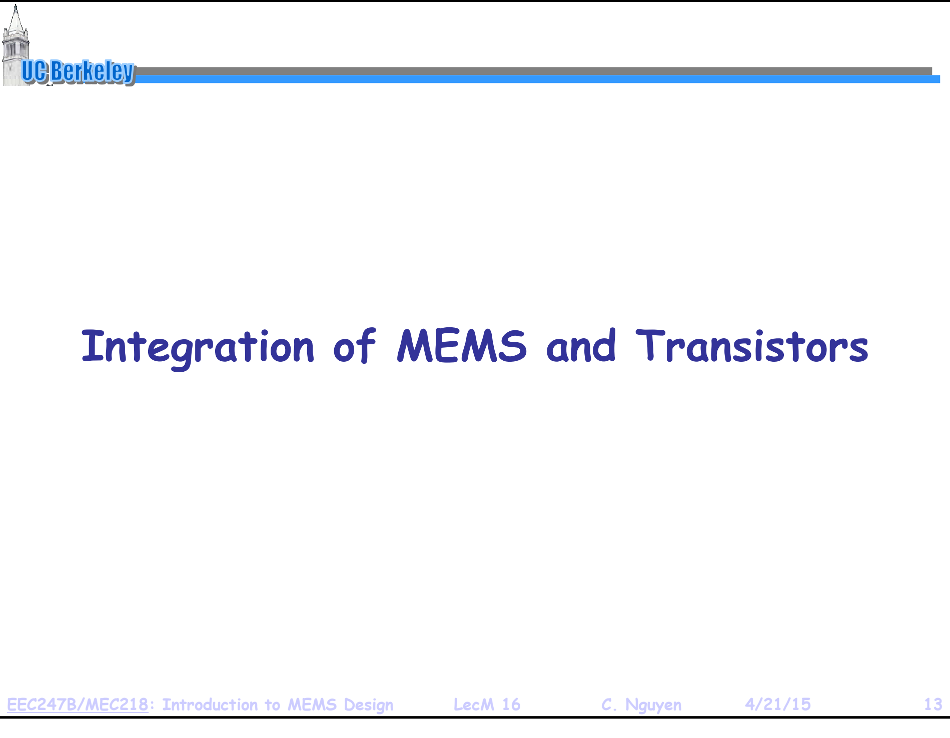


Copyright © 2016 Regents of the University of California





Copyright © 2016 Regents of the University of California

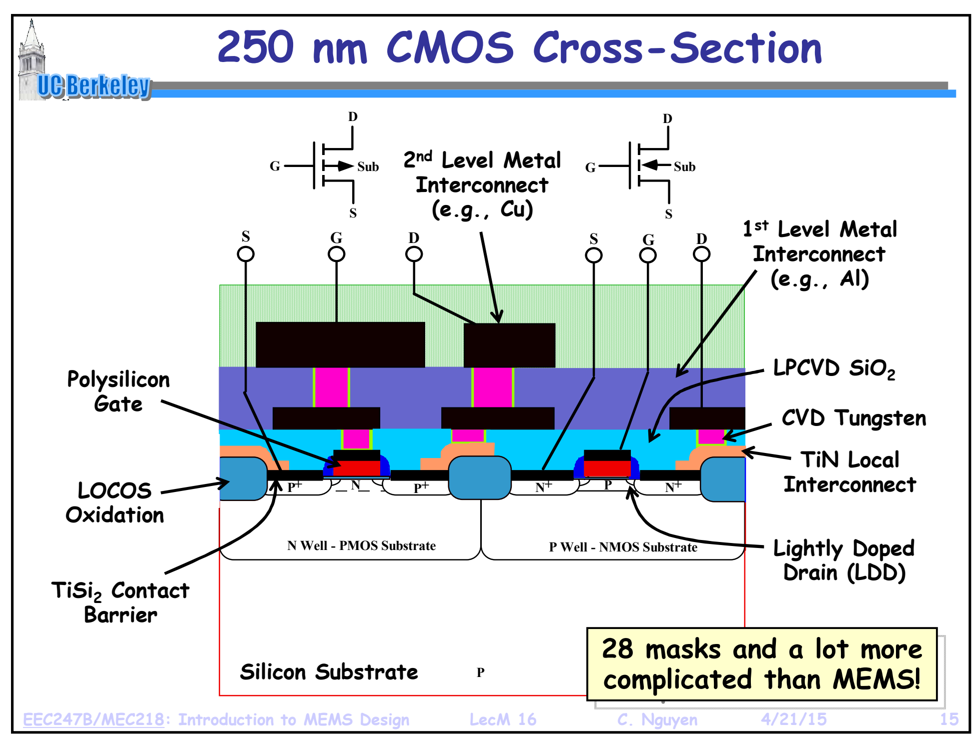


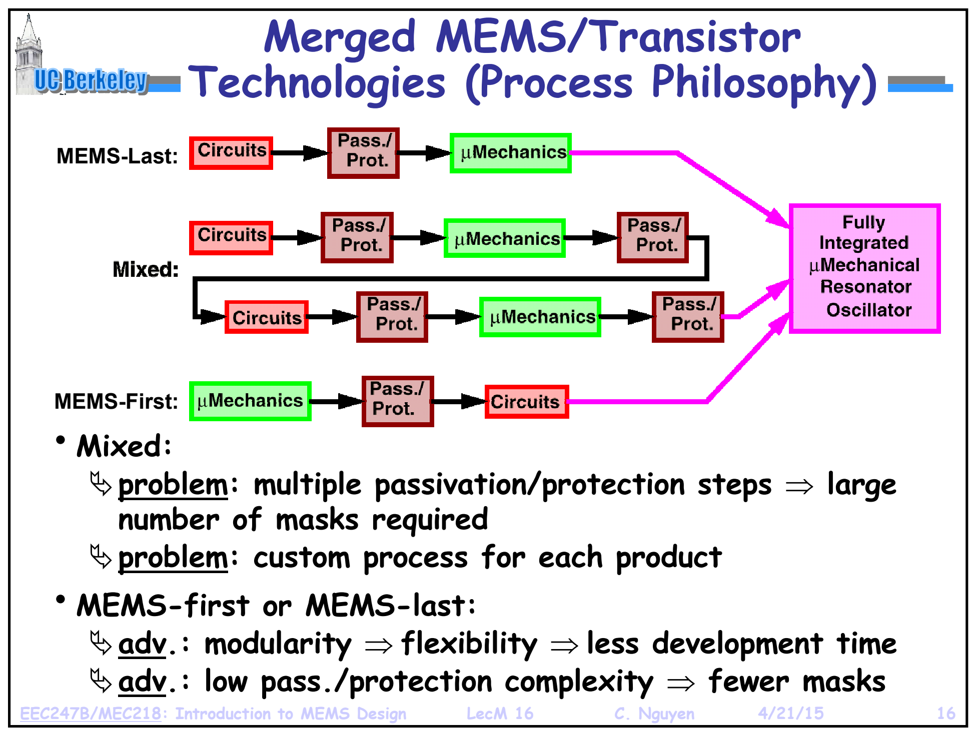
Integrate or Not?

- Benefits:
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality
- Challenges:
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

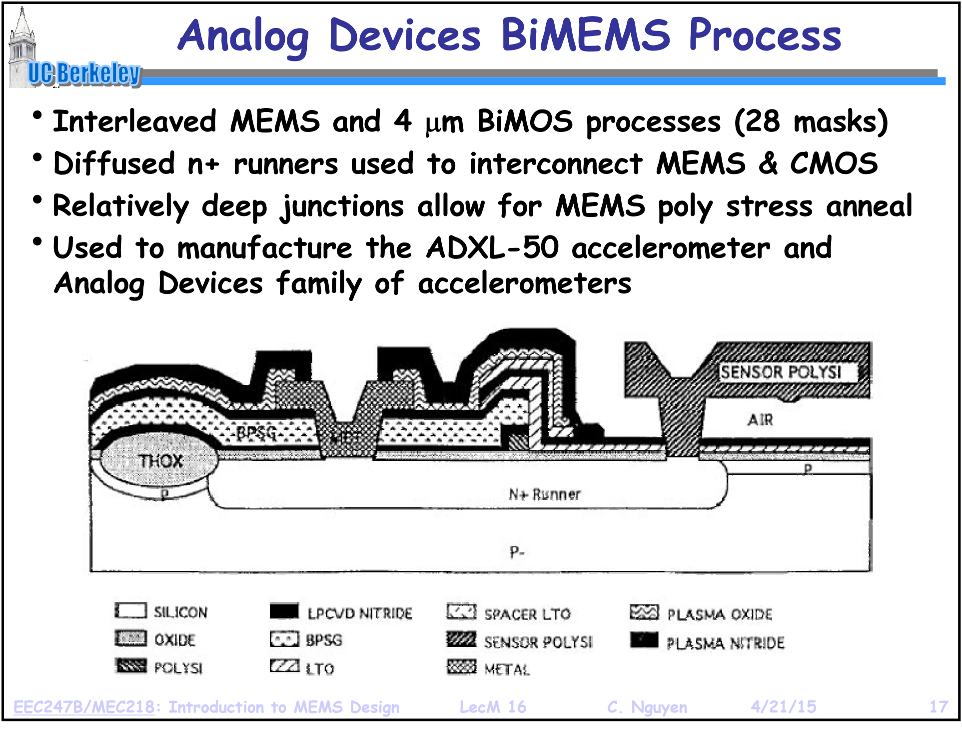
EEC247B/MEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 14

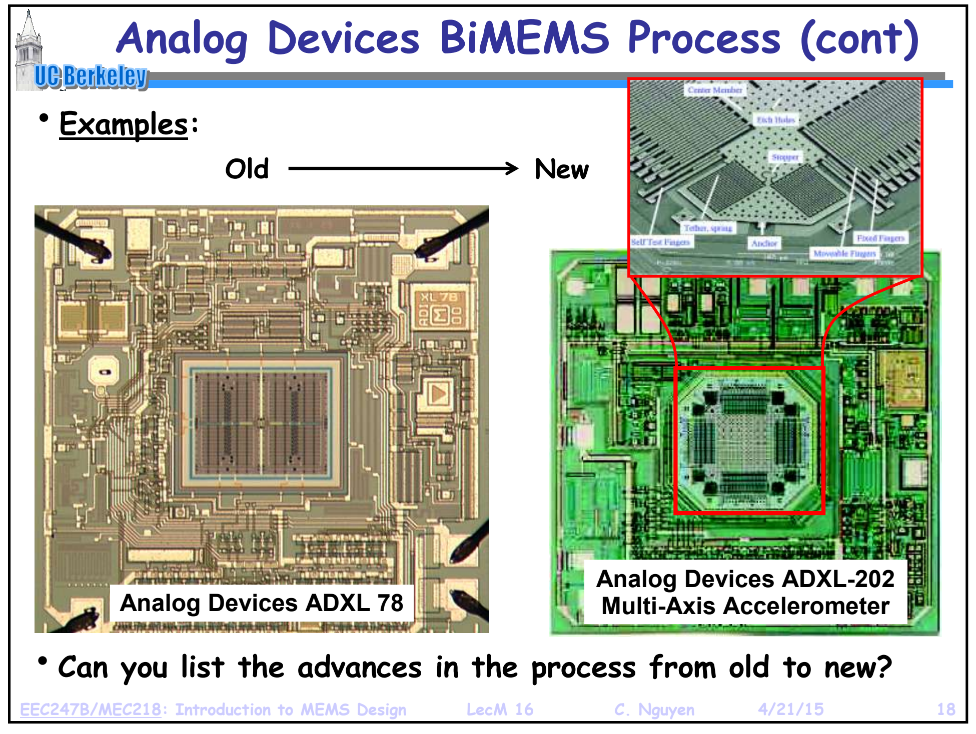
Copyright © 2016 Regents of the University of California



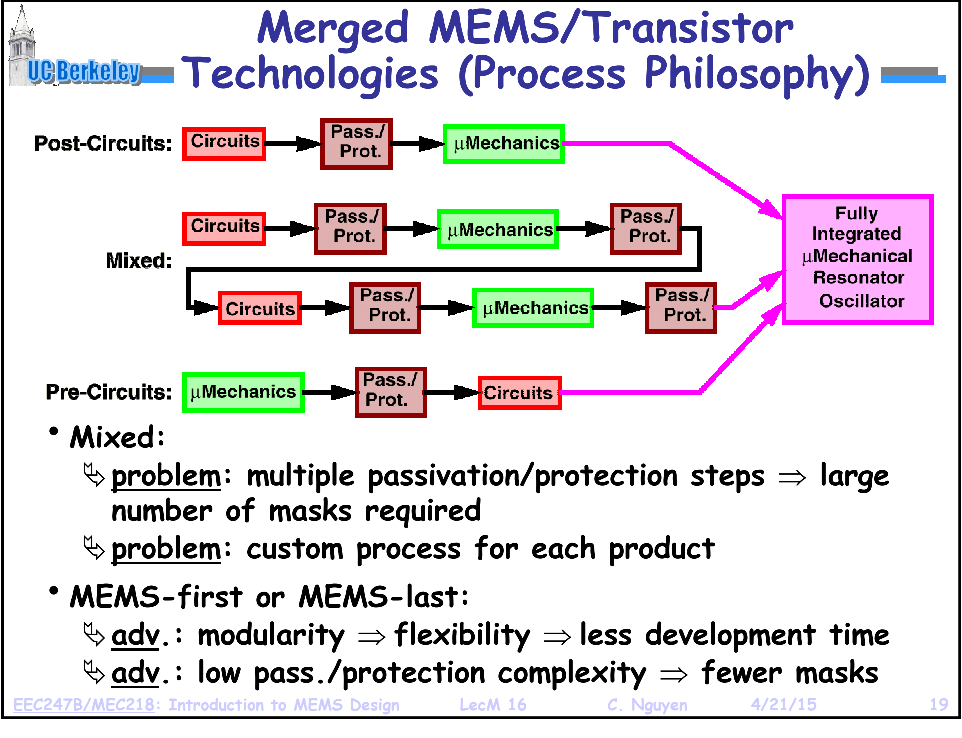


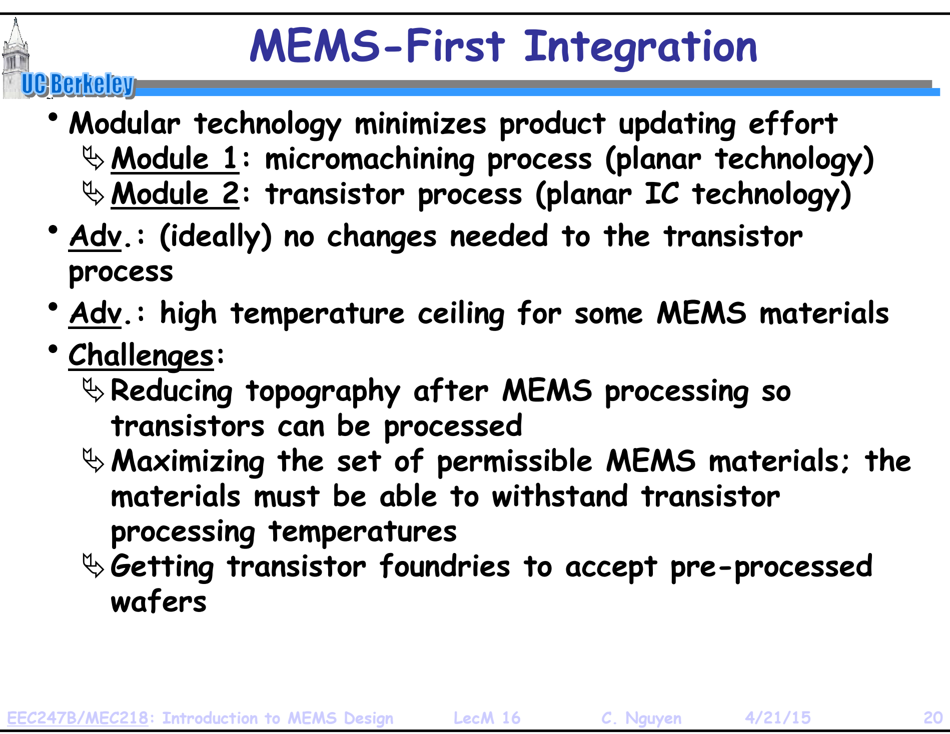
Copyright © 2016 Regents of the University of California



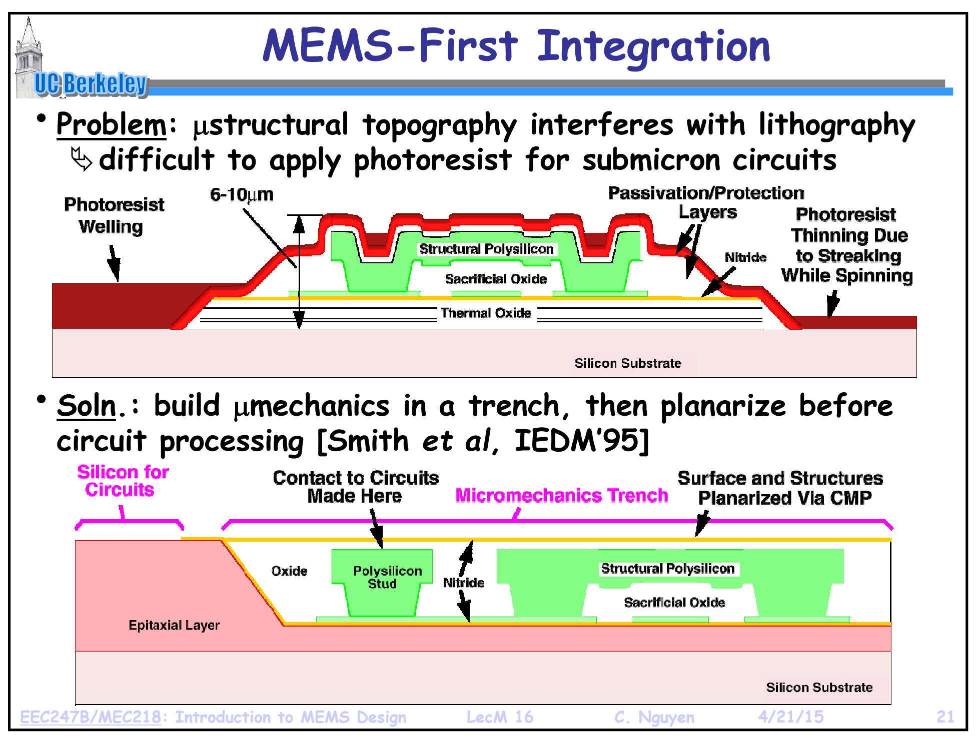


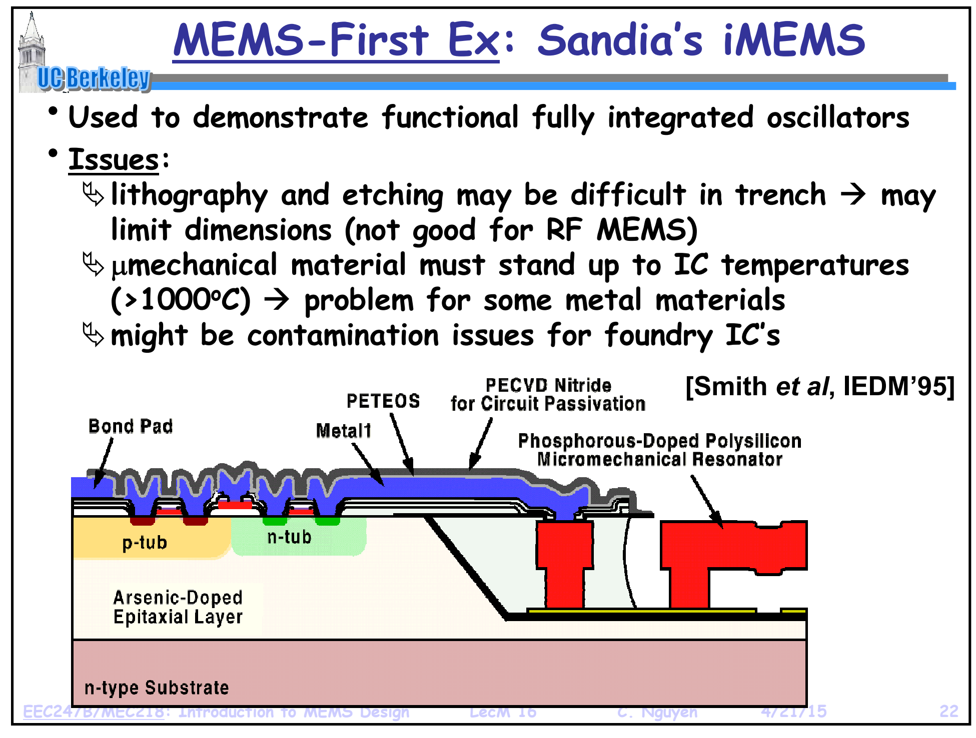
Copyright © 2016 Regents of the University of California



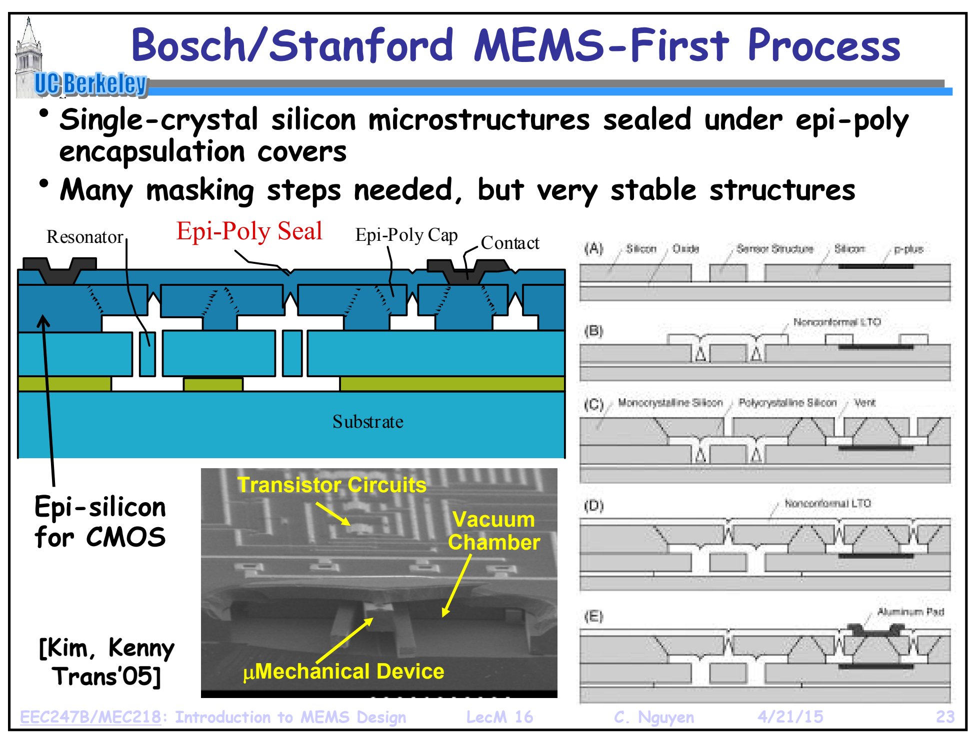


Copyright © 2016 Regents of the University of California





Copyright © 2016 Regents of the University of California



Problems With MEMS-First

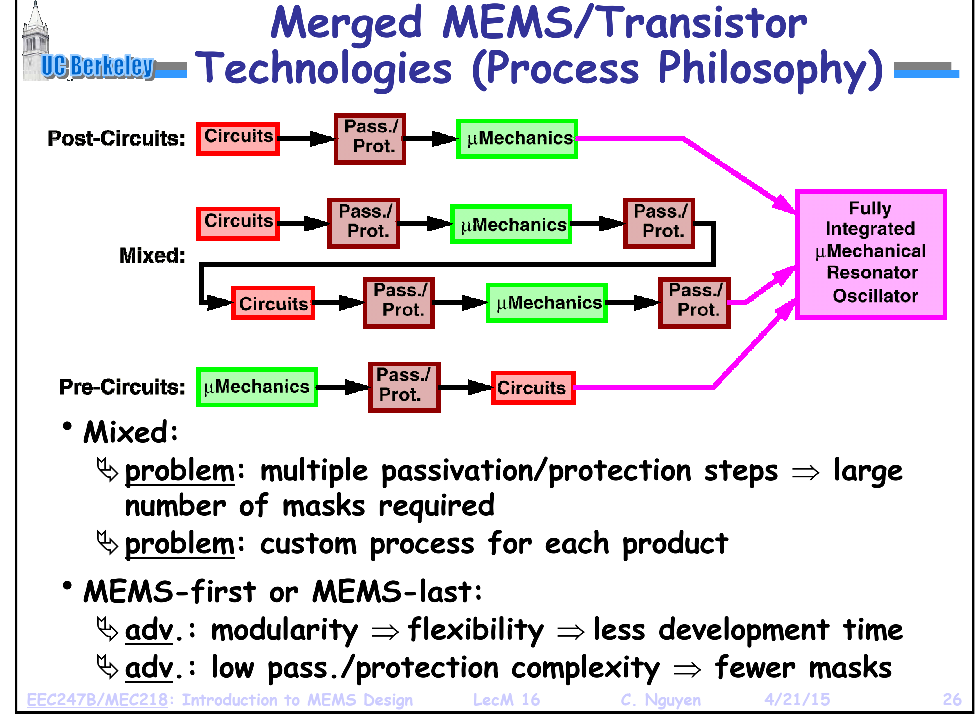
- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - ↳ Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - ↳ thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

EEC247B/MEC218: Introduction to MEMS Design LecM 16 C. Nguyen 4/21/15 24

Copyright © 2016 Regents of the University of California

Foundry Acceptance of MEMS-First?

- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon



Merged MEMS/Transistor Technologies (Process Philosophy)

- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

Copyright © 2016 Regents of the University of California

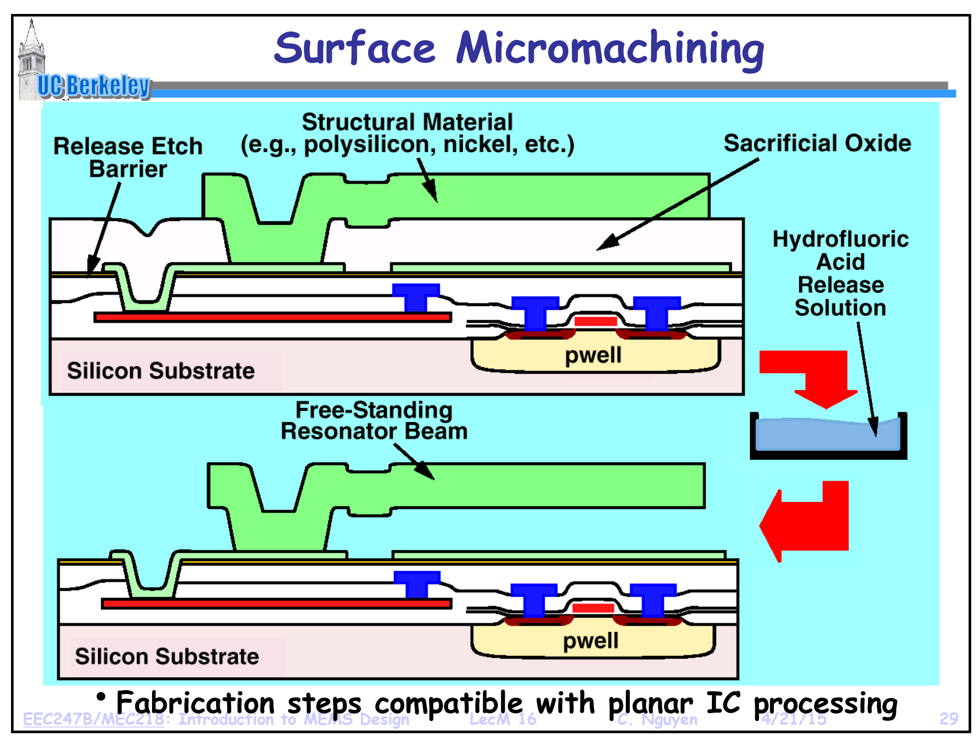
MEMS-Last Integration

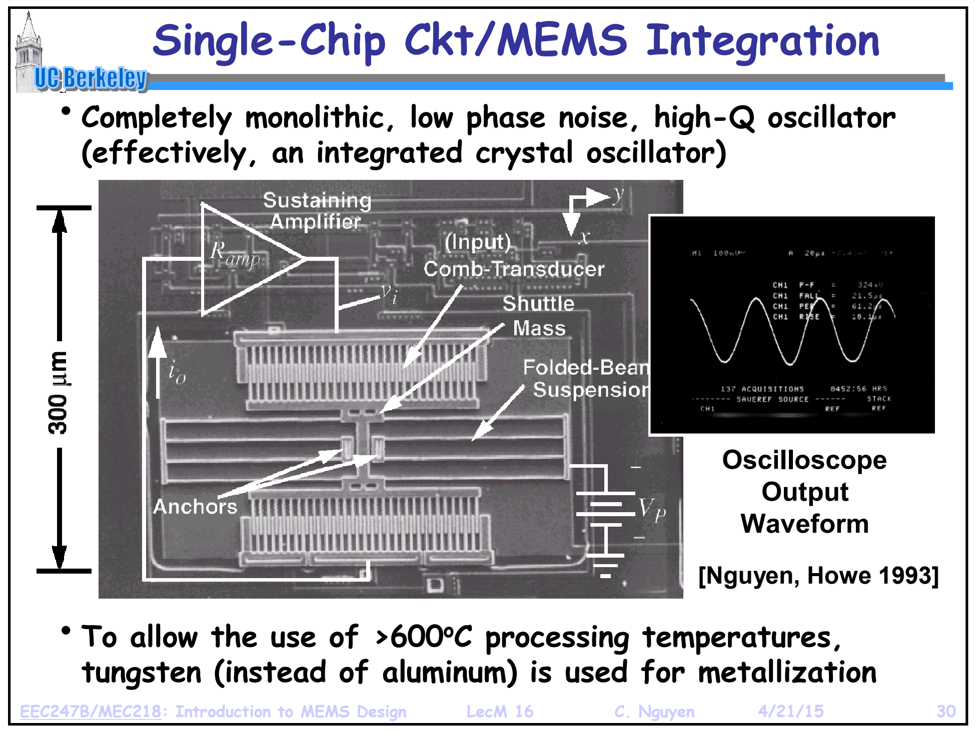
- Modular technology minimizes product updating effort
  - Module 1: transistor process (planar IC technology)
  - Module 2: micromachining process (planar technology)
- Adv.: foundry friendly
  - Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- Issue: limited thermal budget limits the set of usable structural materials
  - Metallization goes bad if temperature gets too high
  - Aluminum grows hillocks and spikes junctions if T>500°C
  - Copper diffusion can be an issue at high temperature
  - Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

Berkeley Polysilicon MICS Process

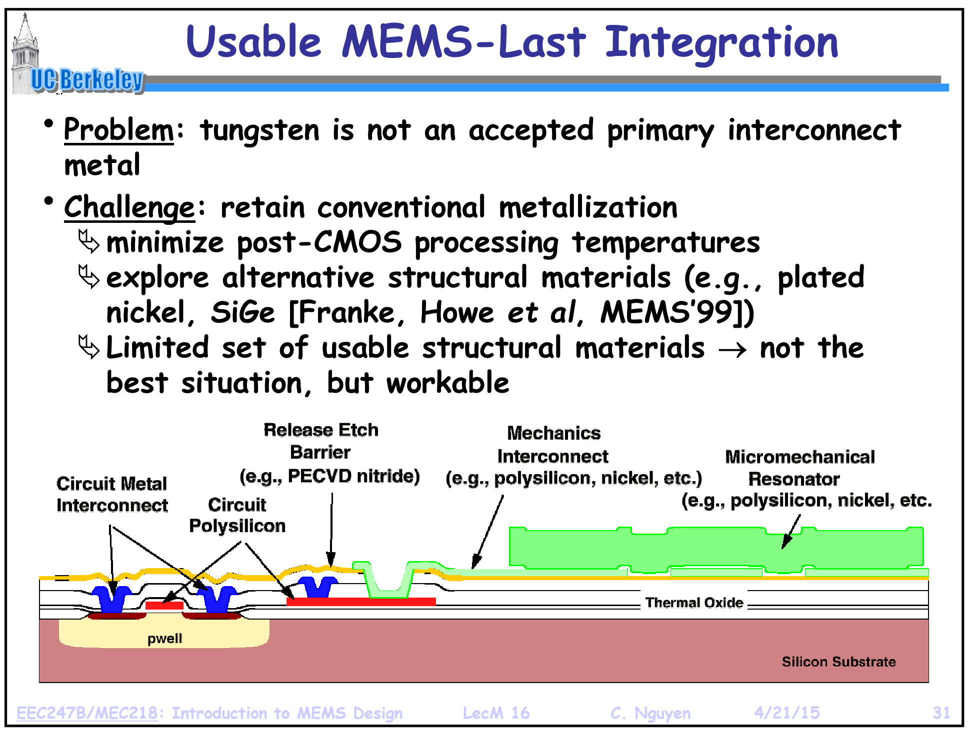
- Uses surface-micromachinedpolysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. T~600°C; nitride dep. T~835°C
  - 1100°C RTA stress anneal for 1 min.
  - metal and junctions must withstand temperatures ~835°C
  - tungsten metallization used with $TiSi_2$ contact barriers
  - *in situ* doped structural polySi; rapid thermal annealing

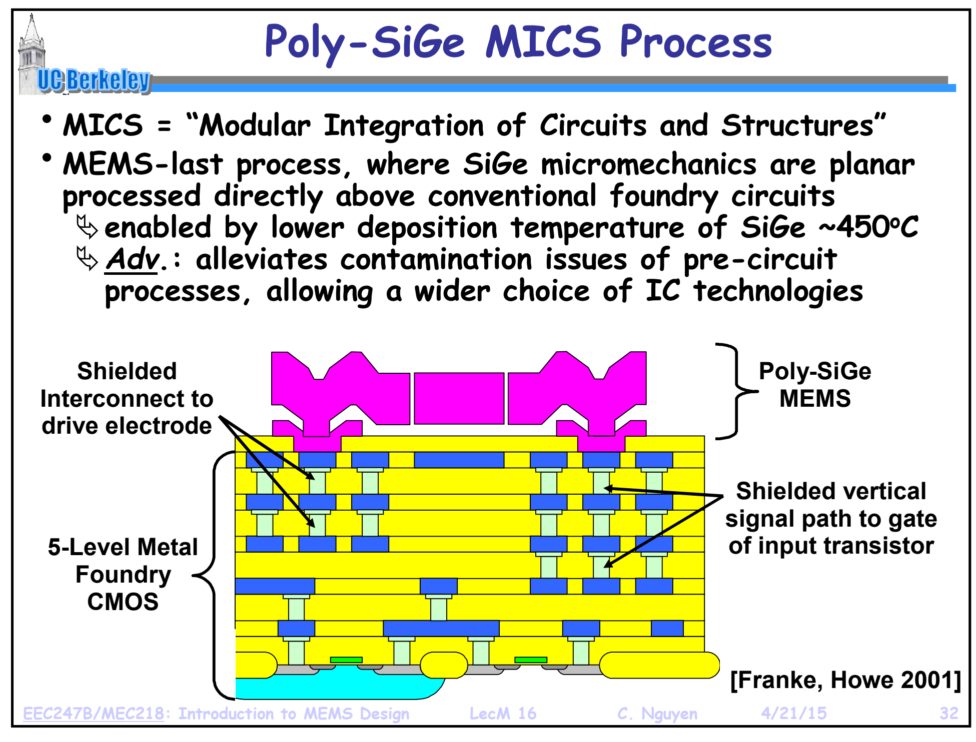
Copyright © 2016 Regents of the University of California



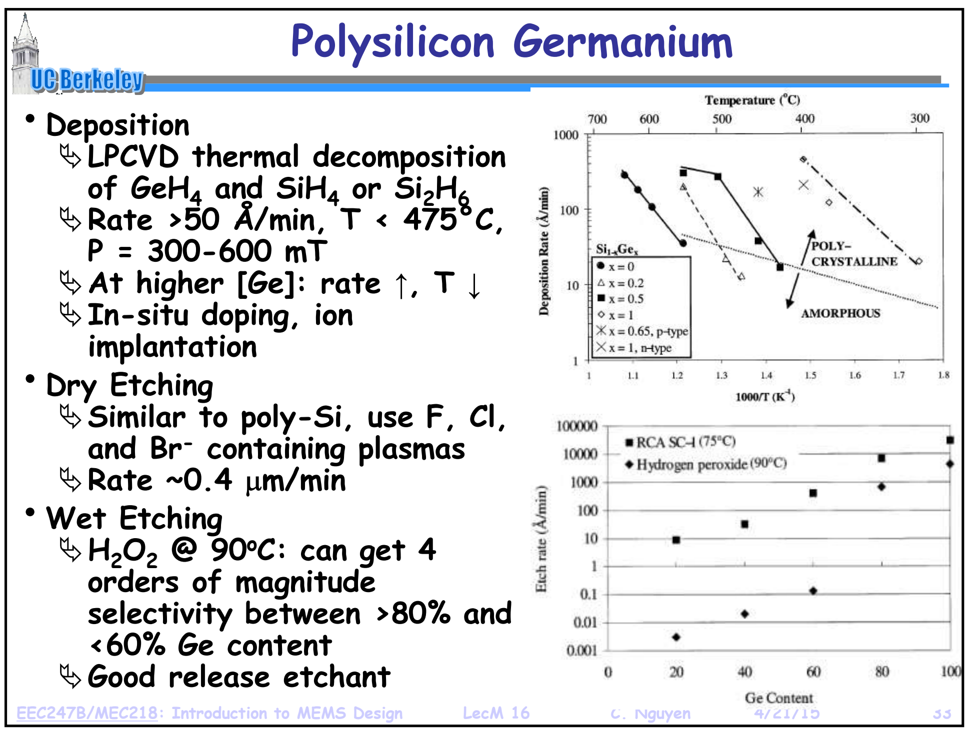


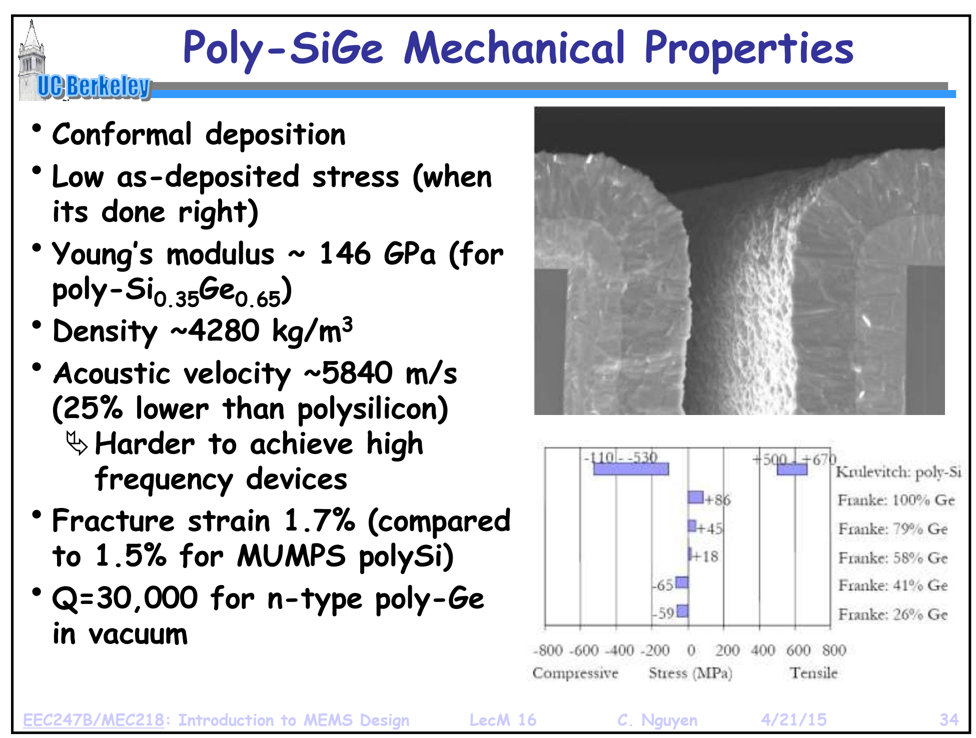
Copyright © 2016 Regents of the University of California



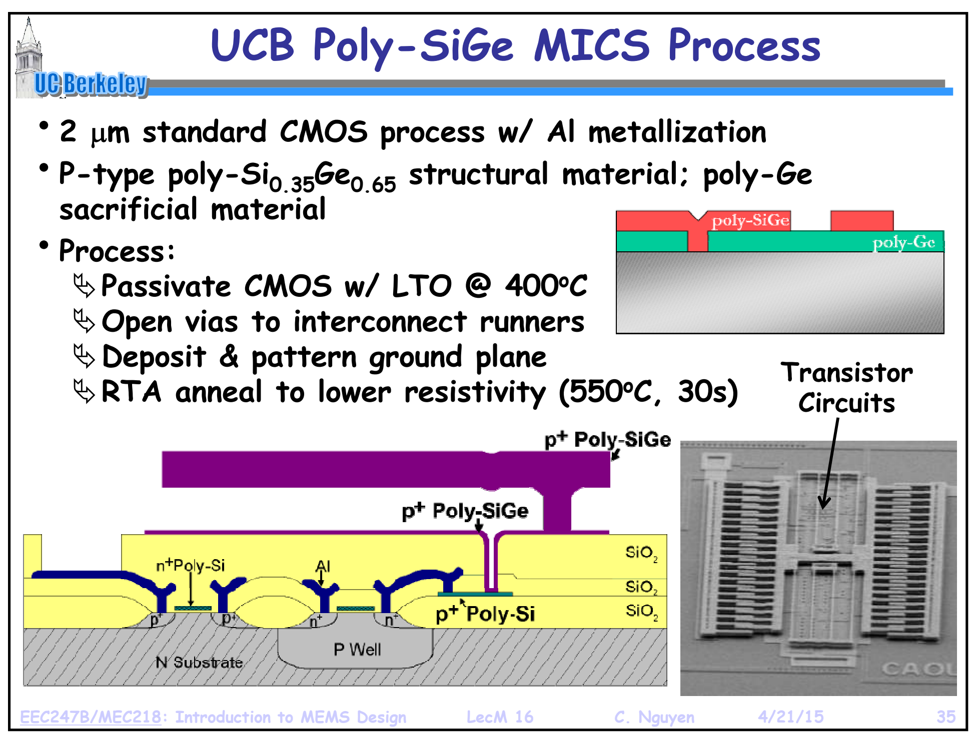


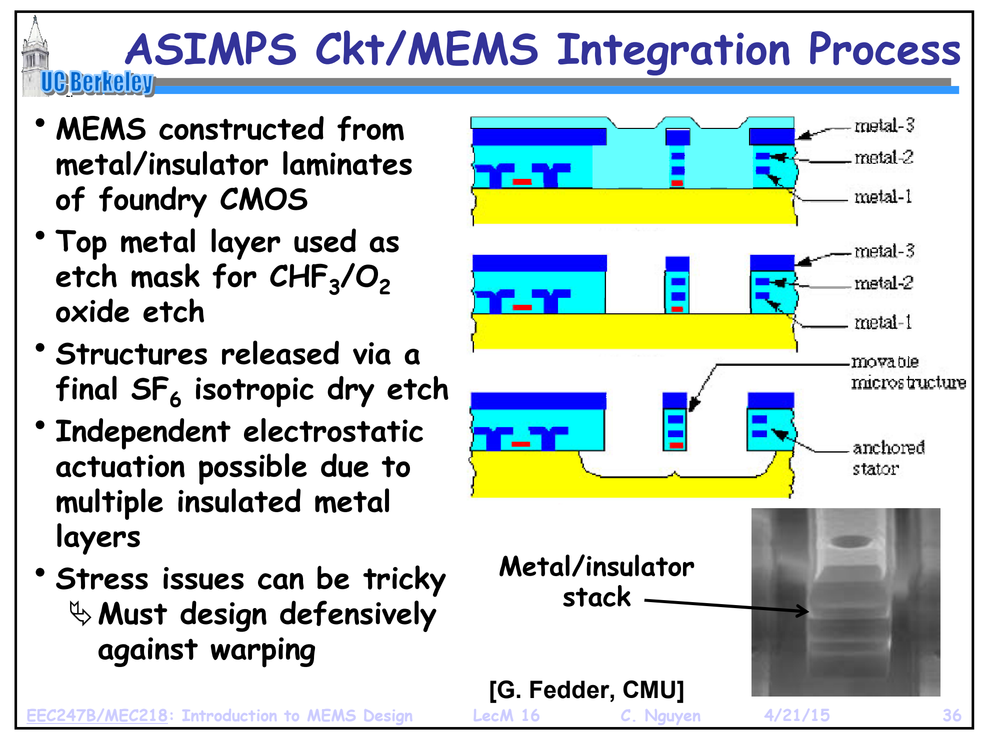
Copyright © 2016 Regents of the University of California



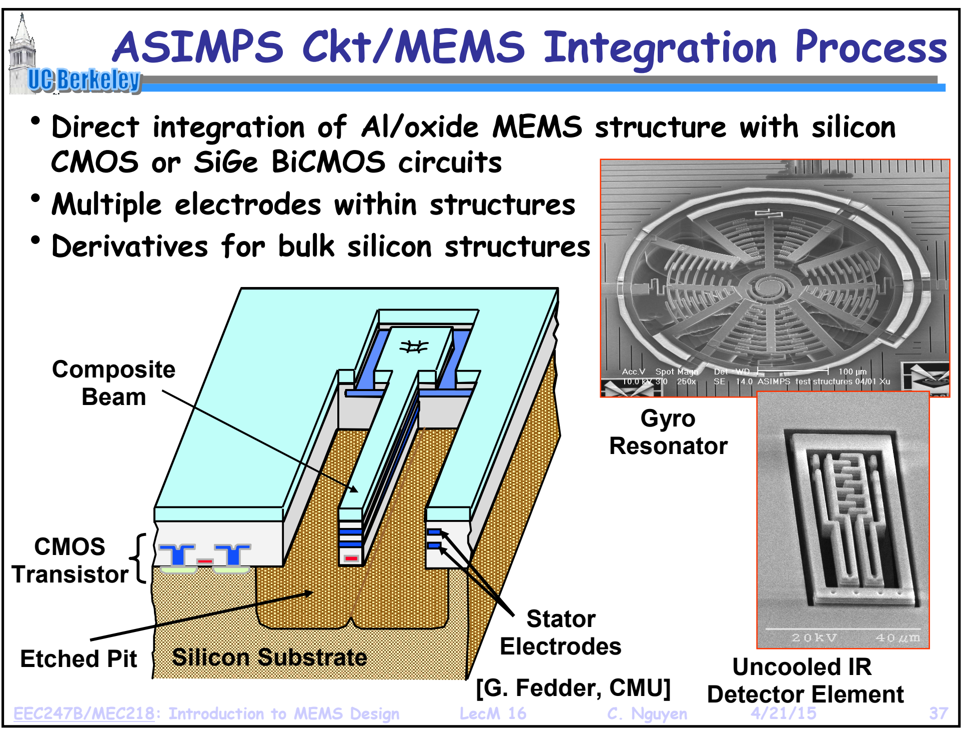


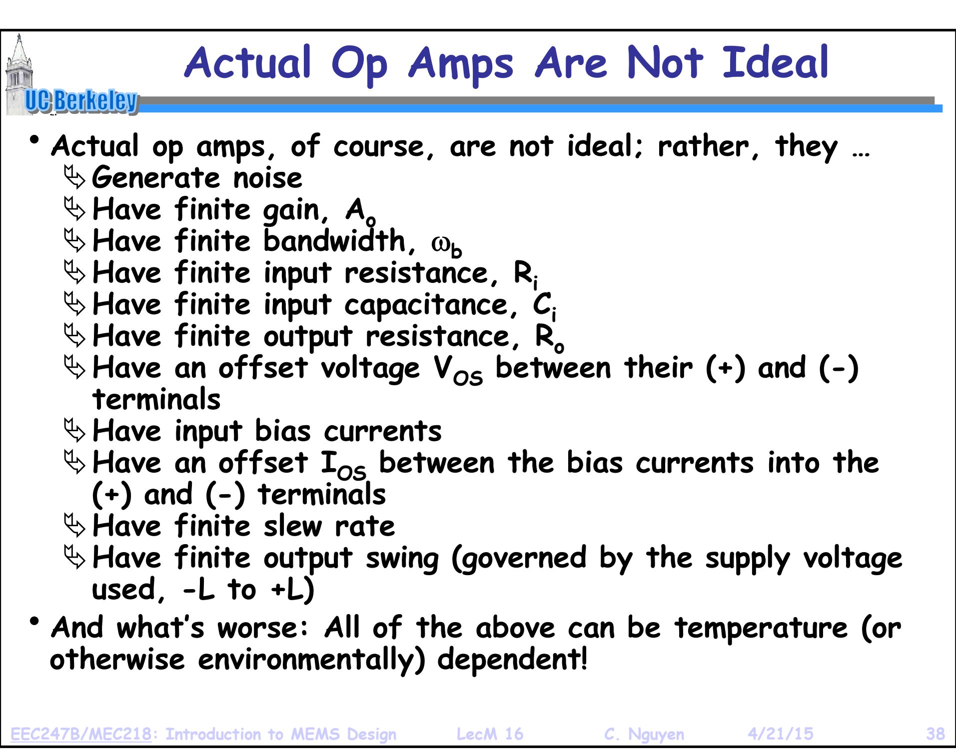
Copyright © 2016 Regents of the University of California



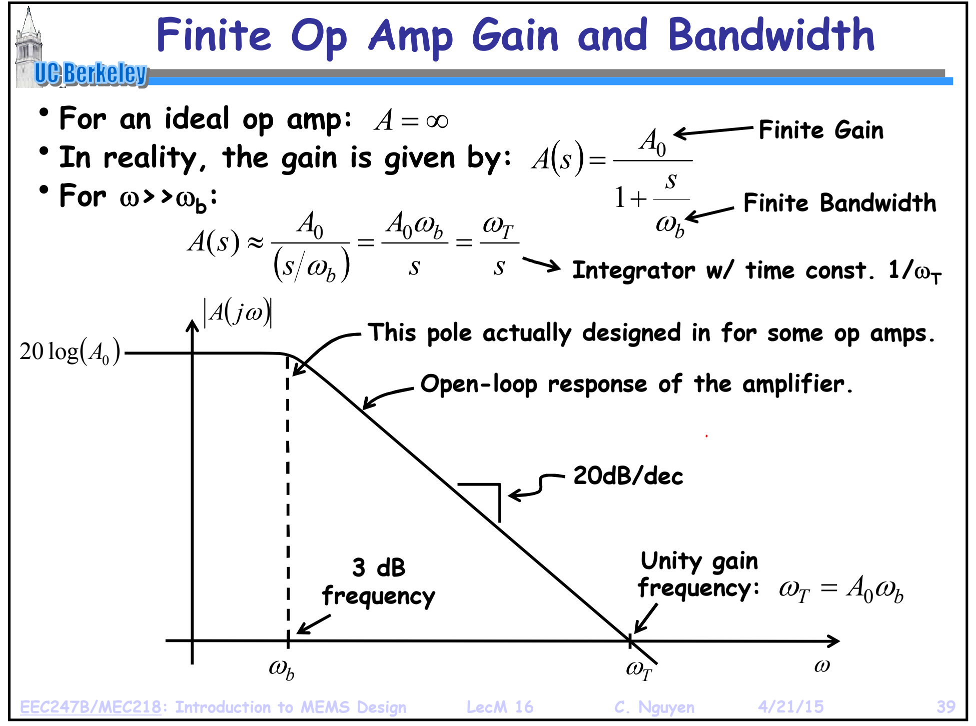


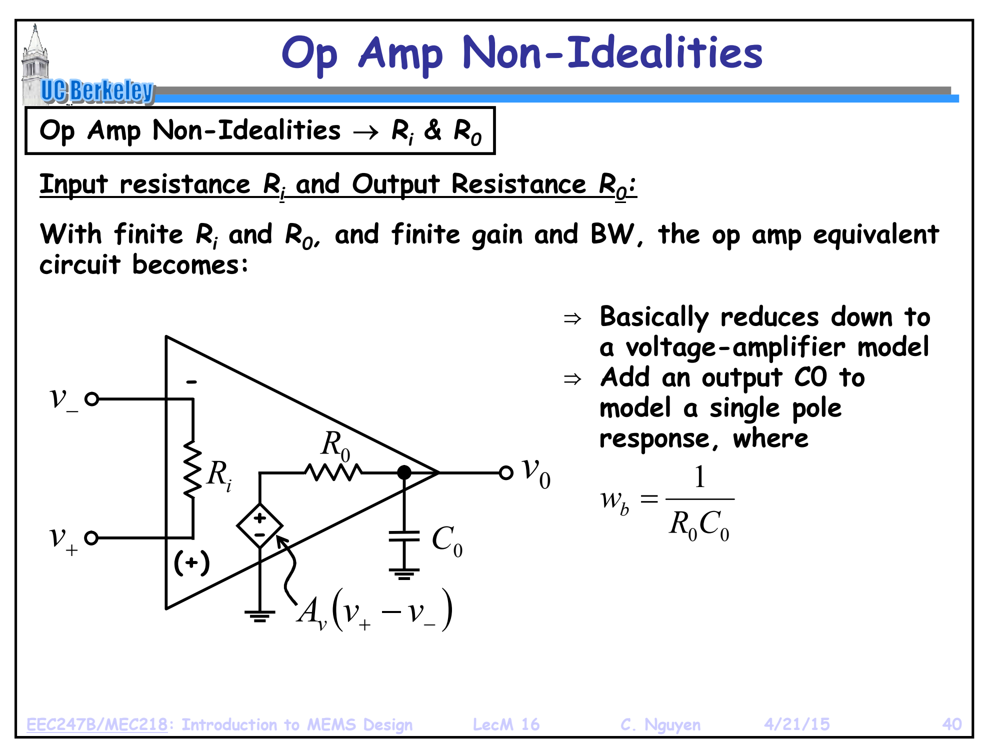
Copyright © 2016 Regents of the University of California



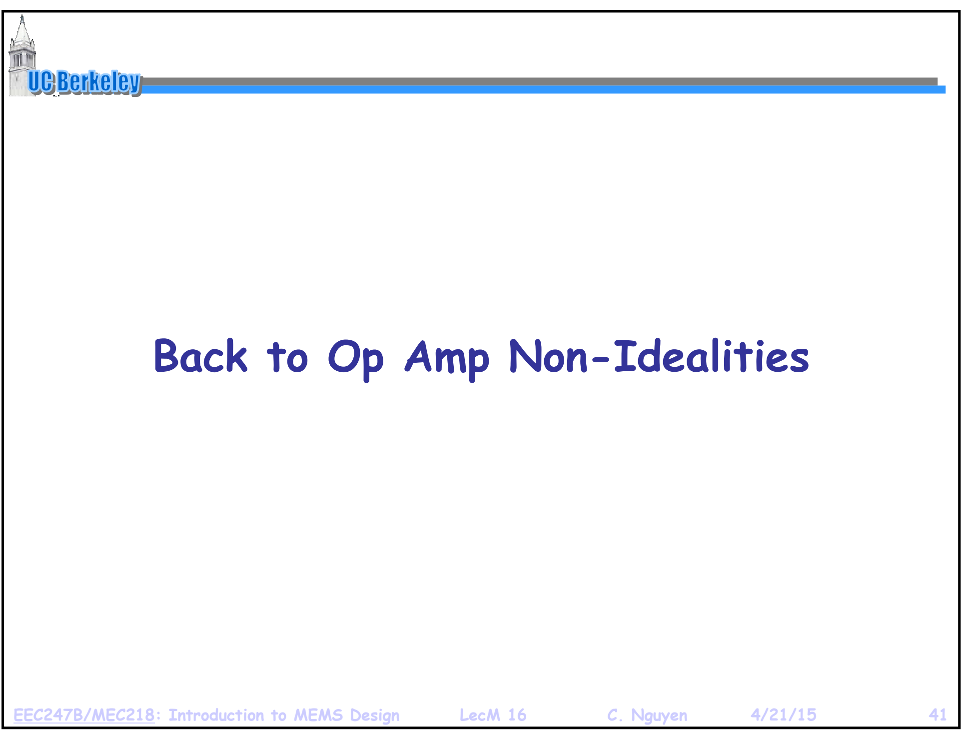


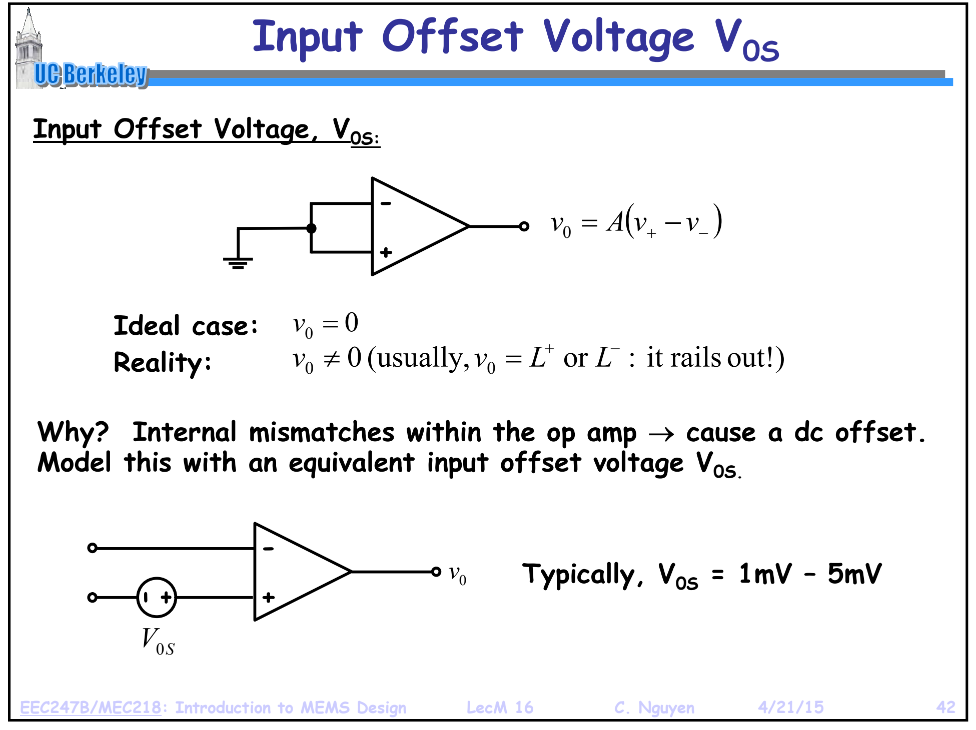
Copyright © 2016 Regents of the University of California



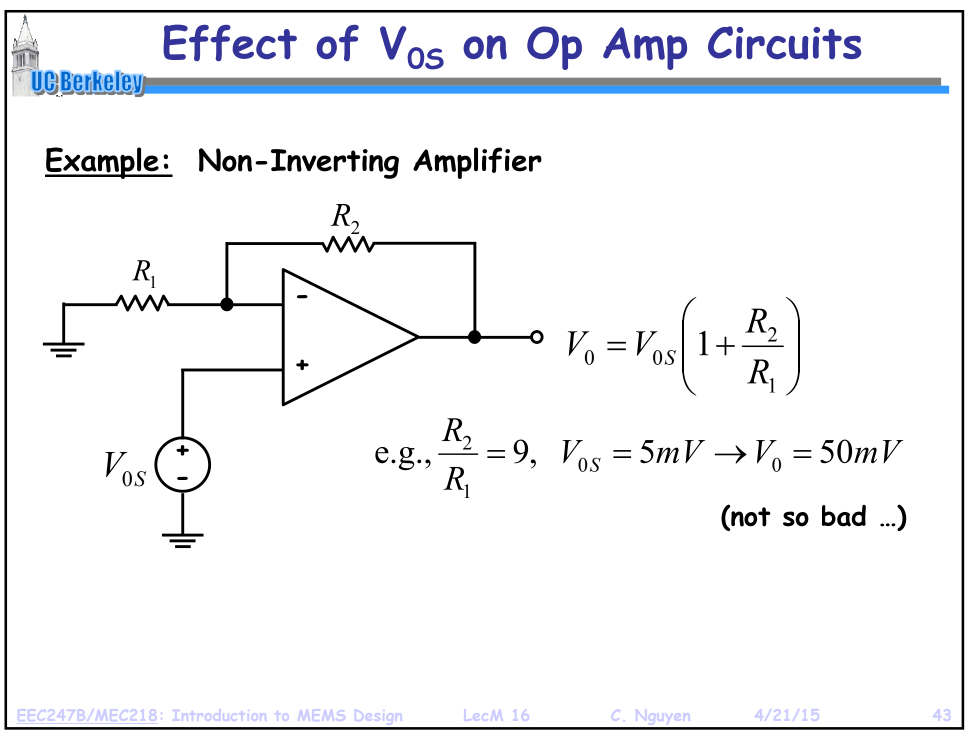


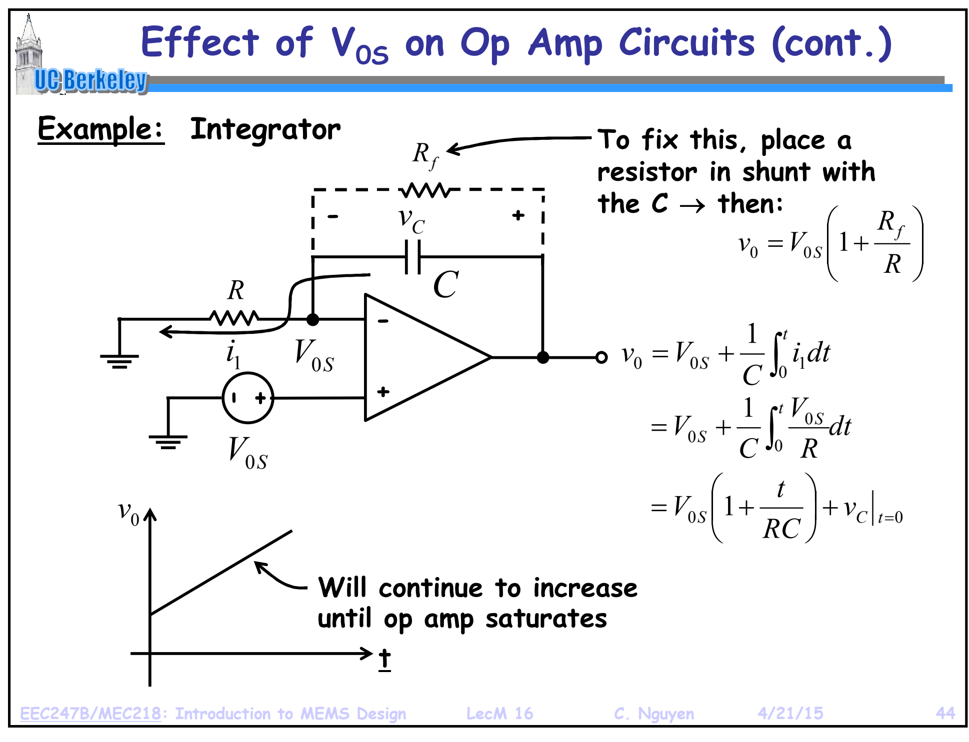
Copyright © 2016 Regents of the University of California





Copyright © 2016 Regents of the University of California





Copyright © 2016 Regents of the University of California