Lecture 7: Process Modules & Surface Micromachining
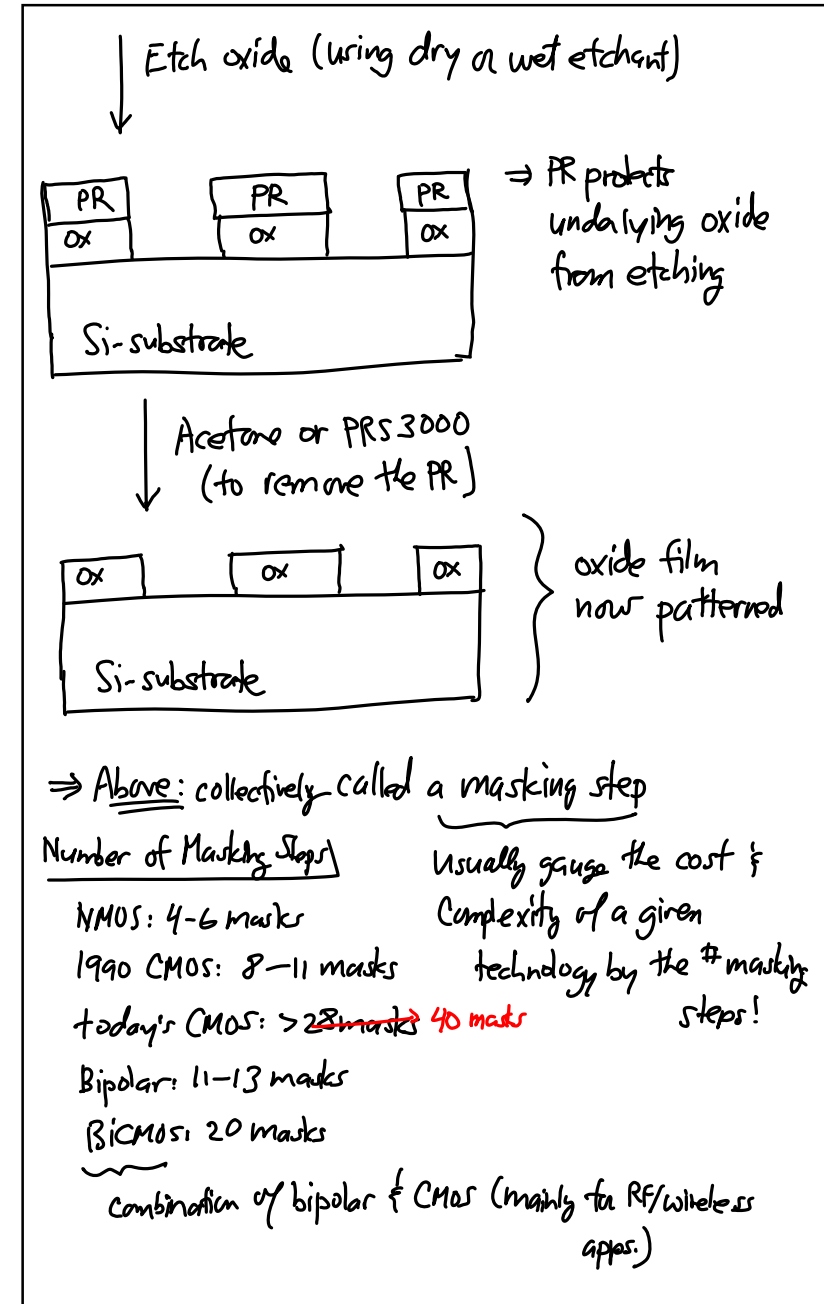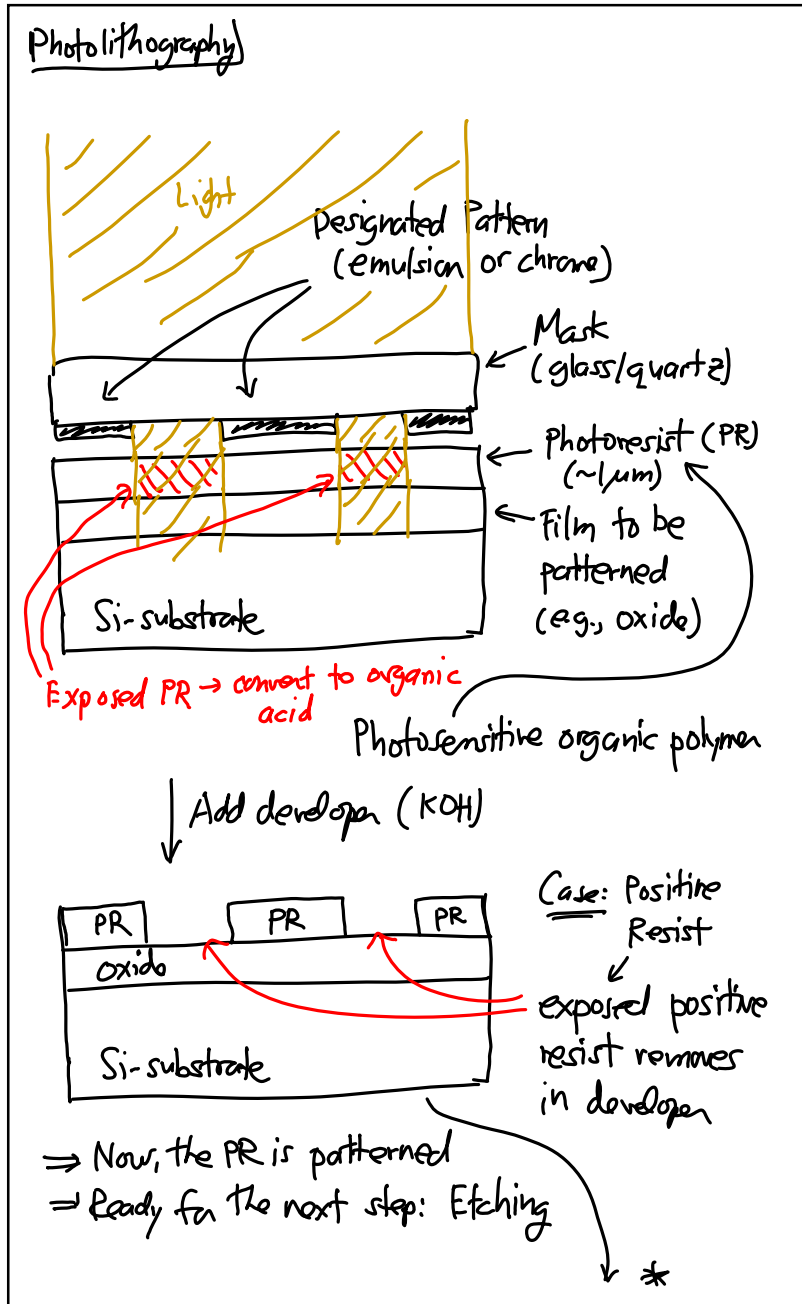- **Announcements:**
- **HW#1 due Tuesday, 2/14 at 10 a.m.**
- **Lecture Module 5 on Surface Micromachining online**
- **I will be traveling this Thursday; look for a video lecture to make this up**
- ---------------------------------------
- **Today:**
- **Senturia, Chpt. 3; Jaeger, Chpt. 2, 3, 6**
    - ↳ Example MEMS fabrication processes
    - ↳ Photolithography
    - ↳ Etching
    - ↳ Oxidation
    - ↳ **Film Deposition**
    - ↳ **Ion Implantation**
    - ↳ **Diffusion**
- **Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: "Surface Micromachining for Microelectromechanical Systems"**
- **Lecture Topics:**
    - ↳ **Polysilicon surface micromachining**
    - ↳ **Stiction**
    - ↳ **Residual stress**
    - ↳ **Topography issues**
    - ↳ **Nickel metal surface micromachining**
    - ↳ **3D "pop-up" MEMS**
    - ↳ **Foundry MEMS: the "MUMPS" process**
    - ↳ **The Sandia SUMMIT process**
- ---------------------------------------
- **Last Time:**
- **Ended up at physical deposition … continue with this**
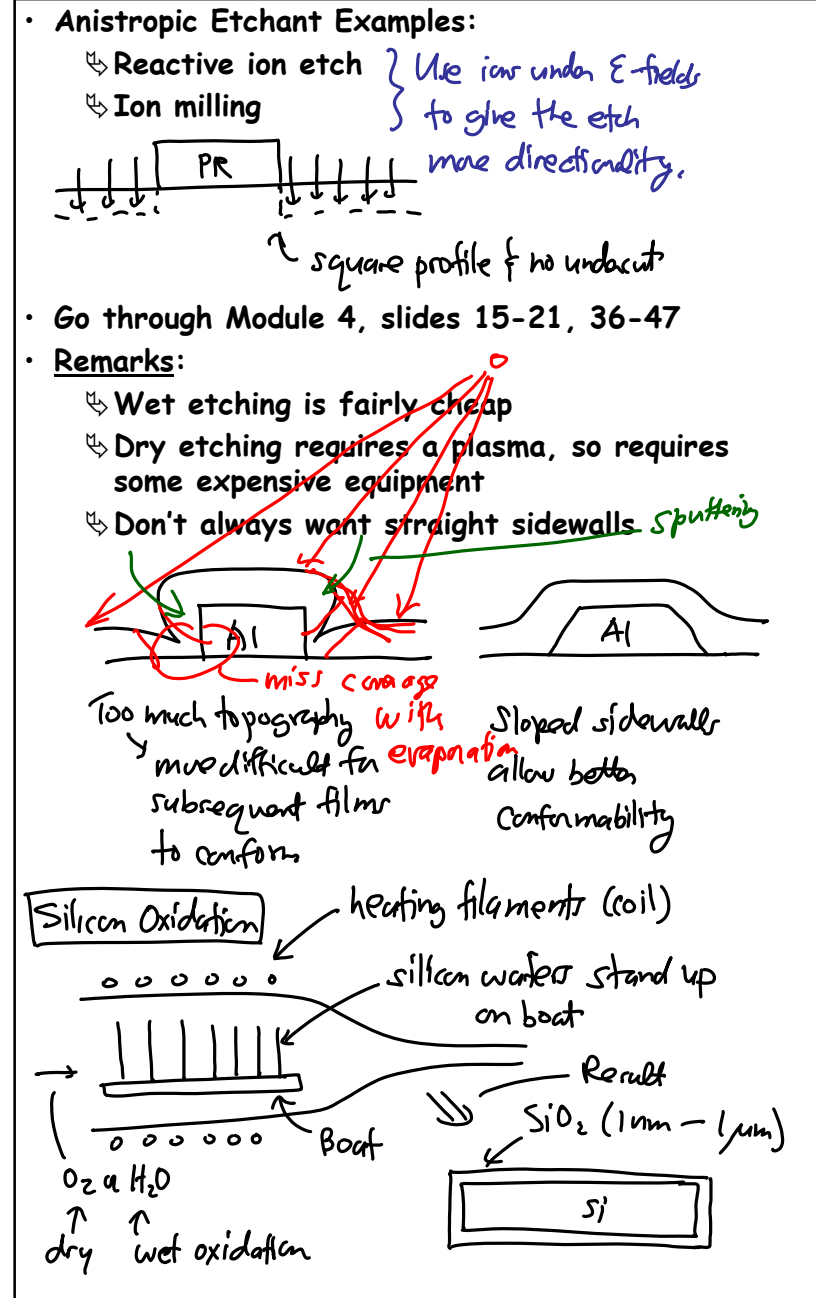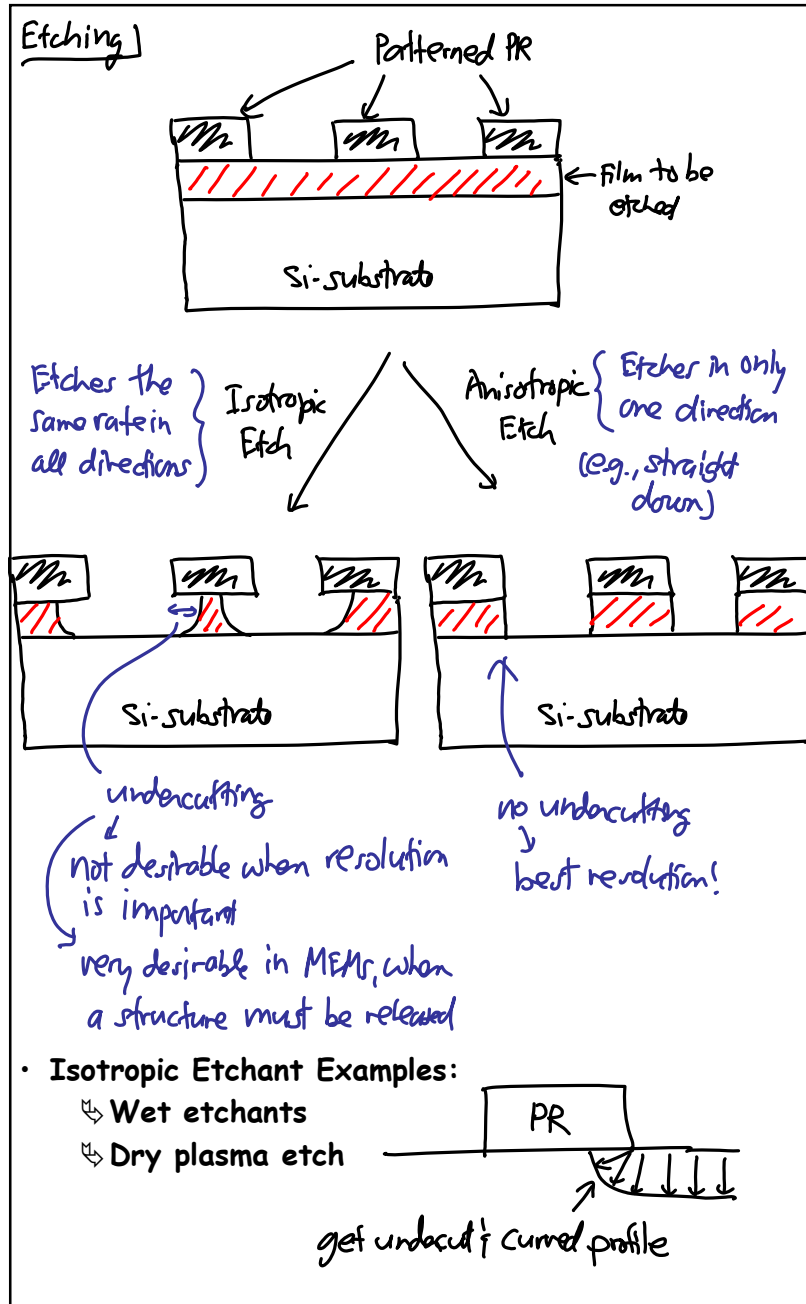
Process Module Overview:
- **Lecture Topics:**
    - ↳ Photolithography
    - ↳ Etching
    - ↳ Oxidation
    - ↳ Film Deposition
    - ↳ Ion Implantation
    - ↳ Diffusion
- **As stated earlier, this is now assumed knowledge**
- **I will gloss over this material to review it a bit, but will not go over it in detail**
- **You can watch my lectures from EE245, Fall 2012, on the Webcast Berkeley site for more in depth coverage: Lectures 6-8**
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Process Modules
⇒ there are actually only a few basic modules used for processing
↓
Combination of these in the correct sequence yields an integrated circuit technology that provides transistors, MEMs, nanodevices, etc.

⇒ For each module, need to understand:
① Physics and engineering of each module in detail.
② Interactions between modules.
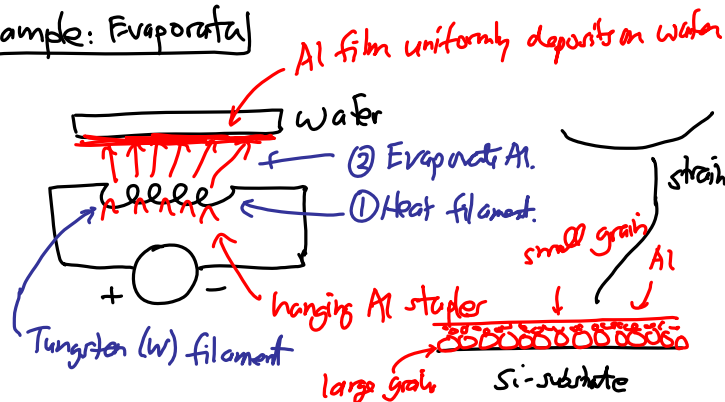③ The effect of each module on the finished device.

Photolithography)

Light

Designated Pattern
(emulsion or chrome)

Mask
(glass/quartz)

Photoresist (PR)
(~1μm)

Film to be
patterned
(e.g., oxide)

Si-substrate

Exposed PR → convert to organic
acid

Photosensitive organic polymer

↓ Add developer (KOH)

PR   PR   PR
Oxide

Si-substrate

Case: Positive
Resist

↓

exposed positive
resist removes
in developer

⇒ Now, the PR is patterned
⇒ Ready for the next step: Etching

*

↓ Etch oxide (using dry or wet etchant)

PR   PR   PR
Ox   Ox   Ox

Si-substrate

⇒ PR protects
underlying oxide
from etching

↓ Acetone or PRS 3000
(to remove the PR)

Ox   Ox   Ox

Si-substrate

} oxide film
now patterned

⇒ **Above**: collectively called a masking step

Number of Masking Steps)

NMOS: 4-6 masks
1990 CMOS: 8-11 masks
today's CMOS: >28 masks 40 masks
Bipolar: 11-13 masks
BiCMOS: 20 masks

Usually gauge the cost &
Complexity of a given
technology by the # masking
steps!

combination of bipolar & CMOS (mainly for RF/wireless
apps.)

Etching

Patterned PR

← Film to be etched

Si-substrate

Etches the same rate in all directions ⟩ Isotropic Etch

Anisotropic Etch ⟨ Etches in only one direction (e.g., straight down)

Si-substrate

Si-substrate

undercutting
not desirable when resolution is important
very desirable in MEMs, when a structure must be released

no undercutting
best resolution!

- Isotropic Etchant Examples:
  ↳ Wet etchants
  ↳ Dry plasma etch

PR

get undercut & curved profile

- Anistropic Etchant Examples:
  ↳ **Reactive ion etch** ⟩ Use ions under E-fields to give the etch more directionality.
  ↳ **Ion milling**

PR

square profile & no undercut

- Go through Module 4, slides 15-21, 36-47
- **Remarks**:
  ↳ **Wet etching is fairly cheap**
  ↳ **Dry etching requires a plasma, so requires some expensive equipment**
  ↳ **Don't always want straight sidewalls** sputtering

Al

Al

miss coverage

Too much topography with evaporation more difficult for subsequent films to conform

Sloped sidewalls allow better conformability

Silicon Oxidation — heating filaments (coil)

silicon wafers stand up on boat

Result
SiO₂ (1nm – 1μm)

Boat

Si

O₂ a H₂O
↑ dry ↑ wet oxidation

- **Remarks**:
  - ↳ Uniformity can be better than 2% across the wafer from lot to lot
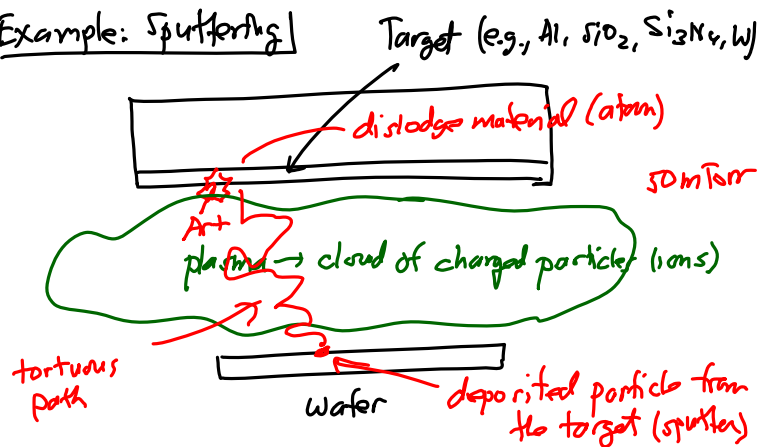 - ↳ Need to flow the O_2 fairly fast in order to minimize reactant losses from the first boat to the last one

Thin-Film Deposition:
- For deposition of films like Al (and other metals), SiO_2, Si_3N_4, and polysilicon
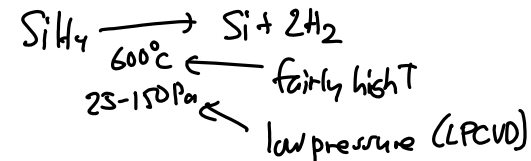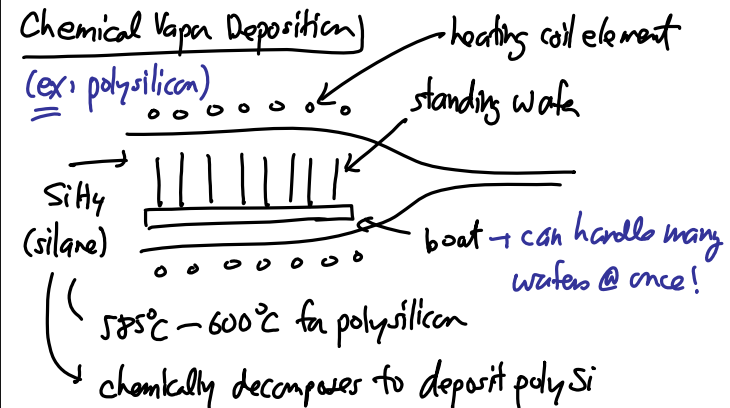- Deposition, not thermal growth

Example: Evaporation

Al film uniformly deposits on wafer

wafer

② Evaporate Al.

① Heat filament.

strain

small grain

Al

hanging Al stapler

Tungsten (W) filament

large grain

Si-substrate

Example: Sputtering

Target (e.g., Al, SiO_2, Si_3N_4, W)

dislodge material (atom)

50 mTorr

Ar+

plasma → cloud of charged particles (ions)

tortuous path
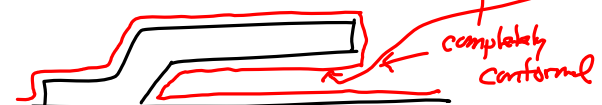
wafer

deposited particle from the target (sputter)

- Also, have chemical vapor deposition (CVD)
  - ↳ Chemical reaction involved in deposition of a given thin film
  - ↳ High temperature, but not nearly as high as often required for thermal growth

Chemical Vapor Deposition)

(ex, polysilicon)

heating coil element

standing wafer

SiH_4 (silane)

boat → can handle many wafers @ once!

585°C ~ 600°C for polysilicon

chemically decomposes to deposit poly Si

$$SiH_4 \xrightarrow[\substack{600°C \\ 25-150\,Pa}]{} Si + 2H_2$$

fairly high T

low pressure (LPCVD)

- **Remarks**:

  w/ high enough temperature, can even coat undersides

  - ↳ Lot's of materials can be deposited in a similar manner: polysilicon, SiO_2, Si_3N_4, tungsten
  - ↳ Compared to sputtering, CVD is less expensive since one can coat many wafers at once; sputtering generally does it one at a time
  - ↳ For higher temperature, CVD films are much more conformal than sputtered films

  completely conformal

- **Diffusion:**
- **Process of introducing dopants into selected areas on an IC**
- **Example:**

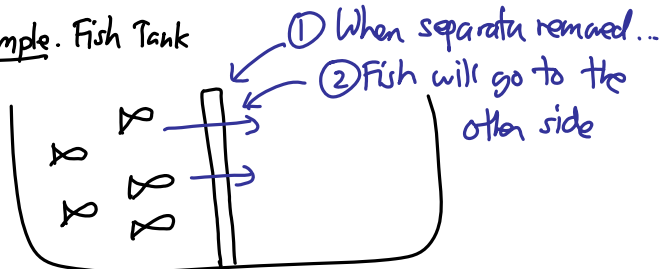diborane gas → B_2H_6 + O_2 @ high temperature ~ 800°C — 1200°C

p-type

n-Si substrate
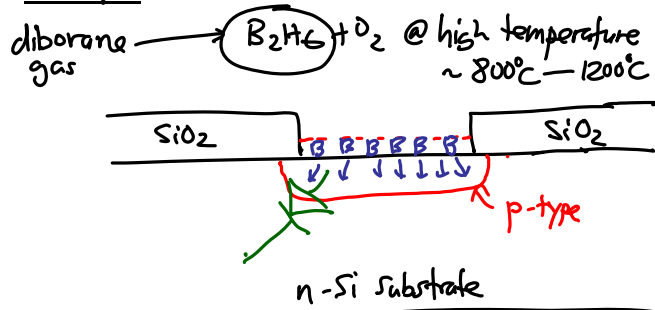
① Form borosilicate glass w/ high B concentration

② Boron diffuses in → this becomes p-type

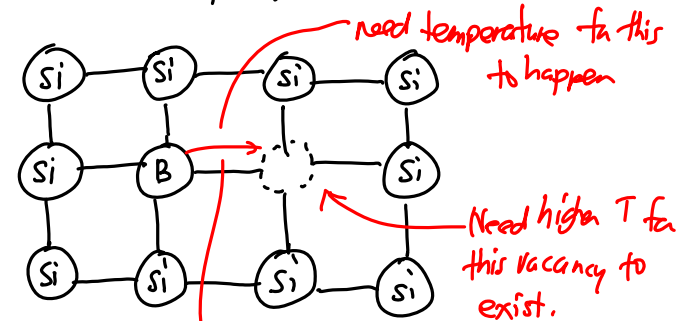⇒ diffusion requires:
① concentration gradient
② movement (velocity)

→ Example. Fish Tank

① When separator removed...
② Fish will go to the other side

highly concentrated

③ Until the concentration is the same on both sides

But they can't if they're dead!

It's similar for an impurity in silicon:

need temperature for this to happen

Need higher T for this vacancy to exist.

Just one mechanism for diffusion → we'll look at others, too

substitutional diffusion:
⇒ impurity moves along vacancies in the lattice
⇒ substitutes for a Si atom in the lattice

For movement to occur:
① Vacancies must exist.
② The B must have enough energy to move.

Both require high temperature!

must heat to induce diffusion of impurities in Si!
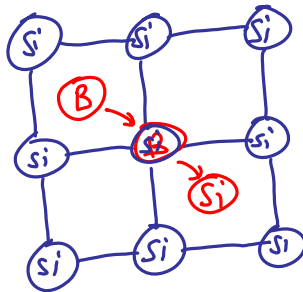
Definitions.

① Predeposition: diffusion w/ dopant source present
② Drive-in: diffusion in an inert ambient, e.g., N_2 w/ no dopant gases present

Ion Implantation

⇒ a more accurate way to introduce dopants before drive-in

B+ B+ B+

① Accelerate B+ ions into the Si-substrate

Masking layer (e.g., oxide n PR)

Si-substrate
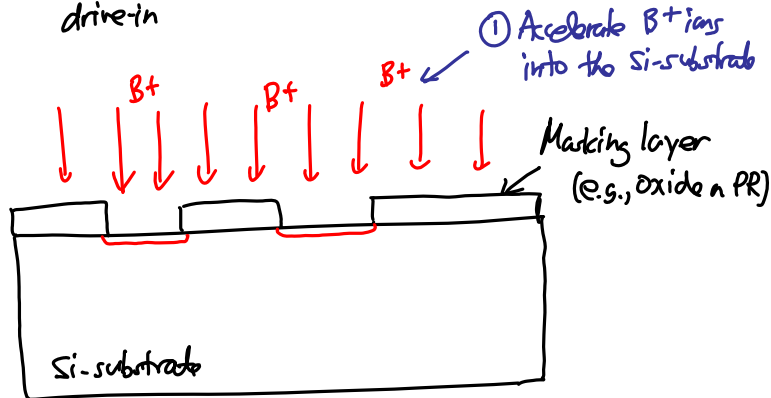
② B+ punches into the Si

③ Raise T to move the B into the lattice → only when it's in the lattice Is it active & can contribute to the doping level
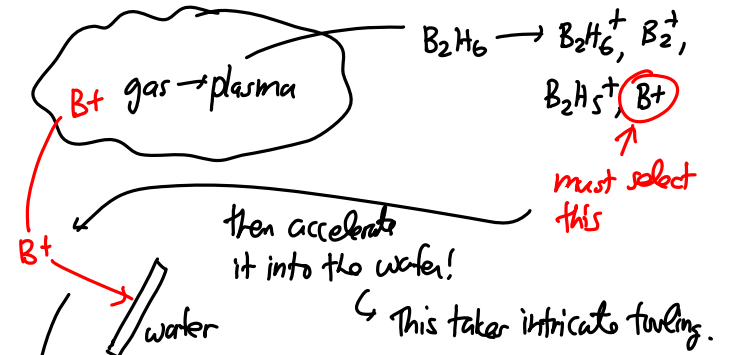
④ keep T up to drive the dopants in to the desired depth.

Advantages:
① accurate dose
② change depth by setting ion energy
③ no need for high temperature

Problem: COST!

An ion implanter is quite a sophisticated piece of equipment! → and expensive! (> $1 million)

B+ gas → plasma

$B_2H_6 \rightarrow B_2H_6^+, B_2^+,$
$B_2H_5^+, B^+$

must select this

B+

then accelerate it into the wafer!
↳ This takes intricate tooling.
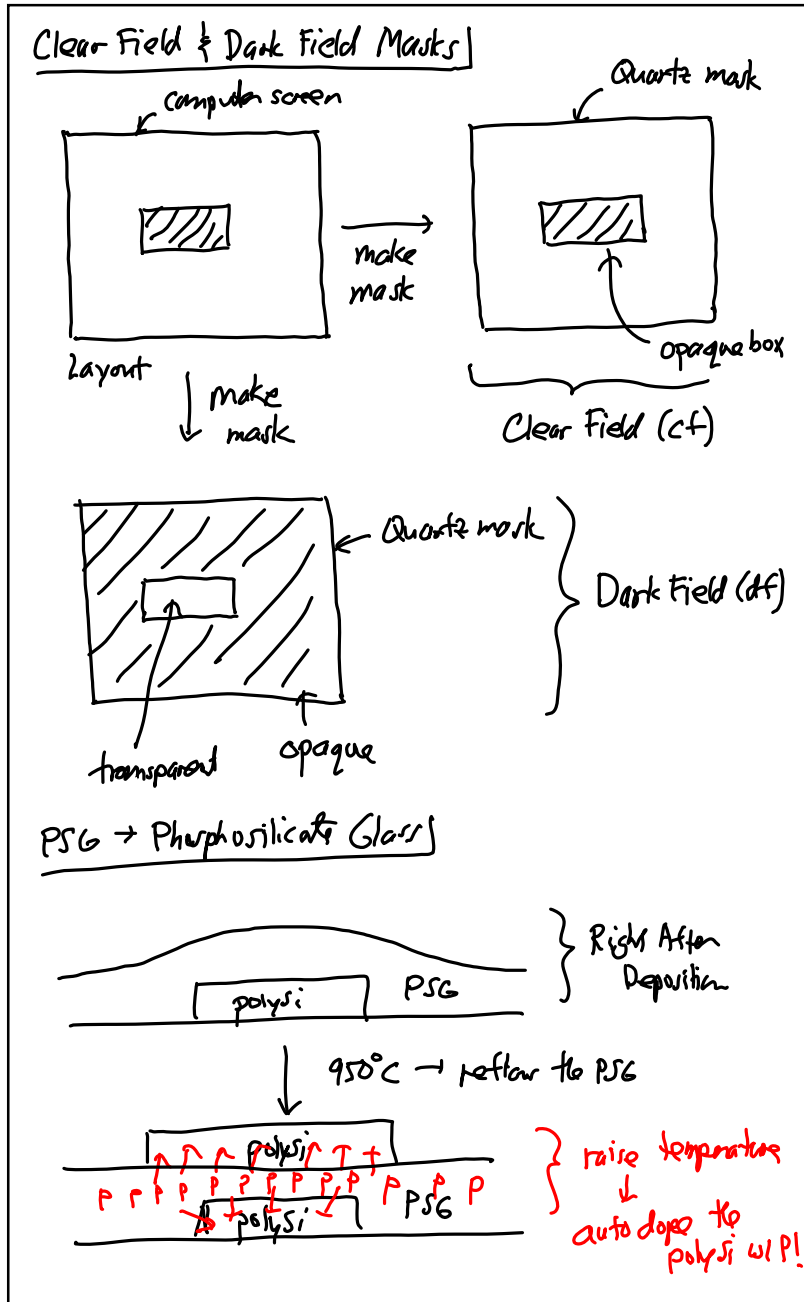
wafer

Energy Range: 20 keV – 100 keV

Penetration Depth: fraction of a μm
⇒ larger ions don't go as far as smaller (heavier ions penetrate shallower than smaller)

Dose: $10^{11} - 10^{15} \, cm^{-2}$

• Now, start going through Module 5 on Surface Micromachining

Clear Field & Dark Field Masks

computer screen

Quartz mask

Layout

make mask

make mask

Clear Field (cf)

opaque box

Quartz mask

} Dark Field (df)

transparent   opaque

PSG → Phosphosilicate Glass

polysi   PSG

} Right After Deposition

950°C → reflow the PSG

polysi

P P P P P P P P P P P P P P P P PSG P

polysi

} raise temperature
↓
auto dope the polysi w/ P!

- • **Straight or Sloped Sidewalls**:
- • **Often want sloped sidewalls in order to reduce the sharpness of corners**
  - ↳ **Easier to deposit over**
  - ↳ **Sharp corners concentrate stresses**
  - ↳ **High stress can weaken structures creating a reliabilty concern**
  - ↳ **High stress can dissipate energy, lowering Q**
- • **When you want straight sidewalls (e.g., for lateral electrostatic drive), use a hard mask**
  - ↳ **PR can't last for thick structures**
  - ↳ **A hard mask suppresses angle transfer**

Etching Sloped Sidewalls

etching after slices of time

PR   PR

SiO₂

↖ polySi Contact Pad

Substrate

⇒ to get sloped sidewalls

sloped PR via overexposure during litho

PR   PR

SiO₂

↖ polySi Contact Pad

Substrate