

UC Berkeley

The Sandia SUMMIT Process

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 61

UC Berkeley

Sandia's SUMMIT V

- **SUMMIT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process**
 - ↪ Five-layer polysilicon surface micromachining process
 - ↪ One electrical interconnect layer & 4 mechanical layers
 - ↪ Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
 - ↪ 14 masks

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 62

UC Berkeley

SUMMIT V Layer Stack

- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 63

UC Berkeley

Chemical Mechanical Polishing (CMP)

- Used to planarize the top surface of a semiconductor wafer or other substrate
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad
 - ↪ Wafer and pad are pressed together
 - ↪ Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 64

CMP: Not the Same as Lapping

Lapping

- Lapping is merely the removal of material to flatten a surface without selectivity
- Everything is removed at approximately the same rate

Chemical Mechanical Polishing

- CMP is selective to certain films, and not selective to others

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 65

Actual SUMMiT Cross-Section

- No CMP until after the first three polySi layers
- 1 μm mmpoly1 and 1.5 μm mmpoly2 can be combined to form a 2.5 μm polysilicon film
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions

EE C245: Introduction to MEMS Design LecM 5 C. Nguyen 8/20/09 66