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EE C247B - ME C218 Introduction to MEMS Design Spring 2018

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Lecture Module 6: Bulk Micromachining

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Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
 - ↪ Bulk Micromachining
 - ↪ Anisotropic Etching of Silicon
 - ↪ Boron-Doped Etch Stop
 - ↪ Electrochemical Etch Stop
 - ↪ Isotropic Etching of Silicon
 - ↪ Deep Reactive Ion Etching (DRIE)

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Bulk Micromachining

- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
 - ↪ Isotropic vs. anisotropic
 - ↪ Reaction-limited
 - Etch rate dep. on temp.
 - ↪ Diffusion-limited
 - Etch rate dep. on mixing
 - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
 - ↪ Desired shape
 - ↪ Etch depth and uniformity
 - ↪ Surface roughness (e.g., sidewall roughness after etching)
 - ↪ Process compatibility (w/ existing layers)
 - ↪ Safety, cost, availability, environmental impact

	Wet etch	Plasma (dry) etch
Isotropic		
Anisotropic		

adsorption surface reaction desorption

slowest step controls rate of reaction

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Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
 - ↪ Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm²)
 - ↪ Young's Modulus near that of stainless steel
 - ↪ {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
 - ↪ Mechanical properties uniform, no intrinsic stress
 - ↪ Mechanical integrity up to 500°C
 - ↪ Good thermal conductor
 - ↪ Low thermal expansion coefficient
 - ↪ High piezoresistivity

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Anisotropic Etching of Silicon

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- Etching of Si w/ KOH

$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4e^-$$

$$4\text{H}_2\text{O} + 4e^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
- Crystal orientation dependent etch rates
 - {110}:{100}:{111}=600:400:1
 - {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
 - {111} plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
 - {111} forms protective oxide
 - {111} smoother than other crystal planes → good for optical MEMS (mirrors)

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Anisotropic Etching of Silicon

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- Deposit nitride:
 - Target = 100nm
 - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
 - RIE using SF₆
 - Remove PR in PRS2000
- Etch the silicon
 - Use 1:2 KOH:H₂O (wt.), stirred bath @ 80°C
 - Etch Rates:
 - (100) Si → 1.4 μm/min
 - Si₃N₄ → ~ 0 nm/min
 - SiO₂ → 1-10 nm/min
 - Photoresist, Al → fast
 - Micromasking by H₂ bubbles leads to roughness
 - Stir well to displace bubbles
 - Can also use oxidizer for (111) surfaces
 - Or surfactant additives to suppress bubble formation

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Silicon Wafers

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[Maluf]

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Silicon Crystallography

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Miller Indices (h k l):

- Planes
 - Reciprocal of plane intercepts with axes
 - e.g., for (110), intercepts: (x,y,z) = (1,1,∞); reciprocals: (1,1,0) → (110)
 - (unique), {family}
- Directions
 - One endpoint of vector @ origin
 - [unique], <family>

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Determining Angles Between Planes

• The angle between vectors $[abc]$ and $[xyz]$ is given by:

$$ax + by + cz = |(a, b, c)| \cdot |(x, y, z)| \cdot \cos \theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1} \left[\frac{ax + by + cz}{|(a, b, c)| \cdot |(x, y, z)|} \right]$$

- For $\{100\}$ and $\{110\} \rightarrow 45^\circ$
- For $\{100\}$ and $\{111\} \rightarrow 54.74^\circ$
- For $\{110\}$ and $\{111\} \rightarrow 35.26^\circ, 90^\circ,$ and 144.74°

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Silicon Crystal Origami

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]

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Undercutting Via Anisotropic Si Etching

- Concave corners bounded by $\{111\}$ are not attacked
- ... but convex corners bounded by $\{111\}$ are attacked
- Two $\{111\}$ planes intersecting now present two dangling bonds \rightarrow no longer have just one dangling bond \rightarrow etch rate fast
- Result: can undercut regions around convex corners

Concave corner

Convex corner

Suspended Beam

[Ristic]

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Corner Compensation

- Protect corners with "compensation" areas in layout
- Below: Mesa array for self-assembly structures [Smith 1995]

Mask pattern

Shaded regions are the desired result

Groove W_1

2α

$d = \text{Depth of groove}$

Mask pattern

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Other Anisotropic Silicon Etchants

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
 - ↳ Etch rate (100) = 0.5-1.5 μm/min
 - ↳ Attacks Al
 - Si-doped Al safe & IC compatible
 - ↳ Etch ratio (100)/(111) = 10-35
 - ↳ Etch masks: SiO₂, Si₃N₄ ~ 0.05-0.25 nm/min
 - ↳ Boron doped etch stop, up to 40× slower
- EDP (115°C)
 - ↳ Carcinogenic, corrosive
 - ↳ Etch rate (100) = 0.75 μm/min
 - ↳ Al may be etched
 - ↳ R(100) > R(110) > R(111)
 - ↳ Etch ratio (100)/(111) = 35
 - ↳ Etch masks: SiO₂ ~ 0.2 nm/min, Si₃N₄ ~ 0.1 nm/min
 - ↳ Boron doped etch stop, 50× slower

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Boron-Doped Etch Stop

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Boron-Doped Etch Stop

- Control etch depth precisely with boron doping (p++)
 - ↳ [B] > 10²⁰ cm⁻³ reduces KOH etch rate by 20-100×
 - ↳ Can use gaseous or solid boron diffusion
 - ↳ Recall etch chemistry:

$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
 - ↳ At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH⁻
- **Result:**
 - ↳ Beams, suspended films
 - ↳ 1-20 μm layers possible

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Ex: Micronozzle

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

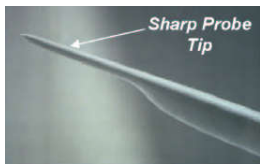
1. Pattern mask
2. Etch circle in p++
3. Mask front side
4. Anisotropic etch

[Maluf]

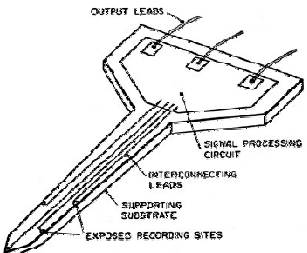
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Ex: Microneedle

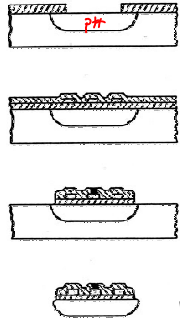
- Below: micro-neurostimulator
 - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan



Sharp Probe Tip



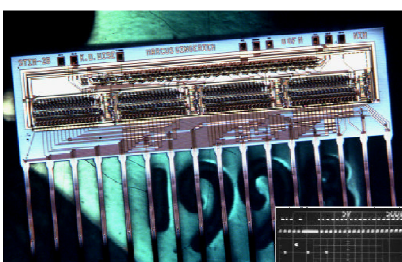
Multi-Channel Recording Array Structure



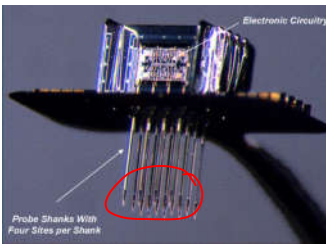
- Selectively diffuse p++ into substrate
- Deposit interconnect pattern and insulate conductors
- Pattern dielectric and metallize recording sites
- Dissolve away the wafer (no mask needed)

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Ex: Microneedles (cont.)



64-Site Multiplexed Stimulating Array



Probe Shanks With Four Sites per Shank

[Wise, U. of Michigan]

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400 μm site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

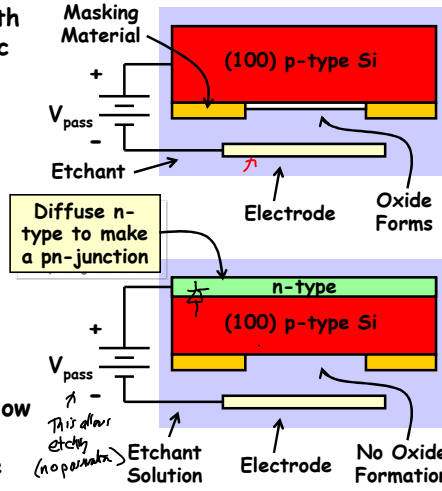
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Electrochemical Etch Stop

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Electrochemical Etch Stop

- When silicon is biased with a sufficiently large anodic potential relative to the etchant \rightarrow get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented \rightarrow no oxide growth, and etching can proceed
 - Can prevent current flow by adding a reverse-biased diode structure



Masking Material

(100) p-type Si

Electrode

Oxide Forms

Diffuse n-type to make a pn-junction

n-type

(100) p-type Si

Electrode

No Oxide Formation

Etchant Solution

This allows etching (no passivation)

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Electrochemical Etch Stop

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- Electrochemical etch stop
 - n-type epitaxial layer grown on p-type wafer forms p-n junction diode
 - $V_p > V_n \rightarrow$ electrical conduction (current flow)
 - $V_p < V_n \rightarrow$ reverse bias current (very little current flow)
- Passivation potential: potential at which thin SiO_2 film forms
 - different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- Setup:
 - p-n diode in reverse bias
 - p-substrate floating \rightarrow etched
 - n-layer above passivation potential \rightarrow not etched

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Electrochemical Etching of CMOS

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- N-type Si well with circuits suspended f/ SiO_2 support beam
- Thermally and electrically isolated
- If use TMAH etchant, doped (w/Si) Al bond pads safe

[Reay, et al. (1994)]
[Kovacs Group, Stanford]

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Ex: Bulk Micromachined Pressure Sensors

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- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection $< 1 \mu\text{m}$

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Ex: Pressure Sensors

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- Below: catheter tip pressure sensor [Lucas NovaSensor]
 - Only $150 \times 400 \times 900 \mu\text{m}^3$

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Deep Reactive-Ion Etching (DRIE)

The Bosch process:

- Inductively-coupled plasma
- Etch Rate: 1.5-4 $\mu\text{m}/\text{min}$
- Two main cycles in the etch:
 - Etch cycle** (5-15 s): SF_6 (SF_x^+) etches Si
 - Deposition cycle**: (5-15 s): C_4F_8 deposits fluorocarbon protective polymer (CF_2^-)_n
- Etch mask selectivity:
 - $\text{SiO}_2 \sim 200:1$
 - Photoresist $\sim 100:1$
- Issue**: finite sidewall roughness
 - scalloping $< 50 \text{ nm}$
- Sidewall angle: $90^\circ \pm 2^\circ$

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DRIE Issues: Etch Rate Variance

- Etch rate is diffusion-limited and drops for narrow trenches
 - Adjust mask layout to eliminate large disparities
 - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

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DRIE Issues: "Footing"

- Etch depth precision
 - Etch stop: buried layer of SiO_2
 - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- Problem**: Lateral undercut at Si/ SiO_2 interface \rightarrow "footing"
 - Caused by charge accumulation at the insulator

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Recipe-Based Suppression of "Footing"

- Use **higher process pressure** to reduce ion charging [Nozawa]
 - High operating pressure \rightarrow concentration of (-) charge increases and can neutralize (+) surface charge
 - Issue**: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe** to reduce overetching [Schmidt]
 - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
 - Issue**: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
 - Low frequency \rightarrow more ions with low directionality and kinetic energy \rightarrow neutralizes (-) potential barrier at trench entrance
 - Allows e^- 's to reach the trench base and neutralize (+) charge \rightarrow maintain charge balance inside the trench

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Metal Interlayer to Prevent "Footing"

Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial) (f) Silicon Thinning
(b) Preparatory trenches (g) Photolithography 2
(c) Metal interlayer deposition (h) DRIE
(d) Lift-off (remove PR) (i) Remove metal interlayer
(e) Anodic Bonding (j) Metallize

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Footing Prevention (cont.)

- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach

[Kim, Stanford]

No metal interlayer: Footing, Local damages, Pre trench (cavity)

No footing: Damage free!

With metal interlayer

[Kim, Seoul Nat. Univ.]

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DRIE Examples

High aspect-ratio gear Tunable Capacitor [Yao, Rockwell]

Microgripper [Keller, MEMS Precision Instruments]

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Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride (XeF_2)
 $2\text{XeF}_{2(g)} + \text{Si}_{(s)} \rightarrow 2\text{Xe}_{(g)} + \text{SiF}_{4(g)}$
- Set-up:
 - Xe sublimates at room T
 - Closed chamber, 1-4 Torr
 - Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 $\mu\text{m}/\text{min}$, isotropic
- Etch masks: photoresist, SiO_2 , Si_3N_4 , Al, other metals
- Issues:
 - Etched surfaces have granular structure, 10 μm roughness
 - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

Xactix XeF_2 Etcher

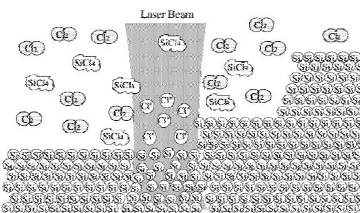
Inductor w/ no substrate [Pister]

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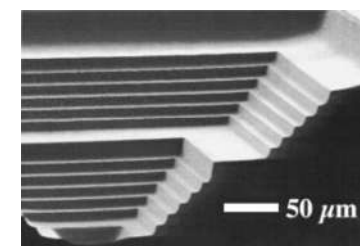
Laser-Assisted Chemical Etching

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- Laser creates Cl radicals from $\text{Cl}_2 \rightarrow$ reaction forms SiCl_2
- Etch rate: $100,000 \mu\text{m}^3/\text{s}$
 - Takes 3 min. to etch $500 \times 500 \times 125 \mu\text{m}^3$ trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file



- At right:**
 - Laser assisted etching of a $500 \times 500 \mu\text{m}^2$ terraced silicon well
 - Each step is $6 \mu\text{m}$ -deep



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Wafer Bonding

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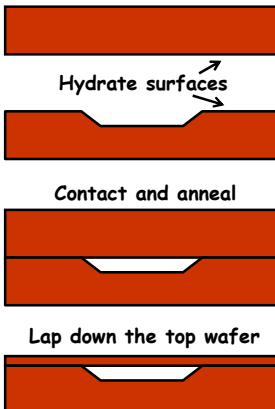
Wafer Bonding

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Fusion Bonding

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- Two ultra-smooth ($<1 \text{ nm}$ roughness) wafers are bonded without adhesives or applied external forces
- Procedure:**
 - Prepare surfaces: must be smooth and particle-free
 - Clean & hydrate: O_2 plasma, hydration, or HF dip
 - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
 - Anneal at $600\text{-}1200^\circ\text{C}$ to bring the bond to full strength
- Result:** a bond as strong as the silicon itself!



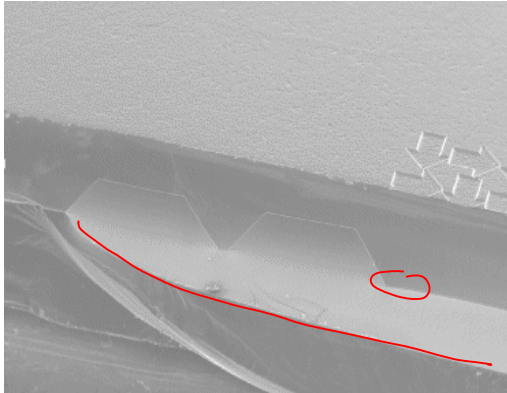
Works for Si-to-Si bonding and Si-to-SiO₂ bonding

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Fusion Bonding Example

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- Below:** capacitive pressure sensor w/ fusion-bonded features



work problem!
no bonding!

[Univ. of Southampton]

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Anodic Bonding

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- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
 - Press Si and glass together
 - Elevate temperature: 180-500°C
 - Apply (+) voltage to Si: 200-1500V
 - (+) voltage repels Na⁺ ions from the glass surface
 - Get net (-) charge at glass surface
 - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
 - Current drops to zero when bonding is complete

The schematic shows a Silicon (Si) wafer on top of a Glass (Pyrex) substrate, with an Electrode (Elec) plate on the glass. Arrows indicate the flow of electrons (e⁻) from the Si to the glass and Na⁺ ions from the glass to the Si. The graph below shows the process parameters over time: Temperature rises to 400°C, Pressure is applied (1000 mbar), Voltage is applied (800 V), and Current peaks at 10 mA before dropping to zero.

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Anodic Bonding (cont.)

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- Advantage:** high pressure of electrostatic attraction smooths out defects
- Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N₂ @ 1000 mbar

The four images show the bonding process: 1. after 5 sec (Only center bond pin active), 2. after 20 sec (All bond pins active), 3. after 2.5 min (Bond front spreads), 4. after 8 min (Bond 98% completed).

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Metal Layer Bonding

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- Pattern seal rings and bond pads photolithographically
- Eutectic bonding**
 - Uses eutectic point in metal-Si phase diagrams to form silicides
 - Au and Si have eutectic point at 363°C
 - Low temperature process
 - Can bond slightly rough surfaces
 - Issue:** Au contamination of CMOS
- Solder bonding**
 - PbSn (183°C), AuSn (280°C)
 - Lower-T process
 - Can bond very rough surfaces
 - Issue:** outgassing (not good for encapsulation)
- Thermocompression**
 - Commonly done with electroplated Au or other soft metals
 - Room temperature to 300°C
 - Lowest-T process
 - Can bond rough surfaces with topography

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Thermocompression Bonding

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- Below:** Transfer of hexsil actuator onto CMOS wafer

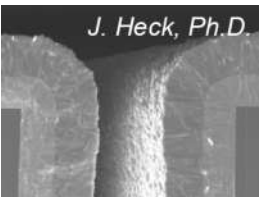
The SEM image shows a hexsil actuator structure on a CMOS wafer. The image includes technical details: 20KV X200 0007 100.0U MS. [Singh, et al, Transducers'97]

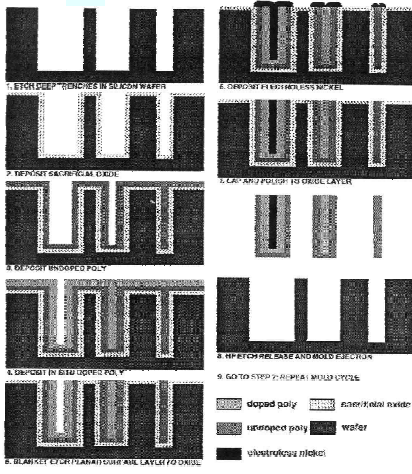
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Hexsil MEMS

- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength





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