Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- Eutectic bonding
  - Uses eutectic point in metal-Si phase diagrams to form silicides
  - Au and Si have eutectic point at 363°C
  - Low temperature process
  - Can bond slightly rough surfaces
  - Issue: Au contamination of CMOS
- Solder bonding
  - PbSn (183°C), AuSn (280°C)
  - Lower-T process
  - Can bond very rough surfaces
  - Issue: outgassing (not good for encapsulation)
- Thermocompression
  - Commonly done with electroplated Au or other soft metals
  - Room temperature to 300°C
  - Lowest-T process
  - Can bond rough surfaces with topography

Thermocompression Bonding

- Below: Transfer of hexsil actuator onto CMOS wafer

[Singh, et al, Transducers'97]

Hexsil MEMS

- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength

Hexsil MEMS Actuator

- Below: Transfer of hexsil actuator onto CMOS wafer

[Singh, et al, Transducers'97]

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Silicon-on-Insulator (SOI) MEMS

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

Nitride DI Trench
CMOS Interconnect
MEM Structure
Device Wafer
Bonding Oxide
Handle Wafer

Cross Section | Top View

Silicon
SiO_2
SOI starting material
Silicon
Nitride
Trench and Backfill
Integrated Circuitry
Structure definition and release

SOI MEMS Examples

[Brosnihan]

Micromirror
[Analog Devices]

The SCREAM Process

- SCREAM: Single Crystal Reactive Etching and Metallization process

Photoresist
Oxide
Silicon substrate
1. Deposit oxide and photoresist
2. Lithography and oxide etch
3. Silicon etch
4. Coat sidewalls with PECVD oxide
Suspended beam
Sharp tip
5. Remove oxide at bottom and etch silicon
6. Plasma etch in SF_6 to release structures

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