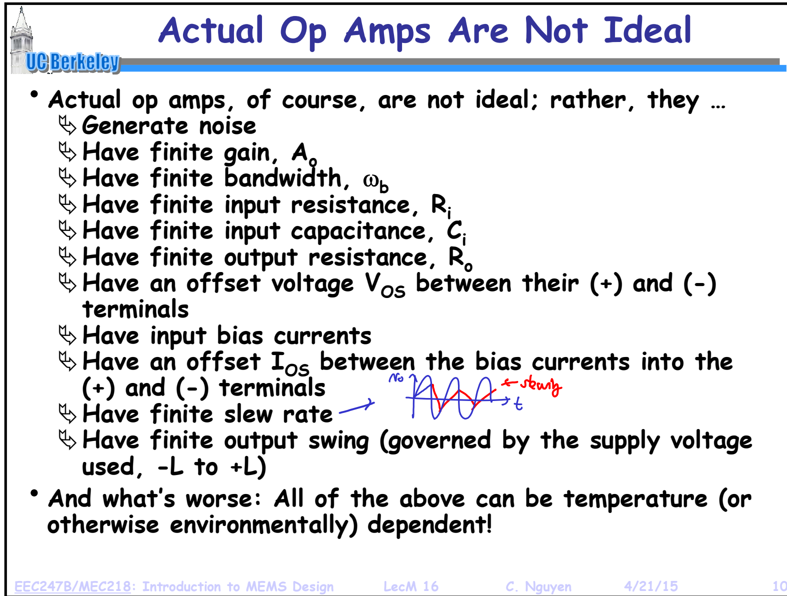

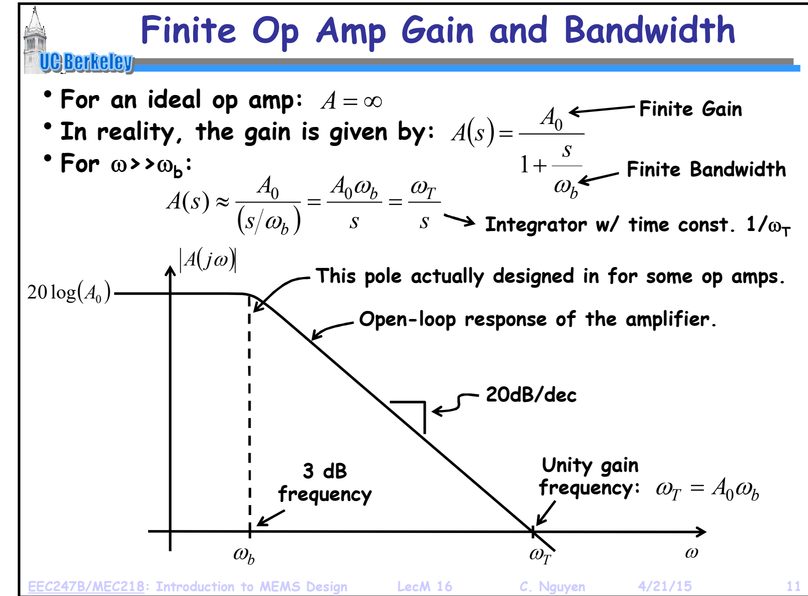

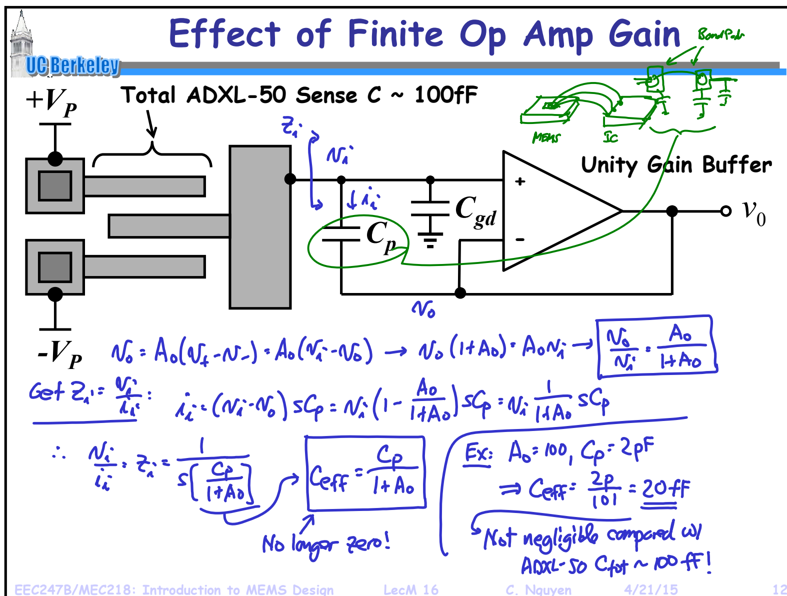

UC Berkeley

Integration of MEMS and Transistors

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Integrate or Not?

- Benefits:
  - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
  - Better reliability
  - Reduced size → lower cost?
  - Reduced packaging complexity → integration is a form of packaging → lower cost?
  - Higher integration density supports greater functionality
- Challenges:
  - Temperature ceilings imposed by the transistors or MEMS
  - Protecting one process from the other
  - Surface topography of MEMS
  - Material incompatibilities
  - Multiplication of yield losses (versus non-integrated)
  - Acceptance by transistor foundries

250 nm CMOS Cross-Section

Merged MEMS/Transistor Technologies (Process Philosophy)

- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

Analog Devices BiMEMS Process

- Interleaved MEMS and 4 µm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

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Analog Devices BiMEMS Process (cont)

- Examples:

Old ⟶ New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

- Can you list the advances in the process from old to new?

Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. → Circuits → Pass./Prot. → μMechanics → Pass./Prot.

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

→ Fully Integrated μMechanical Resonator Oscillator

- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

MEMS-First Integration

- Modular technology minimizes product updating effort
  - Module 1: micromachining process (planar technology)
  - Module 2: transistor process (planar IC technology)
- Adv.: (ideally) no changes needed to the transistor process
- Adv.: high temperature ceiling for some MEMS materials
- Challenges:
  - Reducing topography after MEMS processing so transistors can be processed
  - Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
  - Getting transistor foundries to accept pre-processed wafers

MEMS-First Integration

- Problem: μstructural topography interferes with lithography
  - difficult to apply photoresist for submicron circuits

Photoresist Welling; 6-10μm; Passivation/Protection Layers; Photoresist Thinning Due to Streaking While Spinning; Nitride; Structural Polysilicon; Sacrificial Oxide; Thermal Oxide; Silicon Substrate

- Soln.: build μmechanics in a trench, then planarize before circuit processing [Smith *et al*, IEDM'95]

Silicon for Circuits; Contact to Circuits Made Here; Micromechanics Trench; Surface and Structures Planarized Via CMP; Oxide; Polysilicon Stud; Nitride; Structural Polysilicon; Sacrificial Oxide; Epitaxial Layer; Silicon Substrate

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MEMS-First Ex: Sandia's iMEMS

- Used to demonstrate functional fully integrated oscillators
- Issues:
  - lithography and etching may be difficult in trench → may limit dimensions (not good for RF MEMS)
  - μmechanical material must stand up to IC temperatures (>1000°C) → problem for some metal materials
  - might be contamination issues for foundry IC's

[Smith *et al*, IEDM'95]

Bosch/Stanford MEMS-First Process

- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

Epi-silicon for CMOS

[Kim, Kenny Trans'05]

Problems With MEMS-First

- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

Foundry Acceptance of MEMS-First?

- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon

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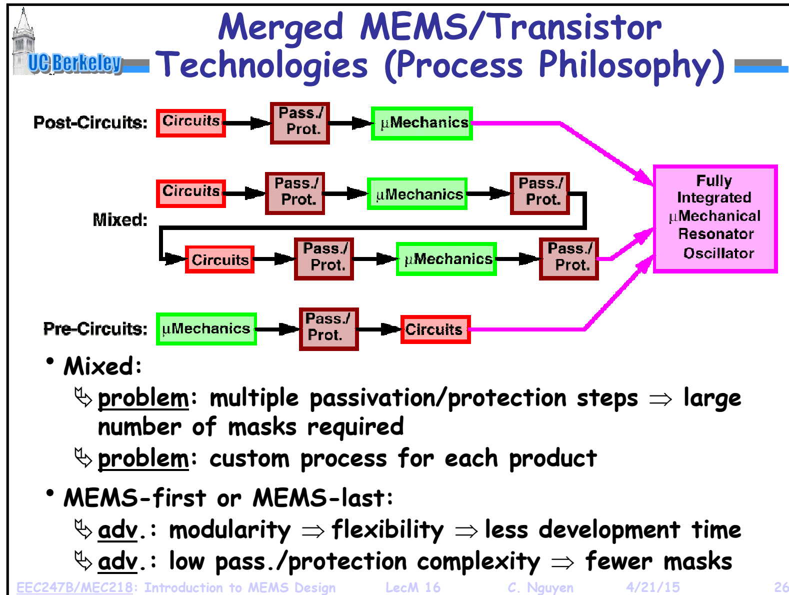

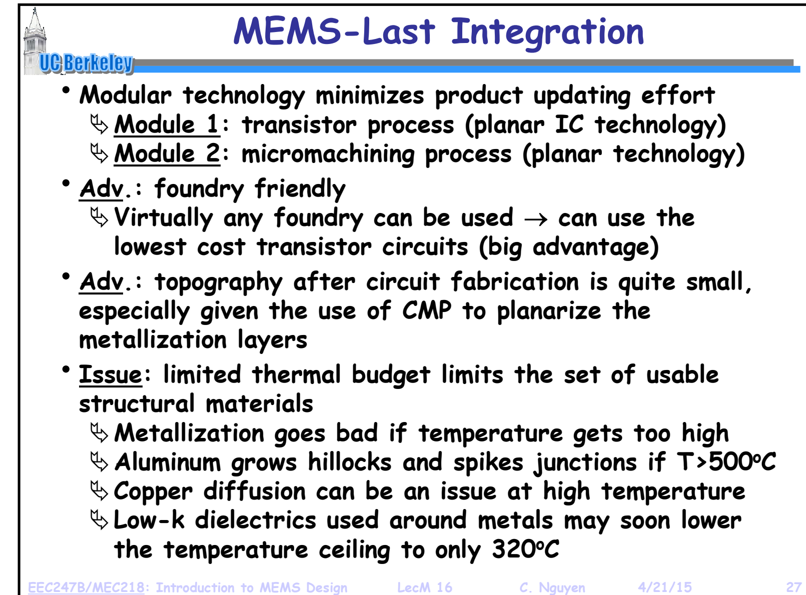

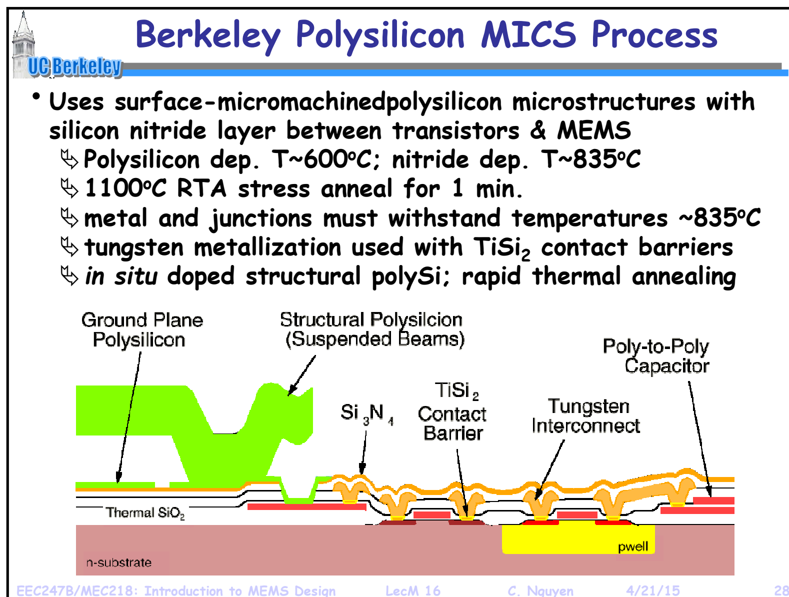

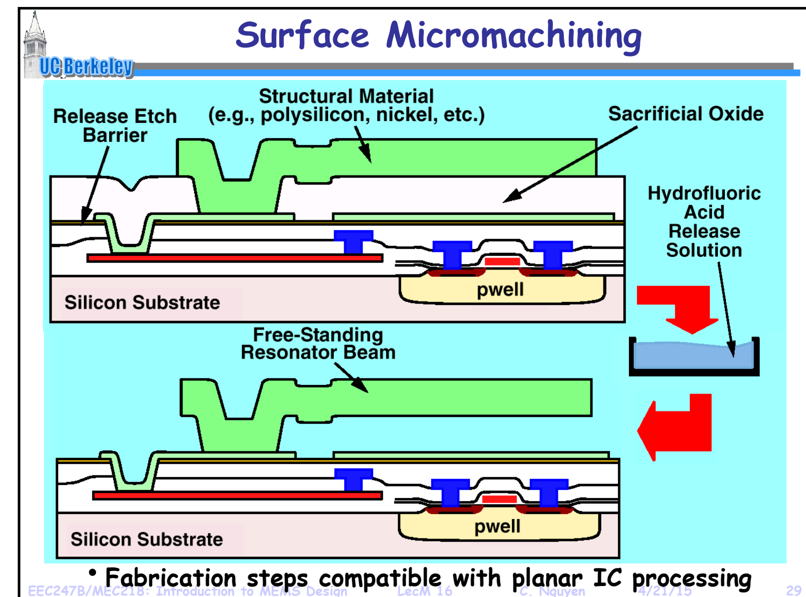

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Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

[Nguyen, Howe 1993]

- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

Usable MEMS-Last Integration

- Problem: tungsten is not an accepted primary interconnect metal
- Challenge: retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe *et al*, MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable

Poly-SiGe MICS Process

- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe ~450°C
  - *Adv.*: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

[Franke, Howe 2001]

Polysilicon Germanium

- Deposition
  - LPCVD thermal decomposition of GeH_4 and SiH_4 or Si_2H_6
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation
- Dry Etching
  - Similar to poly-Si, use F, Cl, and Br⁻ containing plasmas
  - Rate ~0.4 μm/min
- Wet Etching
  - H_2O_2 @ 90°C: can get 4 orders of magnitude selectivity between >80% and <60% Ge content
  - Good release etchant

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Poly-SiGe Mechanical Properties

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus ~ 146 GPa (for poly-$Si_{0.35}Ge_{0.65}$)
- Density ~4280 kg/m^3
- Acoustic velocity ~5840 m/s (25% lower than polysilicon)
  - Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q=30,000 for n-type poly-Ge in vacuum

UCB Poly-SiGe MICS Process

- 2 μm standard CMOS process w/ Al metallization
- P-type poly-$Si_{0.35}Ge_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)

ASIMPS Ckt/MEMS Integration Process

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF_3/O_2 oxide etch
- Structures released via a final SF_6 isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
  - Must design defensively against warping

ASIMPS Ckt/MEMS Integration Process

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

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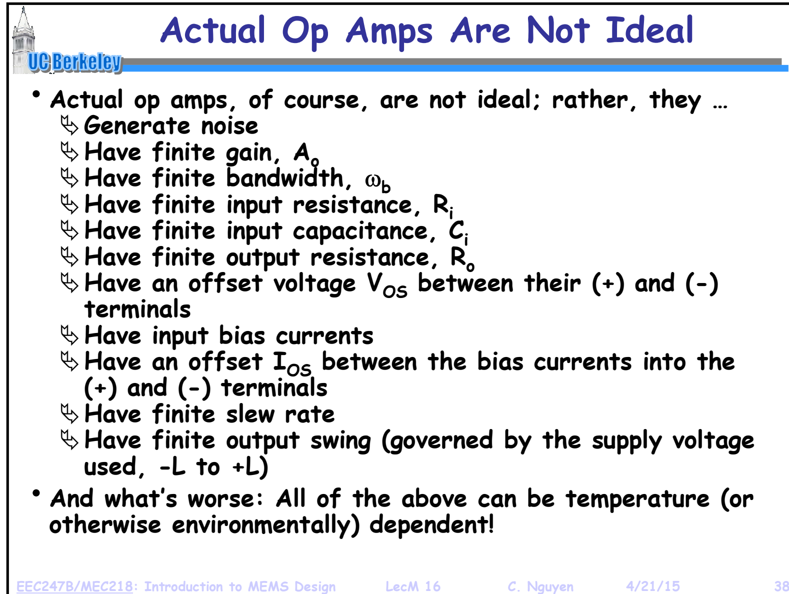

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