


EE C247B - ME C218
Introduction to MEMS Design
Spring 2018

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Module 16: Sensing Non-Idealities & Integration

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Lecture Outline

- Reading: Senturia Chpt. 14, 15
- Lecture Topics:
 - ↗ Ideal Op Amps
 - ↗ Op Amp Non-Idealities
 - ↗ MEMS-Transistor Integration
 - Mixed
 - MEMS-First
 - MEMS-Last
 - ↗ Op Amp Non-Idealities (cont.)

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Ideal Operational Amplifiers

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Ideal Op Amp

- Equivalent Circuit of an Ideal Op Amp:**

v_1 (input), R_{in} (input resistor), v_+ (non-inverting input), v_- (inverting input), $i_1 = 0$, $i_2 = 0$, $A(v_+ - v_-)$ (gain), $v_0 = A(v_+ - v_-) = A(v_2 - v_1)$ (output), R_0 (output resistor), Voltage-Controlled Voltage Source (VCVS)

- Properties of Ideal Op Amps:**

- $R_{in} = \infty$ \longrightarrow 4. $i_+ = i_- = 0$
- $R_0 = 0$
- $A = \infty$ \longrightarrow 5. $v_+ = v_-$, assuming $v_0 = \text{finite}$ **Why?**

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Ideal Op Amp (cont)

• Properties of Ideal Op Amps:

1. $R_{in} = \infty \longrightarrow$
2. $R_o = 0$
3. $A = \infty \longrightarrow$
4. $i_+ = i_- = 0$
5. $v_+ = v_-$, assuming $v_o = \text{finite}$

Why? Because for

$$\infty(v_+ - v_-) = v_o = \text{finite}$$

$$\therefore \underbrace{v_+ - v_- = 0}_{\frac{v_o}{\infty}} \rightarrow v_+ = v_-$$

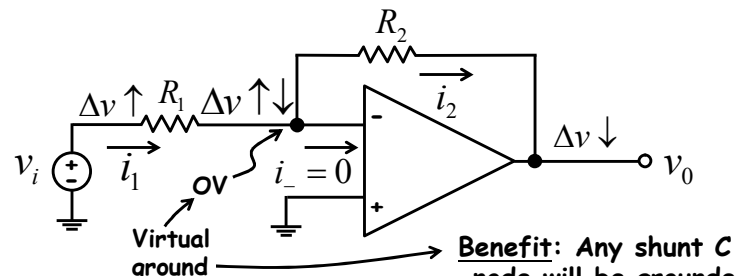
$\frac{v_o}{\infty} \Rightarrow$ virtual short circuit (virtual ground)

• Big assumption! ($v_o = \text{finite}$)

• How can we assume this? We can assume this only when there is an appropriate negative feedback path!

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Inverting Amplifier



Benefit: Any shunt C at this node will be grounded out.

1. Verify that there is negative FB.
2. $\therefore v_o = \text{finite} \rightarrow v_+ = v_- \rightarrow$ node attached to (-) terminal is virtual ground.
3. $i_- = 0 \therefore i_1 = i_2$

$$\left. \begin{aligned} i_1 &= \frac{v_i - 0}{R_1} = \frac{v_i}{R_1} = i_2 \\ v_o &= 0 - i_2 R_2 = -i_2 R_2 \end{aligned} \right\} \Rightarrow v_o = -\left(\frac{v_i}{R_1}\right) R_2 = -\frac{R_2}{R_1} v_i \therefore \boxed{\frac{v_o}{v_i} = -\frac{R_2}{R_1}}$$

NOTE: Gain dependent only on R_1 & R_2 (external components), not on the op amp gain.

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Transresistance Amplifier

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• Take R_1 away

Virtual ground $i_- = 0$

Again, shunt C at this node will be grounded out.

1. Verify that there is neg. FB \rightarrow yes, since same FB as inverting amplifier
2. Thus, $v_o = \text{finite} \rightarrow v_+ = v_- \rightarrow (-)$ terminal is virtual ground
3. $i_- = 0 \rightarrow i_1 = i_2$

$$v_o = -i_2 R_2 = -i_i R_2 \Rightarrow \boxed{\frac{v_o}{i_i} = -R_2}$$

An inverting amplifier is just a transresistance amplifier with an R_1 to convert voltage to current!

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Integrator-Based Diff. Position Sensing

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$R_2 \gg \frac{1}{sC_2}$ (for biasing)

$R_o = 0\Omega$

Can drive next stage's R_1 w/o interference to transfer function!

$i_o = i_1 + i_2 = N_p(sC_1) - N_p(sC_2) = N_p s(C_1 - C_2)$

$\therefore v_o = -i_o \left(\frac{1}{sC_F}\right) = -N_p \left(\frac{C_1 - C_2}{C_F}\right)$


$\boxed{\frac{v_o}{V_p} = -\frac{C_1 - C_2}{C_F}} \Rightarrow$ A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

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Non-Ideal Operational Amplifiers

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Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they ...
 - ↗ Generate noise
 - ↗ Have finite gain, A_o
 - ↗ Have finite bandwidth, ω_b
 - ↗ Have finite input resistance, R_i
 - ↗ Have finite input capacitance, C_i
 - ↗ Have finite output resistance, R_o
 - ↗ Have an offset voltage V_{OS} between their (+) and (-) terminals
 - ↗ Have input bias currents
 - ↗ Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
 - ↗ Have finite slew rate
 - ↗ Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

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Finite Op Amp Gain and Bandwidth

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- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_0}{1 + \frac{s}{\omega_b}}$
 - A_0 ← Finite Gain
 - $1 + \frac{s}{\omega_b}$ ← Finite Bandwidth
- For $\omega \gg \omega_b$: $A(s) \approx \frac{A_0}{(s/\omega_b)} = \frac{A_0 \omega_b}{s} = \frac{\omega_T}{s}$ → Integrator w/ time const. $1/\omega_T$

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Effect of Finite Op Amp Gain

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Total ADXL-50 Sense C ~ 100fF

Unity Gain Buffer

V_o

$+V_P$

$-V_P$

$N_o = A_o(V_i - N_o) = A_o(N_i - N_o) \rightarrow N_o(1 + A_o) = A_o N_i \rightarrow \frac{N_o}{N_i} = \frac{A_o}{1 + A_o}$


Get $Z_i = \frac{V_i}{i_i}$: $i_i = (N_i - N_o) s C_p = N_i \left(1 - \frac{A_o}{1 + A_o}\right) s C_p = N_i \frac{1}{1 + A_o} s C_p$

$\therefore \frac{N_o}{N_i} = Z_i = \frac{1}{s \left[\frac{C_p}{1 + A_o} \right]}$ → $C_{eff} = \frac{C_p}{1 + A_o}$

No longer zero!


Ex: $A_o = 100, C_p = 2 \text{ pF}$
 $\Rightarrow C_{eff} = \frac{2 \text{ pF}}{101} = \underline{20 \text{ fF}}$
 Not negligible compared w/ ADXL-50 $C_{tot} \sim 100 \text{ fF}!$

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Integration of MEMS and Transistors

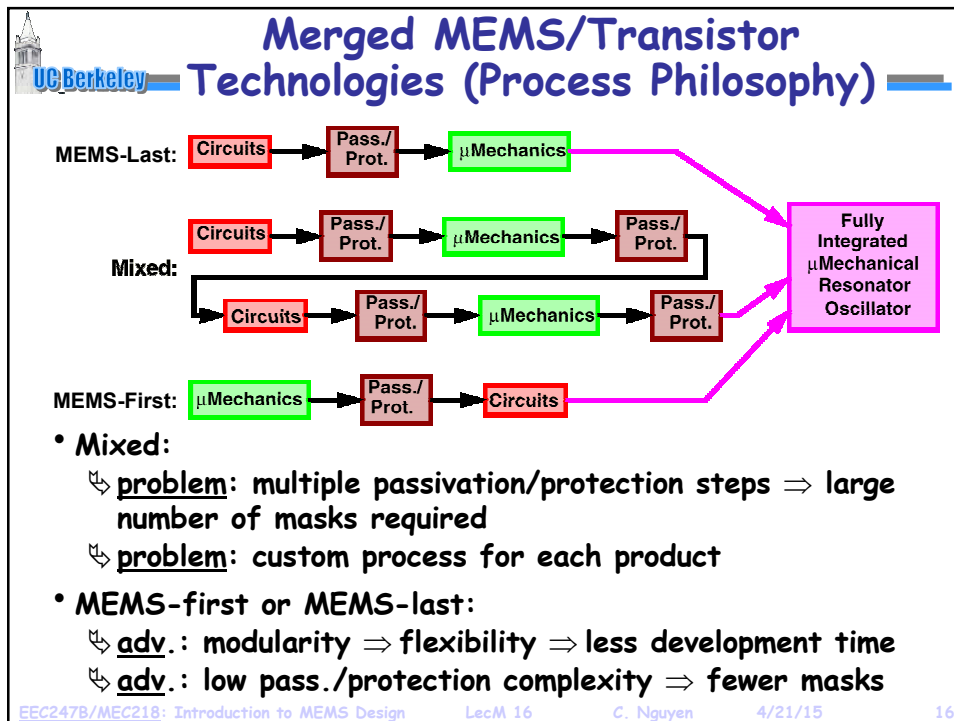
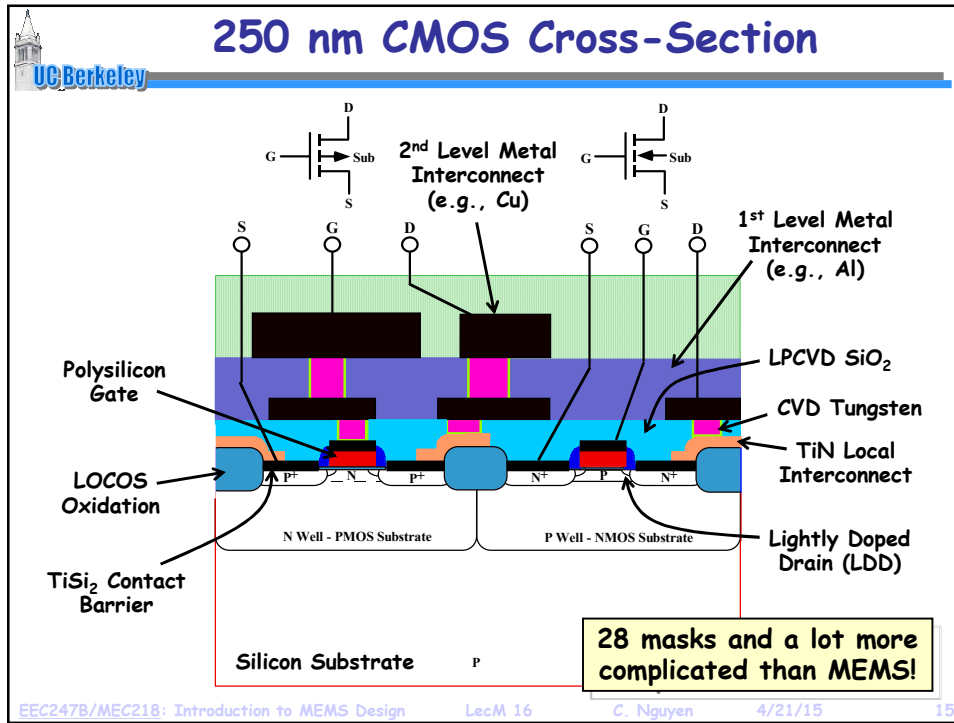
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Integrate or Not?

- **Benefits:**
 - ↖ Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
 - ↖ Better reliability
 - ↖ Reduced size → lower cost?
 - ↖ Reduced packaging complexity → integration is a form of packaging → lower cost?
 - ↖ Higher integration density supports greater functionality
- **Challenges:**
 - ↖ Temperature ceilings imposed by the transistors or MEMS
 - ↖ Protecting one process from the other
 - ↖ Surface topography of MEMS
 - ↖ Material incompatibilities
 - ↖ Multiplication of yield losses (versus non-integrated)
 - ↖ Acceptance by transistor foundries

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Analog Devices BiMEMS Process

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- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

SILICON	LPCVD NITRIDE	SPACER LTO	PLASMA OXIDE
OXIDE	BPSG	SENSOR POLYSI	PLASMA NITRIDE
POLYSI	LTO	METAL	

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Analog Devices BiMEMS Process (cont)

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• **Examples:**

Old → New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

• Can you list the advances in the process from old to new?

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Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot.

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

Fully Integrated μMechanical Resonator Oscillator

- **Mixed:**
 - ↪ **problem:** multiple passivation/protection steps ⇒ large number of masks required
 - ↪ **problem:** custom process for each product
- **MEMS-first or MEMS-last:**
 - ↪ **adv.:** modularity ⇒ flexibility ⇒ less development time
 - ↪ **adv.:** low pass./protection complexity ⇒ fewer masks

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MEMS-First Integration

- **Modular technology** minimizes product updating effort
 - ↪ **Module 1:** micromachining process (planar technology)
 - ↪ **Module 2:** transistor process (planar IC technology)
- **Adv.:** (ideally) no changes needed to the transistor process
- **Adv.:** high temperature ceiling for some MEMS materials
- **Challenges:**
 - ↪ Reducing topography after MEMS processing so transistors can be processed
 - ↪ Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
 - ↪ Getting transistor foundries to accept pre-processed wafers

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MEMS-First Integration

Problem: μ structural topography interferes with lithography
 ↳ difficult to apply photoresist for submicron circuits

Soln.: build μ mechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]

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MEMS-First Ex: Sandia's iMEMS

Used to demonstrate functional fully integrated oscillators

Issues:

- ↳ lithography and etching may be difficult in trench → may limit dimensions (not good for RF MEMS)
- ↳ μ mechanical material must stand up to IC temperatures (>1000°C) → problem for some metal materials
- ↳ might be contamination issues for foundry IC's

[Smith et al, IEDM'95]

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Bosch/Stanford MEMS-First Process

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- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

Resonator, Epi-Poly Seal, Epi-Poly Cap, Contact

Substrate

Epi-silicon for CMOS

Transistor Circuits, Vacuum Chamber, μ Mechanical Device

[Kim, Kenny Trans'05]

(A) Silicon, Oxide, Sensor Structure, Silicon, p-plus
 (B) Nonconformal LTO
 (C) Monocrystalline Silicon, Polycrystalline Silicon, Vent
 (D) Nonconformal LTO
 (E) Aluminum Pad

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Problems With MEMS-First

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- Many masking steps needed, plus CMP required \rightarrow cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
 - \hookrightarrow Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
 - \hookrightarrow thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

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UC Berkeley **Foundry Acceptance of MEMS-First?**

- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
 - ↳ Feature sizes on the nm scale for billions of devices
 - ↳ Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
 - ↳ Many foundries will not accept any pre-processed wafers, MEMS or not → just can't guarantee working transistor circuits with unknowns in starting silicon

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UC Berkeley **Merged MEMS/Transistor Technologies (Process Philosophy)**

```

    graph LR
        subgraph Post-Circuits
            C1[Circuits] --> P1[Pass./Prot.]
            P1 --> M1[μMechanics]
        end
        subgraph Mixed
            C2[Circuits] --> P2[Pass./Prot.]
            P2 --> M2[μMechanics]
            M2 --> P3[Pass./Prot.]
        end
        subgraph Pre-Circuits
            M3[μMechanics] --> P4[Pass./Prot.]
            P4 --> C3[Circuits]
        end
        M1 --> FIO[Fully Integrated μMechanical Resonator Oscillator]
        P3 --> FIO
        C3 --> FIO
    
```

- Mixed:
 - ↳ problem: multiple passivation/protection steps ⇒ large number of masks required
 - ↳ problem: custom process for each product
- MEMS-first or MEMS-last:
 - ↳ adv.: modularity ⇒ flexibility ⇒ less development time
 - ↳ adv.: low pass./protection complexity ⇒ fewer masks

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MEMS-Last Integration

- Modular technology minimizes product updating effort
 - ↳ **Module 1**: transistor process (planar IC technology)
 - ↳ **Module 2**: micromachining process (planar technology)
- **Adv.**: foundry friendly
 - ↳ Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- **Adv.**: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- **Issue**: limited thermal budget limits the set of usable structural materials
 - ↳ Metallization goes bad if temperature gets too high
 - ↳ Aluminum grows hillocks and spikes junctions if $T > 500^\circ\text{C}$
 - ↳ Copper diffusion can be an issue at high temperature
 - ↳ Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

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Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
 - ↳ Polysilicon dep. $T \sim 600^\circ\text{C}$; nitride dep. $T \sim 835^\circ\text{C}$
 - ↳ 1100°C RTA stress anneal for 1 min.
 - ↳ metal and junctions must withstand temperatures $\sim 835^\circ\text{C}$
 - ↳ tungsten metallization used with TiSi_2 contact barriers
 - ↳ *in situ* doped structural polySi; rapid thermal annealing

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Surface Micromachining

The diagram illustrates the surface micromachining process in two stages. In the top stage, a silicon substrate is coated with a sacrificial oxide layer. A structural material (e.g., polysilicon, nickel, etc.) is deposited and patterned to form a resonator beam. A release etch barrier is also present. A pwell is formed in the substrate. In the bottom stage, hydrofluoric acid release solution is used to etch away the sacrificial oxide, resulting in a free-standing resonator beam. The process is noted as being compatible with planar IC processing.

- Fabrication steps compatible with planar IC processing

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Single-Chip Ckt/MEMS Integration

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

The micrograph shows a single-chip Ckt/MEMS integration. Key components labeled include: Sustaining Amplifier, Input, Comb-Transducer, Shuttle Mass, Folded-Beam Suspension, Anchors, and V_p . A vertical scale bar indicates 300 μm . An inset shows an oscilloscope output waveform with the following data:

CH1	P-P	324.0V
CH1	FRE	21.52
CH1	PER	61.22
CH1	RISE	16.16V

Oscilloscope Output Waveform
 [Nguyen, Howe 1993]

- To allow the use of $>600^\circ\text{C}$ processing temperatures, tungsten (instead of aluminum) is used for metallization

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Usable MEMS-Last Integration

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- **Problem:** tungsten is not an accepted primary interconnect metal
- **Challenge:** retain conventional metallization
 - ↳ minimize post-CMOS processing temperatures
 - ↳ explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe *et al*, MEMS'99])
 - ↳ Limited set of usable structural materials → not the best situation, but workable


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Poly-SiGe MICS Process

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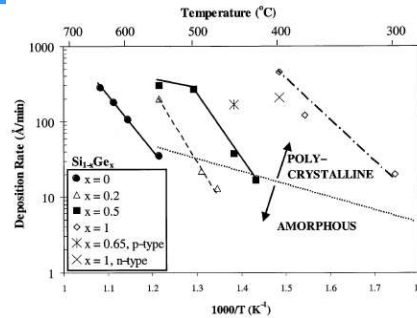
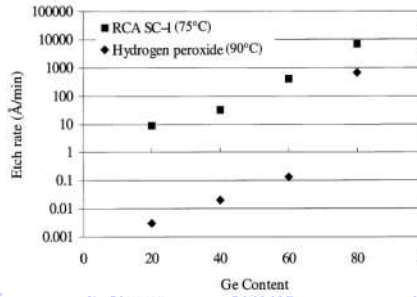
- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
 - ↳ enabled by lower deposition temperature of SiGe ~450°C
 - ↳ **Adv.:** alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

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Polysilicon Germanium

- **Deposition**
 - ↳ LPCVD thermal decomposition of GeH_4 and SiH_4 or Si_2H_6
 - ↳ Rate $> 50 \text{ \AA}/\text{min}$, $T < 475^\circ\text{C}$, $P = 300\text{-}600 \text{ mT}$
 - ↳ At higher $[\text{Ge}]$: rate \uparrow , $T \downarrow$
 - ↳ In-situ doping, ion implantation
- **Dry Etching**
 - ↳ Similar to poly-Si, use F, Cl, and Br^- containing plasmas
 - ↳ Rate $\sim 0.4 \mu\text{m}/\text{min}$
- **Wet Etching**
 - ↳ H_2O_2 @ 90°C : can get 4 orders of magnitude selectivity between $>80\%$ and $<60\%$ Ge content
 - ↳ Good release etchant

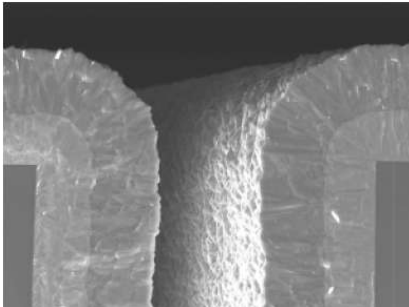
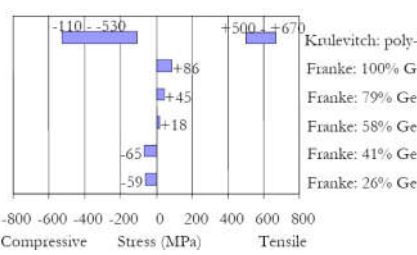



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Poly-SiGe Mechanical Properties

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus $\sim 146 \text{ GPa}$ (for poly- $\text{Si}_{0.35}\text{Ge}_{0.65}$)
- Density $\sim 4280 \text{ kg}/\text{m}^3$
- Acoustic velocity $\sim 5840 \text{ m/s}$ (25% lower than polysilicon)
 - ↳ Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- $Q=30,000$ for n-type poly-Ge in vacuum

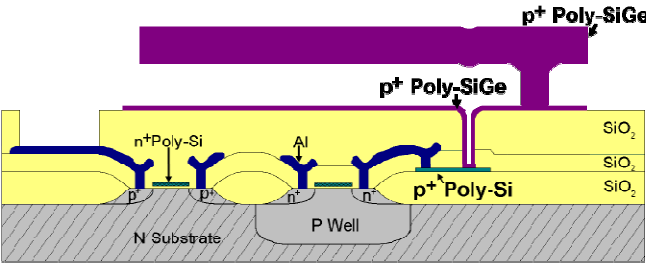
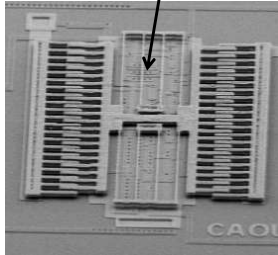



Sample	Stress (MPa)
Kruevitch: poly-Si	-110
Frankle: 100% Ge	-530
Frankle: 79% Ge	+86
Frankle: 58% Ge	+45
Frankle: 41% Ge	+18
Frankle: 26% Ge	-65
Other	-59
Other	+500
Other	+670

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UC Berkeley UCB Poly-SiGe MICS Process

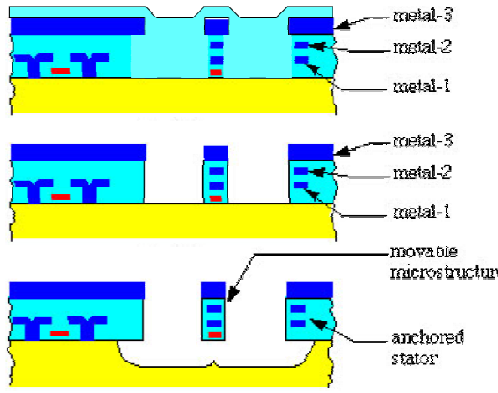
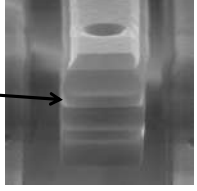
- 2 μm standard CMOS process w/ Al metallization
- P-type poly- $\text{Si}_{0.35}\text{Ge}_{0.65}$ structural material; poly-Ge sacrificial material
- Process:
 - ↳ Passivate CMOS w/ LTO @ 400°C
 - ↳ Open vias to interconnect runners
 - ↳ Deposit & pattern ground plane
 - ↳ RTA anneal to lower resistivity (550°C, 30s)

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UC Berkeley ASIMPS Ckt/MEMS Integration Process

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF_3/O_2 oxide etch
- Structures released via a final SF_6 isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
 - ↳ Must design defensively against warping

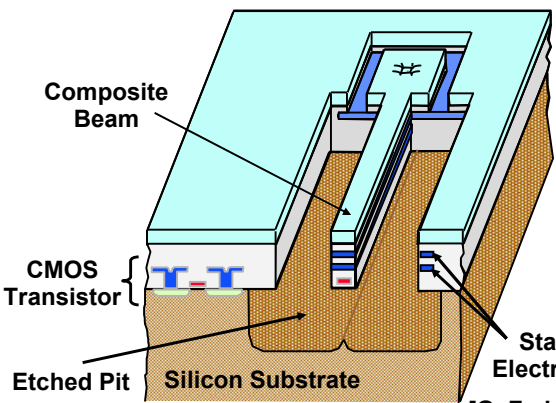
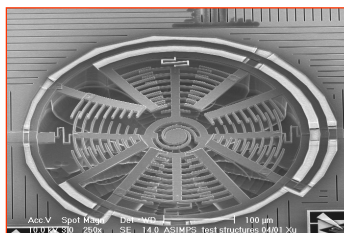



[G. Fedder, CMU]
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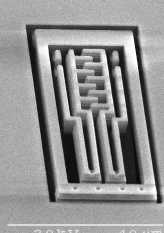
ASIMPS Ckt/MEMS Integration Process

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- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

Gyro Resonator



Uncooled IR Detector Element

[G. Fedder, CMU]

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Actual Op Amps Are Not Ideal

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- Actual op amps, of course, are not ideal; rather, they ...
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 - ↗ Have finite gain, A_o
 - ↗ Have finite bandwidth, ω_b
 - ↗ Have finite input resistance, R_i
 - ↗ Have finite input capacitance, C_i
 - ↗ Have finite output resistance, R_o
 - ↗ Have an offset voltage V_{OS} between their (+) and (-) terminals
 - ↗ Have input bias currents
 - ↗ Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
 - ↗ Have finite slew rate
 - ↗ Have finite output swing (governed by the supply voltage used, $-L$ to $+L$)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

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Finite Op Amp Gain and Bandwidth

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- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_0}{1 + \frac{s}{\omega_b}}$
 - A_0 ← Finite Gain
 - $1 + \frac{s}{\omega_b}$ ← Finite Bandwidth
- For $\omega \gg \omega_b$:

$$A(s) \approx \frac{A_0}{(s/\omega_b)} = \frac{A_0 \omega_b}{s} = \frac{\omega_T}{s} \rightarrow \text{Integrator w/ time const. } 1/\omega_T$$

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Op Amp Non-Idealities

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Op Amp Non-Idealities → R_i & R_o

Input resistance R_i and Output Resistance R_o :

With finite R_i and R_o , and finite gain and BW, the op amp equivalent circuit becomes:

⇒ Basically reduces down to a voltage-amplifier model
 ⇒ Add an output C_0 to model a single pole response, where

$$\omega_b = \frac{1}{R_o C_0}$$

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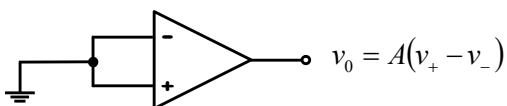
Back to Op Amp Non-Idealities

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Input Offset Voltage V_{OS}

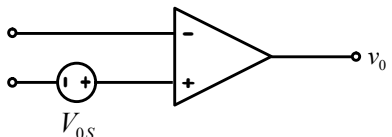
Input Offset Voltage, V_{OS} :



$v_0 = A(v_+ - v_-)$

Ideal case: $v_0 = 0$
Reality: $v_0 \neq 0$ (usually, $v_0 = L^+$ or L^- : it rails out!)

Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage V_{OS} .

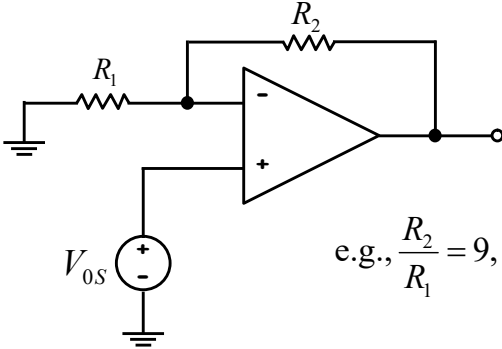


Typically, $V_{OS} = 1\text{mV} - 5\text{mV}$

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Effect of V_{OS} on Op Amp Circuits

Example: Non-Inverting Amplifier



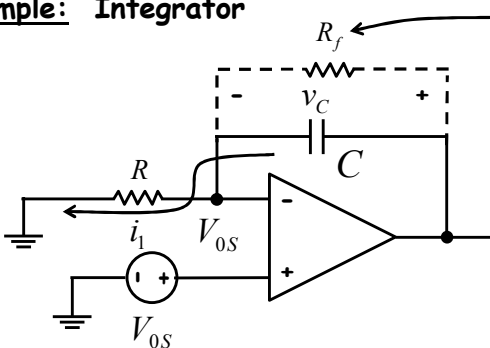
$$V_0 = V_{OS} \left(1 + \frac{R_2}{R_1} \right)$$

e.g., $\frac{R_2}{R_1} = 9, V_{OS} = 5mV \rightarrow V_0 = 50mV$
 (not so bad ...)

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Effect of V_{OS} on Op Amp Circuits (cont.)

Example: Integrator



To fix this, place a resistor in shunt with the C \rightarrow then:

$$v_0 = V_{OS} \left(1 + \frac{R_f}{R} \right)$$

$$v_0 = V_{OS} + \frac{1}{C} \int_0^t i_1 dt$$

$$= V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt$$

$$= V_{OS} \left(1 + \frac{t}{RC} \right) + v_C|_{t=0}$$

Will continue to increase until op amp saturates

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