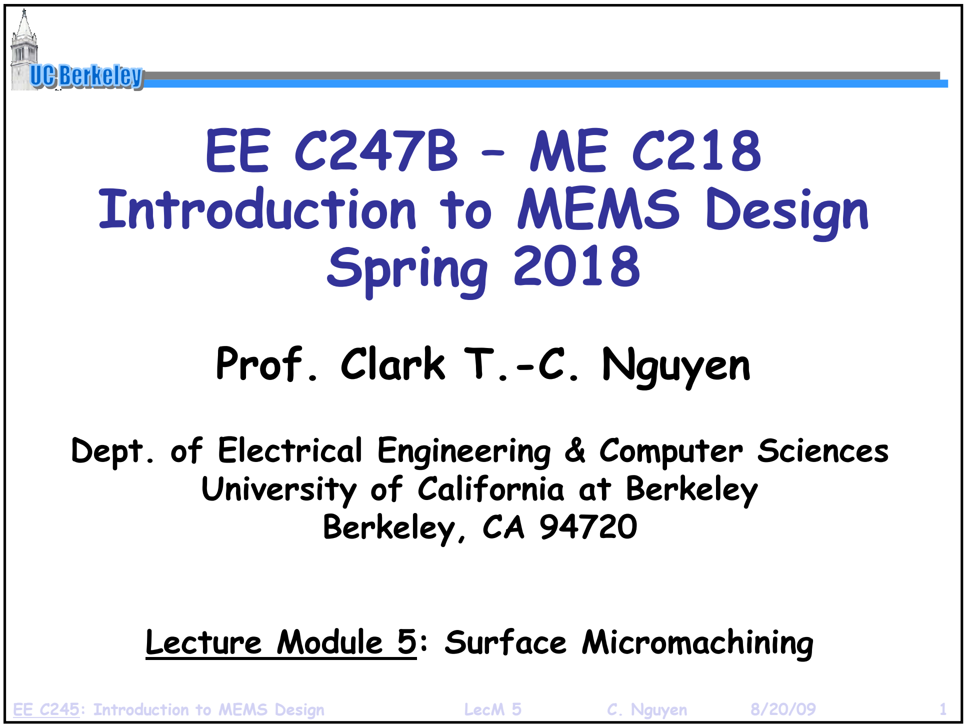

EE C247B – ME C218
Introduction to MEMS Design
Spring 2018

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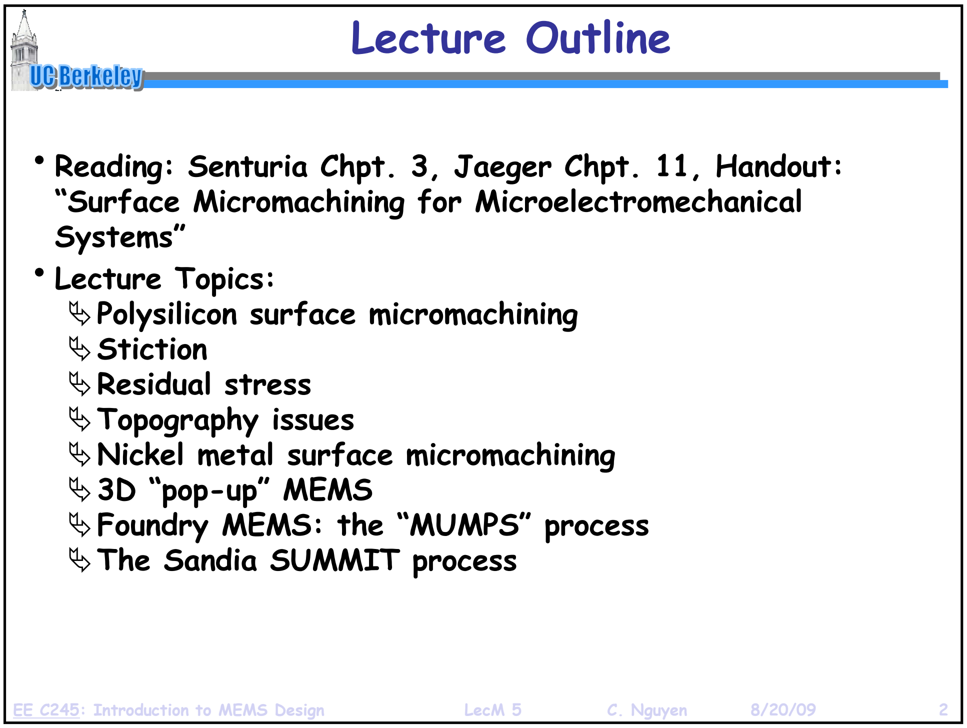
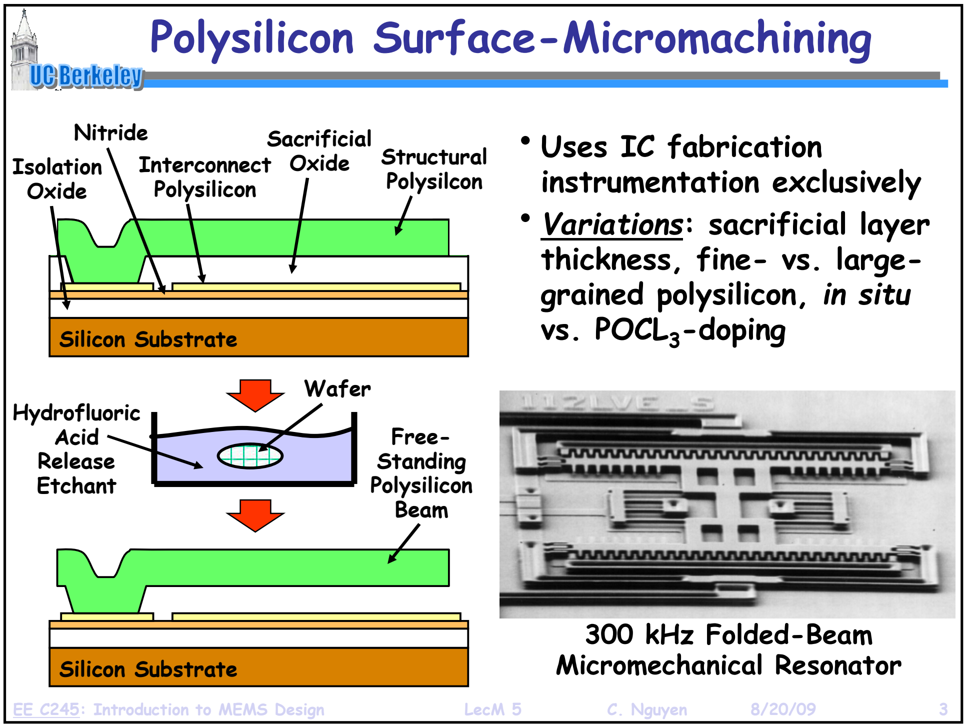
Lecture Module 5: Surface Micromachining



Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: "Surface Micromachining for Microelectromechanical Systems"
- Lecture Topics:
  - Polysilicon surface micromachining
  - Stiction
  - Residual stress
  - Topography issues
  - Nickel metal surface micromachining
  - 3D "pop-up" MEMS
  - Foundry MEMS: the "MUMPS" process
  - The Sandia SUMMIT process

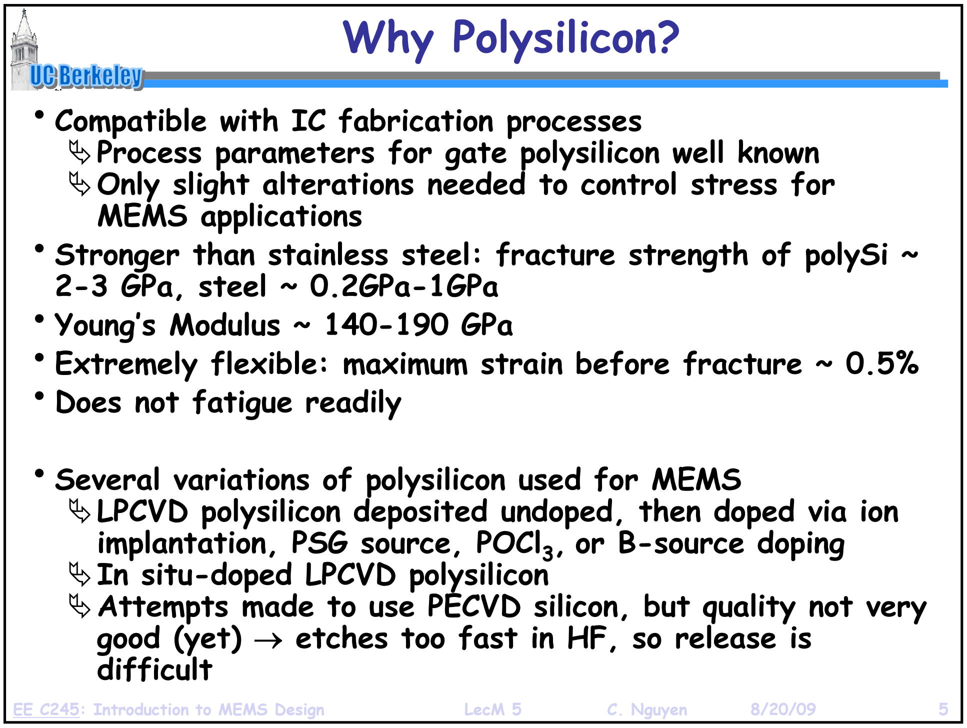


Polysilicon Surface-Micromachining

- Uses IC fabrication instrumentation exclusively
- ***Variations***: sacrificial layer thickness, fine- vs. large-grained polysilicon, *in situ* vs. $POCL_3$-doping

300 kHz Folded-Beam Micromechanical Resonator

Polysilicon

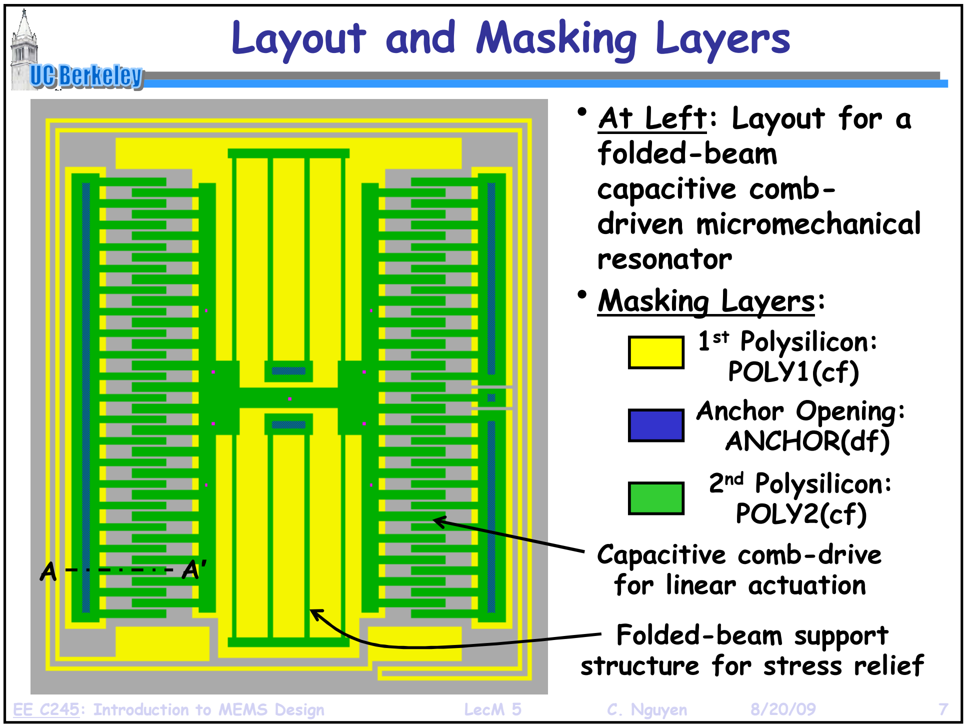


Why Polysilicon?

- Compatible with IC fabrication processes
  - Process parameters for gate polysilicon well known
  - Only slight alterations needed to control stress for MEMS applications
- Stronger than stainless steel: fracture strength of polySi ~ 2-3 GPa, steel ~ 0.2GPa-1GPa
- Young's Modulus ~ 140-190 GPa
- Extremely flexible: maximum strain before fracture ~ 0.5%
- Does not fatigue readily

- Several variations of polysilicon used for MEMS
  - LPCVD polysilicon deposited undoped, then doped via ion implantation, PSG source, $POCl_3$, or B-source doping
  - In situ-doped LPCVD polysilicon
  - Attempts made to use PECVD silicon, but quality not very good (yet) → etches too fast in HF, so release is difficult

Polysilicon Surface-Micromachining Process Flow

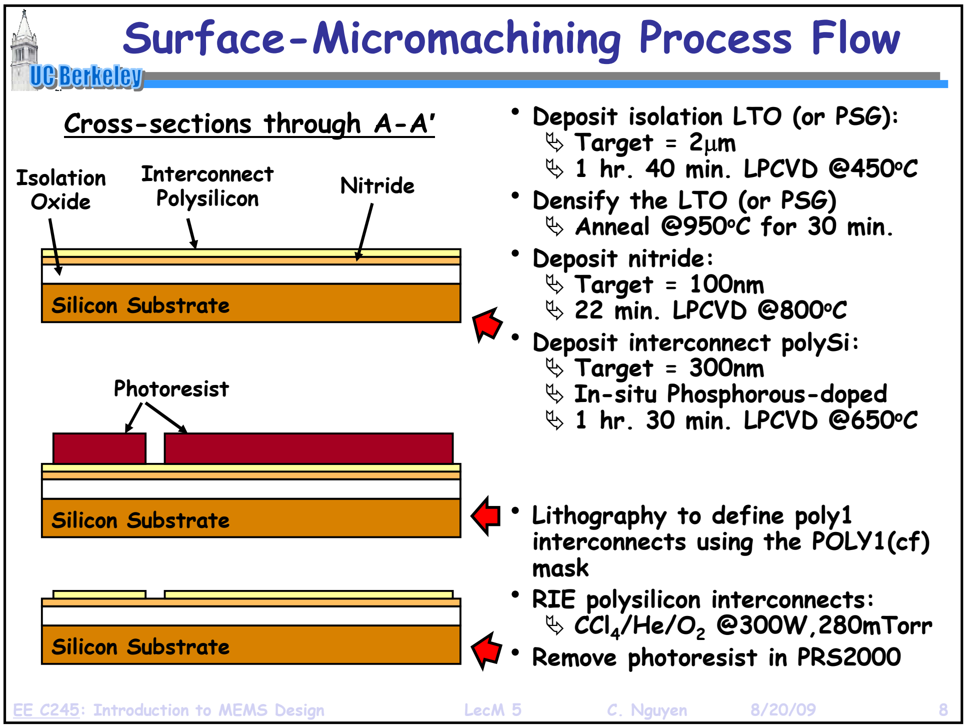


Layout and Masking Layers

- **At Left**: Layout for a folded-beam capacitive comb-driven micromechanical resonator
- **Masking Layers**:
  - 🟨 1st Polysilicon: POLY1(cf)
  - 🟦 Anchor Opening: ANCHOR(df)
  - 🟩 2nd Polysilicon: POLY2(cf)

Capacitive comb-drive for linear actuation

Folded-beam support structure for stress relief

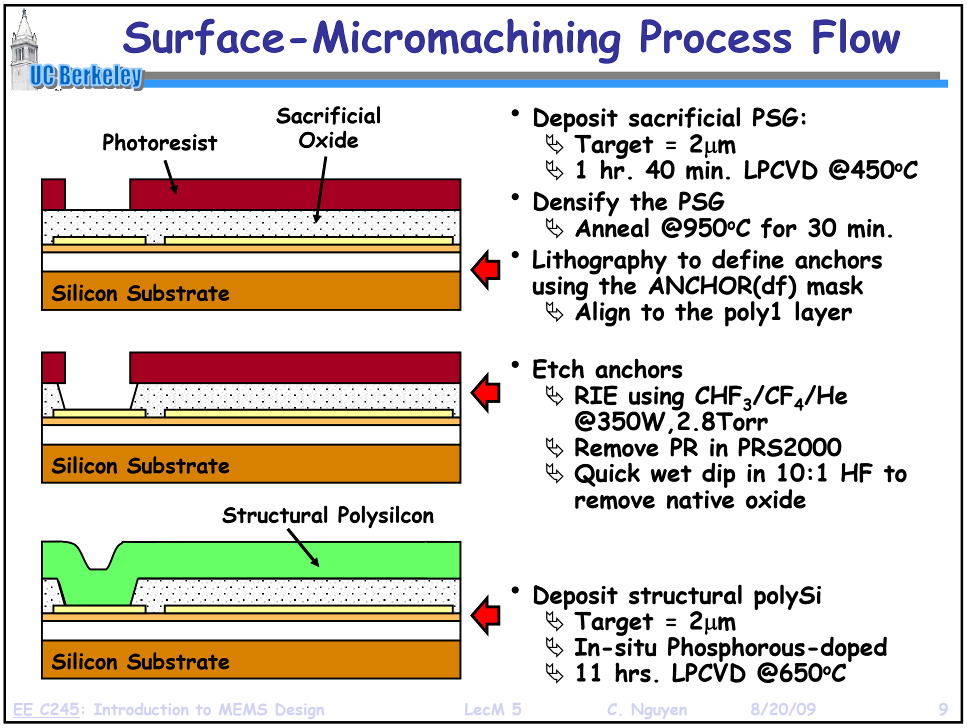


Surface-Micromachining Process Flow

- Deposit isolation LTO (or PSG):
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO (or PSG)
  - Anneal @950°C for 30 min.
- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Deposit interconnect polySi:
  - Target = 300nm
  - In-situ Phosphorous-doped
  - 1 hr. 30 min. LPCVD @650°C

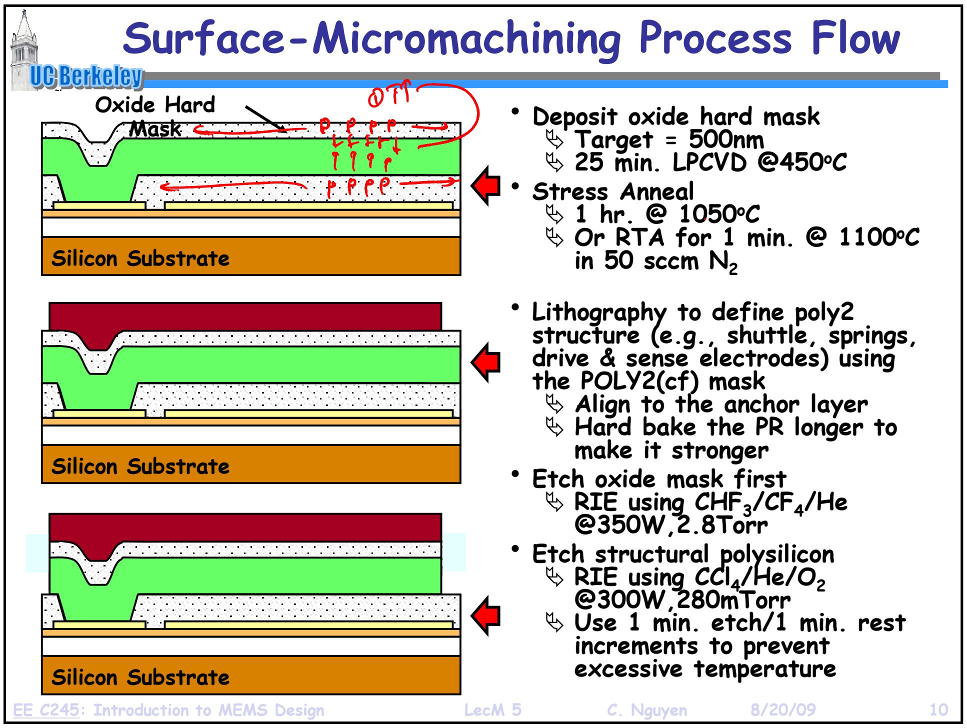
- Lithography to define poly1 interconnects using the POLY1(cf) mask

- RIE polysilicon interconnects:
  - $CCl_4/He/O_2$ @300W,280mTorr
- Remove photoresist in PRS2000



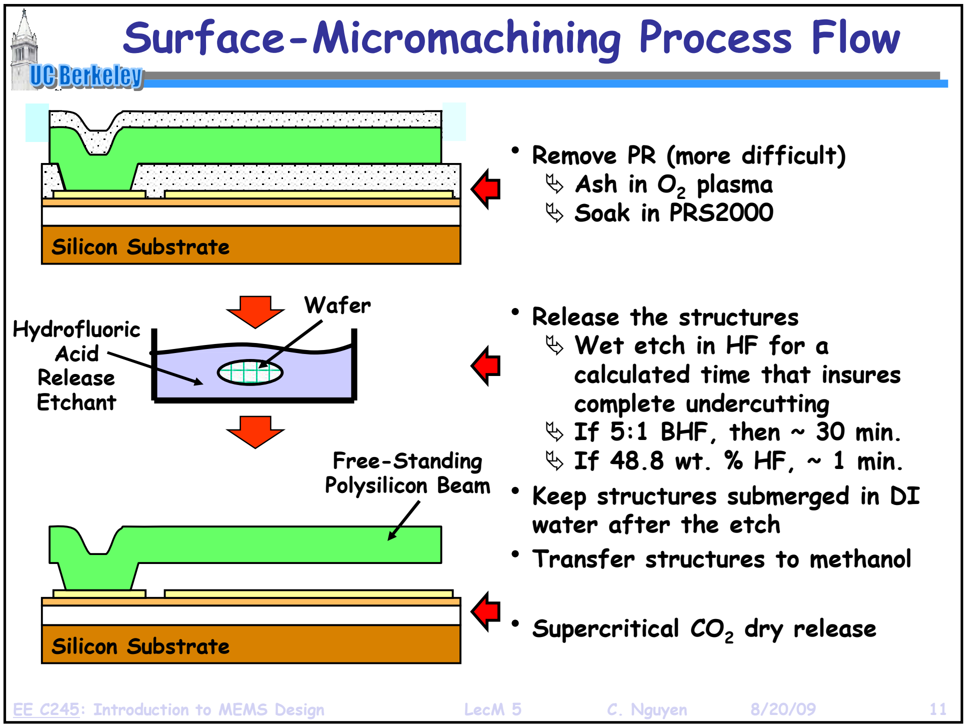
Surface-Micromachining Process Flow

- Deposit sacrificial PSG:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the PSG
  - Anneal @950°C for 30 min.
- Lithography to define anchors using the ANCHOR(df) mask
  - Align to the poly1 layer
- Etch anchors
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr
  - Remove PR in PRS2000
  - Quick wet dip in 10:1 HF to remove native oxide
- Deposit structural polySi
  - Target = 2μm
  - In-situ Phosphorous-doped
  - 11 hrs. LPCVD @650°C



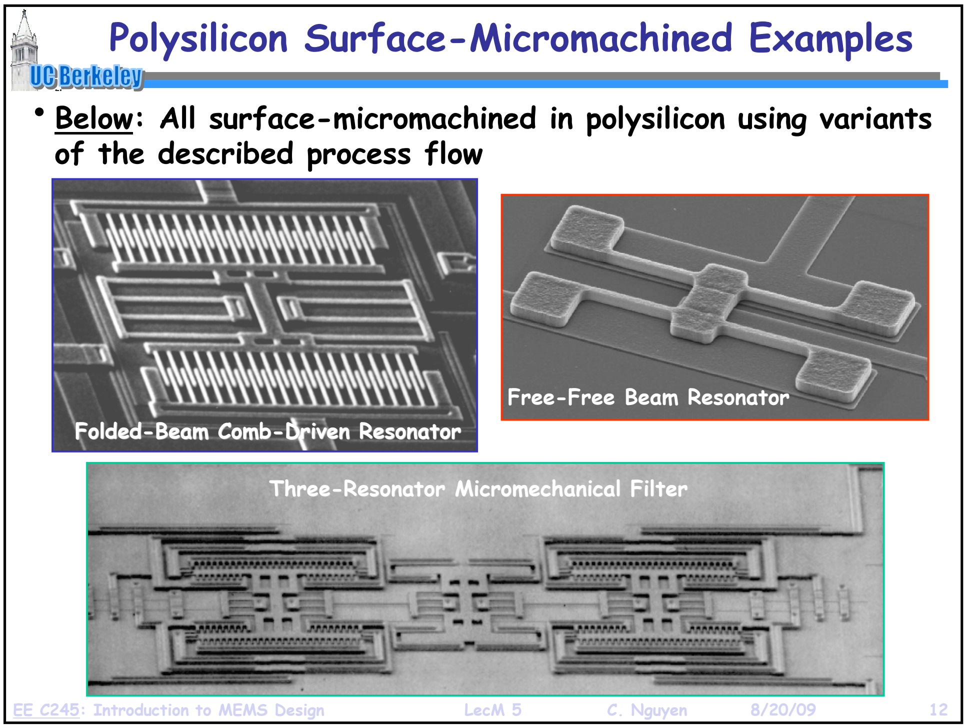
Surface-Micromachining Process Flow

- Deposit oxide hard mask
  - Target = 500nm
  - 25 min. LPCVD @450°C
- Stress Anneal
  - 1 hr. @ 1050°C
  - Or RTA for 1 min. @ 1100°C in 50 sccm N_2
- Lithography to define poly2 structure (e.g., shuttle, springs, drive & sense electrodes) using the POLY2(cf) mask
  - Align to the anchor layer
  - Hard bake the PR longer to make it stronger
- Etch oxide mask first
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr
- Etch structural polysilicon
  - RIE using $CCl_4/He/O_2$ @300W,280mTorr
  - Use 1 min. etch/1 min. rest increments to prevent excessive temperature



Surface-Micromachining Process Flow

- Remove PR (more difficult)
  - Ash in O_2 plasma
  - Soak in PRS2000
- Release the structures
  - Wet etch in HF for a calculated time that insures complete undercutting
  - If 5:1 BHF, then ~ 30 min.
  - If 48.8 wt. % HF, ~ 1 min.
- Keep structures submerged in DI water after the etch
- Transfer structures to methanol
- Supercritical CO_2 dry release



Polysilicon Surface-Micromachined Examples

- Below: All surface-micromachined in polysilicon using variants of the described process flow

Folded-Beam Comb-Driven Resonator

Free-Free Beam Resonator

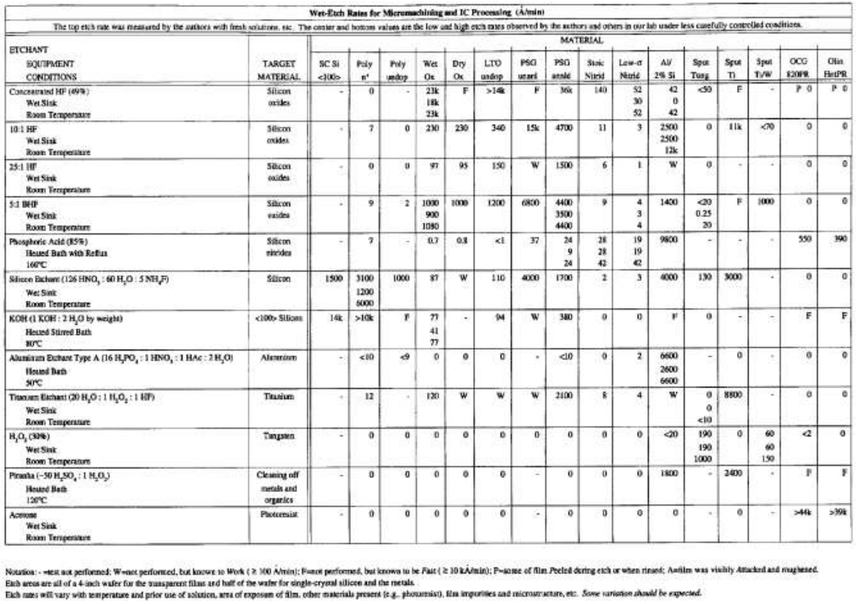
Three-Resonator Micromechanical Filter

Structural/Sacrifical Material Combinations

Structural Material	Sacrificial Material	Etchant
Poly-Si	SiO_2, PSG, LTO	HF, BHF
Al	Photoresist	O_2 plasma
SiO_2	Poly-Si	XeF_2
Al	Si	TMAH, XeF_2
Poly-SiGe	Poly-Ge	H_2O_2, hot H_2O

- Must consider other layers, too, as release etchants generally have a finite E.R. on any material
- Ex: concentrated HF (48.8 wt. %)
  - Polysilicon E.R. ~ 0
  - Silicon nitride E.R. ~ 1-14 nm/min
  - Wet thermal SiO_2 ~ 1.8-2.3 μm/min
  - Annealed PSG ~ 3.6 μm/min
  - Aluminum (Si rich) ~ 4 nm/min (much faster in other Al)

Wet Etch Rates (f/ K. Williams)



Wet-Etch Rates for Micromachining and IC Processing (Å/min)

The top etch rate was measured by the authors with fresh solutions, etc. The center and bottom values are the low and high etch rates observed by the authors and others in our lab under less carefully controlled conditions.

ETCHANT EQUIPMENT CONDITIONS	TARGET MATERIAL	MATERIAL SC Si <100>	Poly n+	Poly undop	Wet Ox	Dry Ox	LTO undop	PSG unanl	PSG annld	Stoic Nitrid	Low-σ Nitrid	Al/2% Si	Sput Tung	Sput Ti	Sput Ti/W	OCG 820PR	Olin HntPR
Concentrated HF (49%) Wet Sink Room Temperature	Silicon oxides	-	0	-	23k 18k 23k	F	>14k	F	36k	140	52 30 52	42 0 42	<50	F	-	P 0	P 0
10:1 HF Wet Sink Room Temperature	Silicon oxides	-	7	0	230	230	340	15k	4700	11	3	2500 2500 12k	0	11k	<70	0	0
25:1 HF Wet Sink Room Temperature	Silicon oxides	-	0	0	97	95	150	W	1500	6	1	W	0	-	-	0	0
5:1 BHF Wet Sink Room Temperature	Silicon oxides	-	9	2	1000 900 1080	1000	1200	6800	4400 3500 4400	9	4 3 4	1400	<20 0.25 20	F	1000	0	0
Phosphoric Acid (85%) Heated Bath with Reflux 160°C	Silicon nitrides	-	7	-	0.7	0.8	<1	37	24 9 24	28 28 42	19 19 42	9800	-	-	-	550	390
Silicon Etchant (126 HNO_3 : 60 H_2O : 5 NH_4F) Wet Sink Room Temperature	Silicon	1500	3100 1200 6000	1000	87	W	110	4000	1700	2	3	4000	130	3000	-	0	0
KOH (1 KOH : 2 H_2O by weight) Heated Stirred Bath 80°C	<100> Silicon	14k	>10k	F	77 41 77	-	94	W	380	0	0	F	0	-	-	F	F
Aluminum Etchant Type A (16 H_3PO_4 : 1 HNO_3 : 1 HAc : 2 H_2O) Heated Bath 50°C	Aluminum	-	<10	<9	0	0	0	-	<10	0	2	6600 2600 6600	-	0	-	0	0
Titanium Etchant (20 H_2O : 1 H_2O_2 : 1 HF) Wet Sink Room Temperature	Titanium	-	12	-	120	W	W	W	2100	8	4	W	0 0 <10	8800	-	0	0
H_2O_2 (30%) Wet Sink Room Temperature	Tungsten	-	0	0	0	0	0	0	0	0	0	<20	190 190 1000	0	60 60 150	<2	0
Piranha (~50 H_2SO_4 : 1 H_2O_2) Heated Bath 120°C	Cleaning off metals and organics	-	0	0	0	0	0	-	0	0	0	1800	-	2400	-	F	F
Acetone Wet Sink Room Temperature	Photoresist	-	0	0	0	0	0	-	0	0	0	0	-	0	-	>44k	>39k

Notation: - =test not performed; W=not performed, but known to *Work* (≥ 100 Å/min); F=not performed, but known to be *Fast* (≥ 10 kÅ/min); P=some of film *Peeled* during etch or when rinsed; A=film was visibly *Attacked* and roughened.
Etch areas are all of a 4-inch wafer for the transparent films and half of the wafer for single-crystal silicon and the metals.
Etch rates will vary with temperature and prior use of solution, area of exposure of film, other materials present (e.g., photoresist), film impurities and microstructure, etc. *Some variation should be expected.*

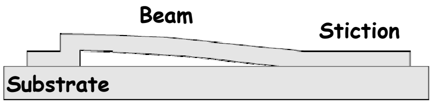
Film Etch Chemistries

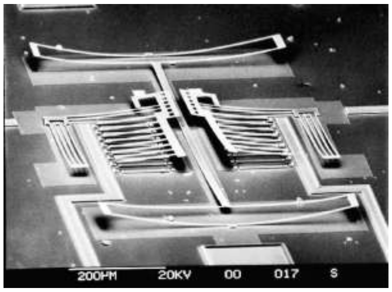
- For some popular films:

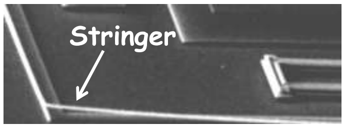
Material	Wet etchant	Etch rate [nm/min]	Dry etchant	Etch rate [nm/min]
Polysilicon	HNO_3:H_2O: NH_4F	120-600	SF_6 + He	170-920
Silicon nitride	H_3PO_4	5	SF_6	150-250
Silicon dioxide	HF	20-2000	CHF_3 + O_2	50-150
Aluminum	H_3PO_4:HNO_3: CH_3COOH	660	Cl_2 + $SiCl_4$	100-150
Photoresist	Acetone	>4000	O_2	35-3500
Gold	KI	40	n/a	n/a

Issues in Surface Micromachining

- Stiction: sticking of released devices to the substrate or to other on-chip structures
  - ↳ Difficult to tell if a structure is stuck to substrate by just looking through a microscope
- Residual Stress in Thin Films
  - ↳ Causes bending or warping of microstructures
  - ↳ Limits the sizes (and sometimes geometries) of structures
- Topography
  - ↳ Stringers can limit the number of structural levels



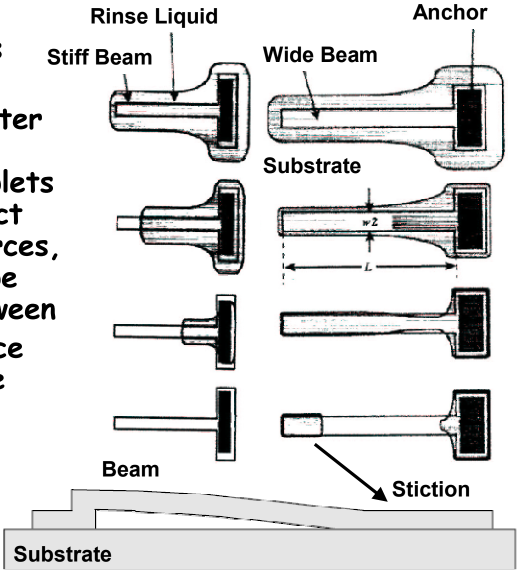


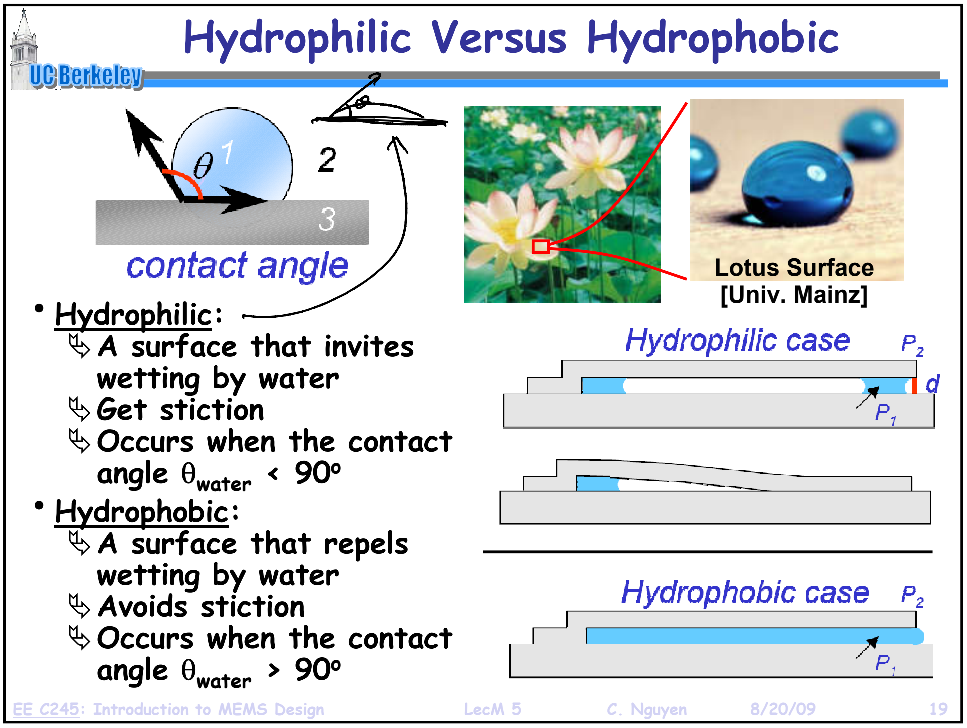


Microstructure Stiction

Microstructure Stiction

- Stiction: the unintended sticking of MEMS surfaces
- Release stiction:
  - ↳ Occurs during drying after a wet release etch
  - ↳ Capillary forces of droplets pull surfaces into contact
  - ↳ Very strong sticking forces, e.g., like two microscope slides w/ a droplet between
- In-use stiction: when device surfaces adhere during use due to:
  - ↳ Capillary condensation
  - ↳ Electrostatic forces
  - ↳ Hydrogen bonding
  - ↳ Van der Waals forces

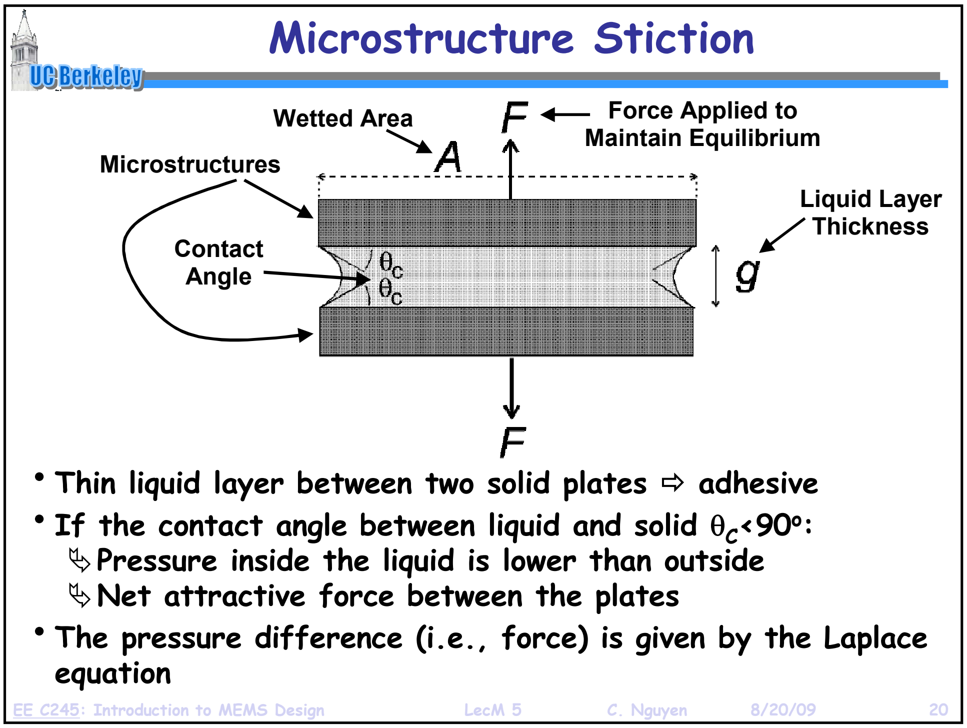




Hydrophilic Versus Hydrophobic

contact angle

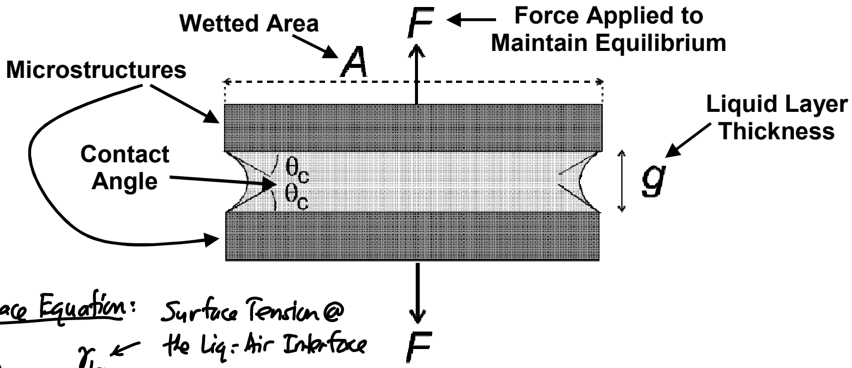
- Hydrophilic:
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle $\theta_{water} < 90^\circ$
- Hydrophobic:
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle $\theta_{water} > 90^\circ$



Microstructure Stiction

- Thin liquid layer between two solid plates ⇨ adhesive
- If the contact angle between liquid and solid $\theta_C < 90^\circ$:
  - Pressure inside the liquid is lower than outside
  - Net attractive force between the plates
- The pressure difference (i.e., force) is given by the Laplace equation

Microstructure Stiction Modeling



Laplace Equation: Surface Tension @ the Liq-Air Interface

$$\Delta P_{la} = \frac{\gamma_{la}}{r}$$

← Radius of Curvature of the Meniscus (-) if concave

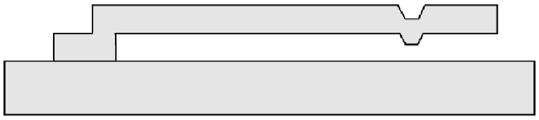
Pressure Difference @ the Liquid-Air Interface

$$\left[r = -\frac{(g/2)}{\cos\theta_c}\right] \Rightarrow \boxed{F = -\Delta P_{la} A = \frac{2A\gamma_{la}\cos\theta_c}{g}}$$

← Force needed to keep the plates apart
⇒ (+) force means a (-) Laplace pressure

Avoiding Stiction

- Reduce droplet area via mechanical design approaches



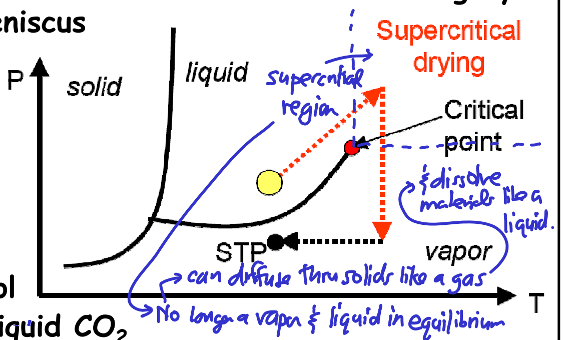
Standoff Bumps

Meniscus-Shaping Features

- Avoid liquid-vapor meniscus formation
  - Use solvents that sublimate
  - Use vapor-phase sacrificial layer etch
- Modify surfaces to change the meniscus shape from concave (small contact angle) to convex (large contact angle)
  - Use teflon-like films
  - Use hydrophobic self-assembled monolayers (SAMs)

Supercritical CO_2 Drying

- A method for stictionless drying of released microstructures by immersing them in CO_2 at its supercritical point
- Basic Strategy: Eliminate surface tension-derived sticking by avoiding a liquid-vapor meniscus
- Procedure:
  - Etch oxide in solution of HF
  - Rinse thoroughly in DI water, but do not dry
  - Transfer the wafer from water to methanol
  - Displace methanol w/ liquid CO_2
  - Apply heat & pressure to take the CO_2 past its critical pt.
  - Vent to lower pressure and allow the supercritical CO_2 to revert to gas → liquid-to-gas Xsition in supercritical region means no capillary forces to cause stiction

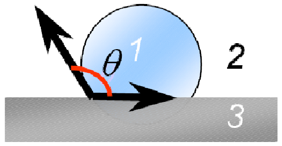


& dissolve materials like a liquid.

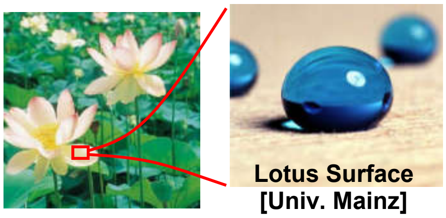
can diffuse thru solids like a gas

No longer a vapor & liquid in equilibrium

Hydrophilic Versus Hydrophobic

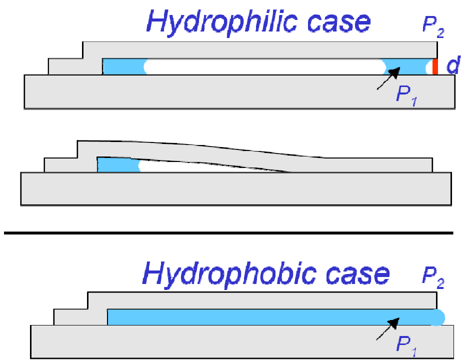


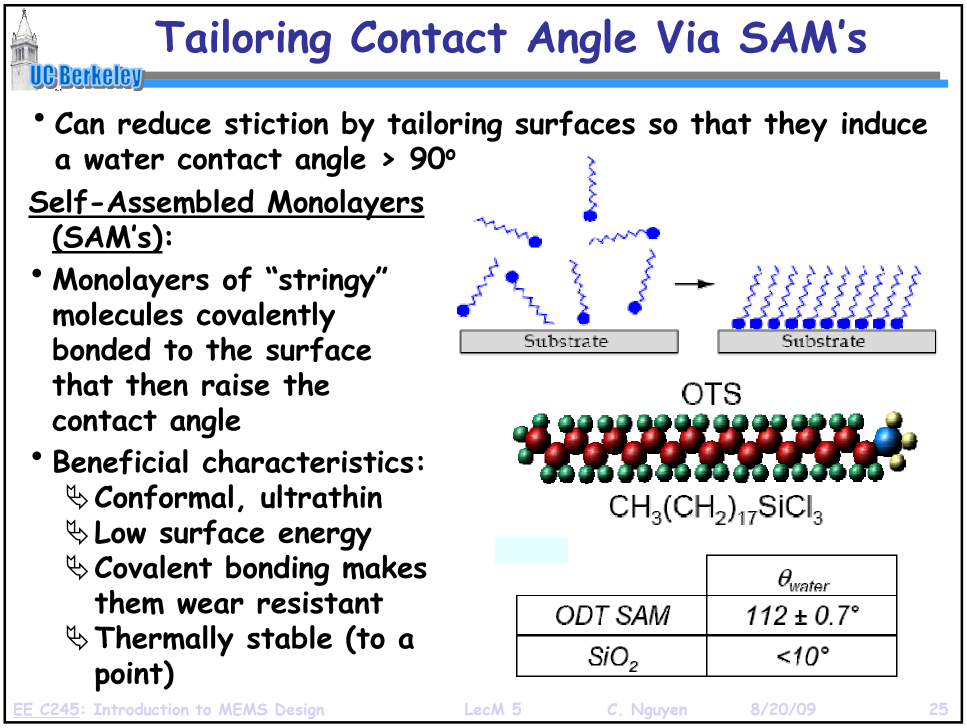
contact angle



Lotus Surface [Univ. Mainz]

- Hydrophilic:
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle θ_{water} < 90°
- Hydrophobic:
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle θ_{water} > 90°





Tailoring Contact Angle Via SAM's

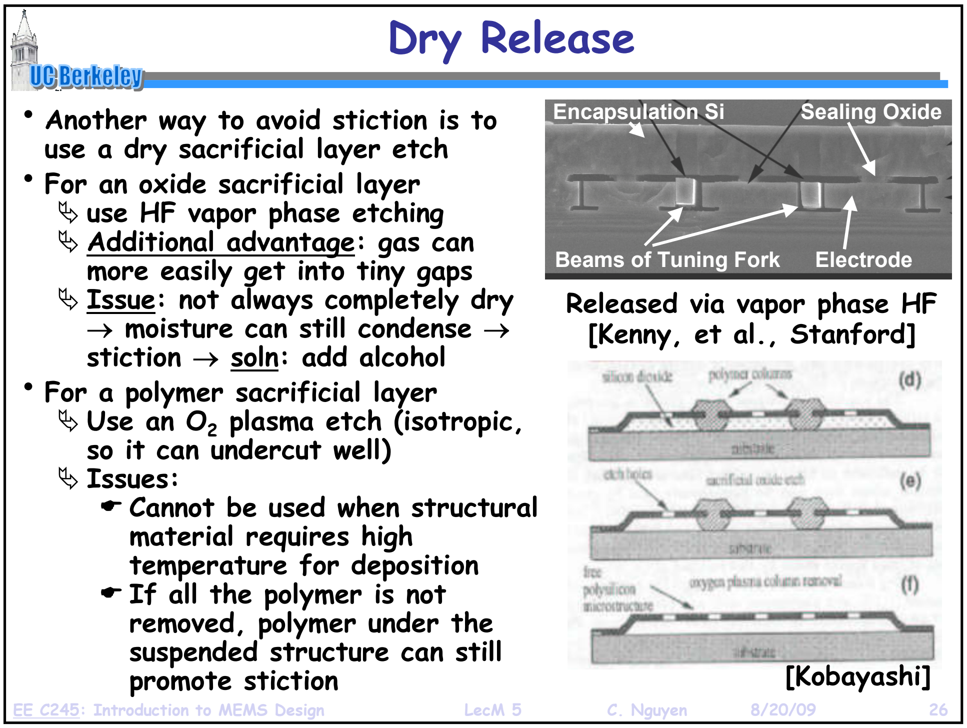
- Can reduce stiction by tailoring surfaces so that they induce a water contact angle > 90°

Self-Assembled Monolayers (SAM's):

- Monolayers of "stringy" molecules covalently bonded to the surface that then raise the contact angle
- Beneficial characteristics:
  - Conformal, ultrathin
  - Low surface energy
  - Covalent bonding makes them wear resistant
  - Thermally stable (to a point)

$CH_3(CH_2)_{17}SiCl_3$

	θ_{water}
ODT SAM	112 ± 0.7°
SiO_2	<10°



Dry Release

- Another way to avoid stiction is to use a dry sacrificial layer etch
- For an oxide sacrificial layer
  - use HF vapor phase etching
  - Additional advantage: gas can more easily get into tiny gaps
  - Issue: not always completely dry → moisture can still condense → stiction → soln: add alcohol
- For a polymer sacrificial layer
  - Use an O_2 plasma etch (isotropic, so it can undercut well)
  - Issues:
    - Cannot be used when structural material requires high temperature for deposition
    - If all the polymer is not removed, polymer under the suspended structure can still promote stiction

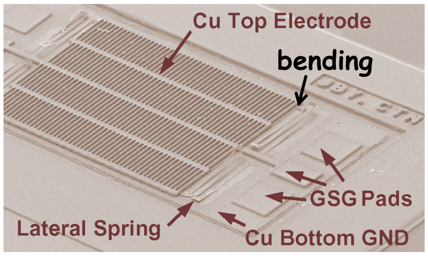
Released via vapor phase HF [Kenny, et al., Stanford]

[Kobayashi]

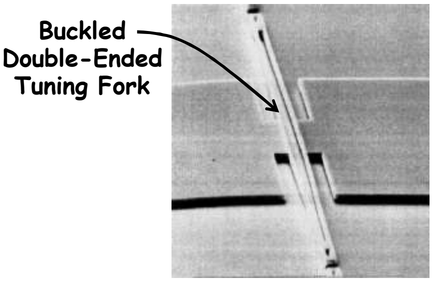
Residual Stress

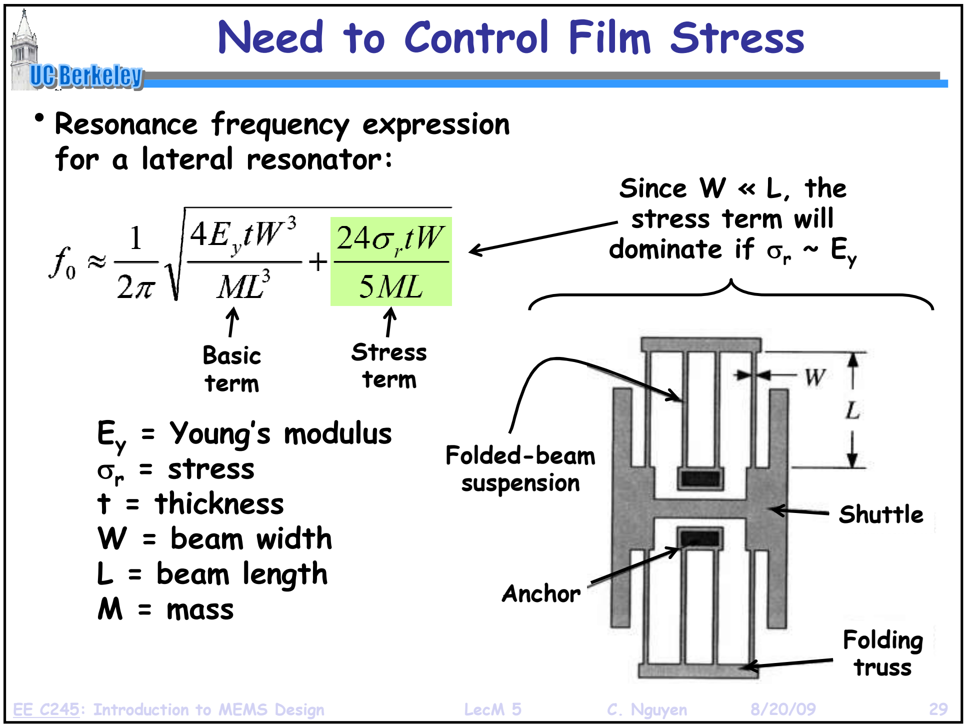
Residual Stress in Thin Films

- After release, poorly designed microstructures might buckle, bend, or warp → often caused by residual film stress
- Origins of residual stress, σ
  - ↳ Growth processes
    - ☛ Non-equilibrium deposition
    - ☛ Grain morphology change
    - ☛ Gas entrapment
    - ☛ Doping
  - ↳ Thermal stresses
    - ☛ Thermal expansion mismatch of materials → introduce stress during cool-down after deposition
    - ☛ Annealing



Tunable Dielectric Capacitor
[Yoon, et al., U. Michigan]





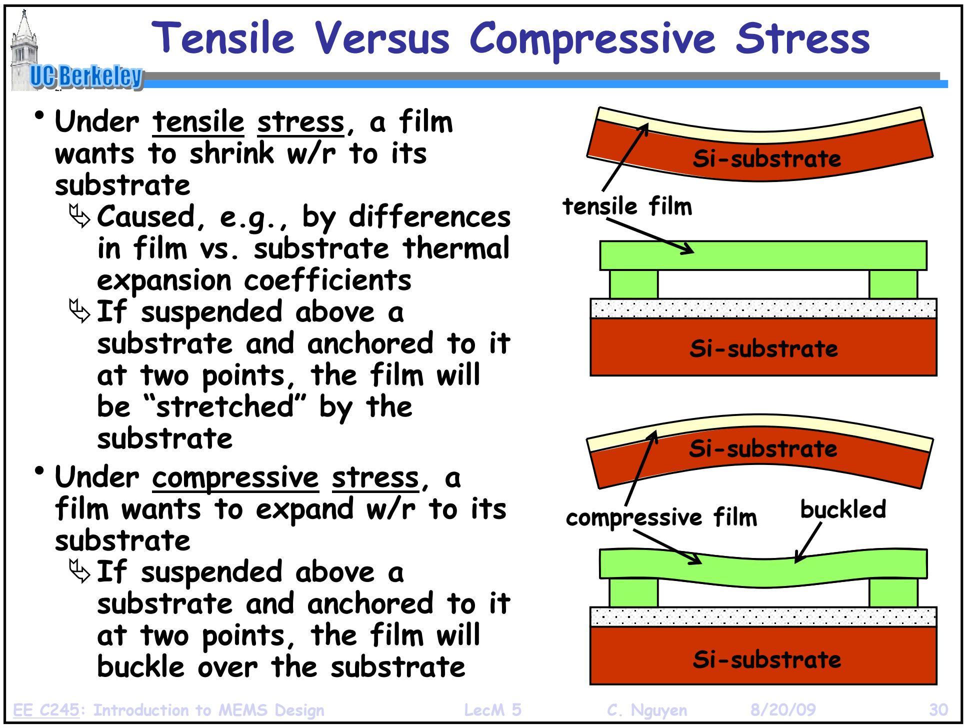
Need to Control Film Stress

- Resonance frequency expression for a lateral resonator:

$$f_0 \approx \frac{1}{2\pi}\sqrt{\underset{\substack{\uparrow\\ \text{Basic}\\ \text{term}}}{\frac{4E_y t W^3}{ML^3}} + \underset{\substack{\uparrow\\ \text{Stress}\\ \text{term}}}{\boxed{\frac{24\sigma_r t W}{5ML}}}}$$

Since W « L, the stress term will dominate if $\sigma_r \sim E_y$

E_y = Young's modulus
σ_r = stress
t = thickness
W = beam width
L = beam length
M = mass

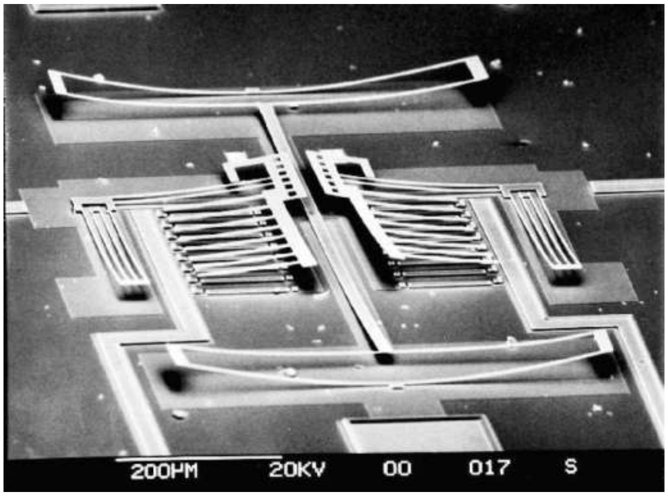


Tensile Versus Compressive Stress

- Under tensile stress, a film wants to shrink w/r to its substrate
  - Caused, e.g., by differences in film vs. substrate thermal expansion coefficients
  - If suspended above a substrate and anchored to it at two points, the film will be "stretched" by the substrate
- Under compressive stress, a film wants to expand w/r to its substrate
  - If suspended above a substrate and anchored to it at two points, the film will buckle over the substrate

Vertical Stress Gradients

- Variation of residual stress in the direction of film growth
- Can warp released structures in z-direction

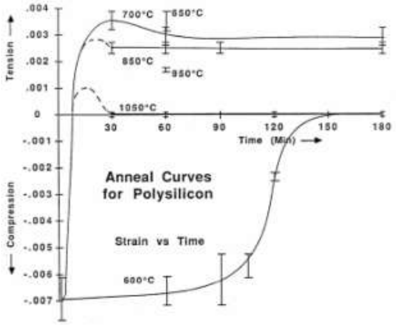


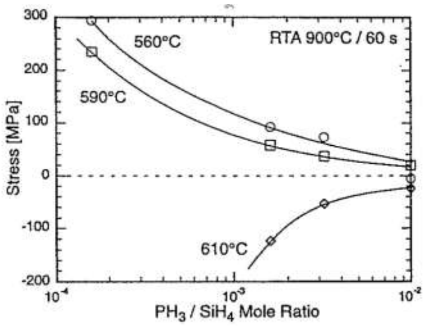
Stress in Polysilicon Films

- Stress depends on crystal structure, which in turn depends upon the deposition temperature
- Temperature ≤ 600°C
  - Films are initially amorphous, then crystallize
  - Get equiaxed crystals, largely isotropic
  - Crystals have higher density → tensile stress
  - Small stress gradient
- Temperature ≥ 600°C
  - Columnar crystals grow during deposition
  - As crystals grow vertically and in-plane they push on neighbors → compressive stress
  - Positive stress gradient

Annealing Out Polysilicon Stress

- Control polySi stress by annealing at high temperatures
  - Typical anneal temperatures: 900-1150°C
  - Grain boundaries move, relax
  - Can dope while annealing by sandwiching the polysilicon between similarly doped oxides (symmetric dopant drive-in), e.g. using 10-15 wt. % PSG

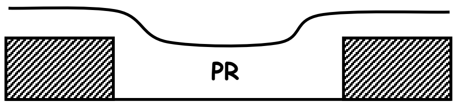




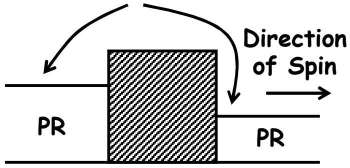
- Rapid thermal anneal (RTA) also effective (surprisingly)

Topography Issues

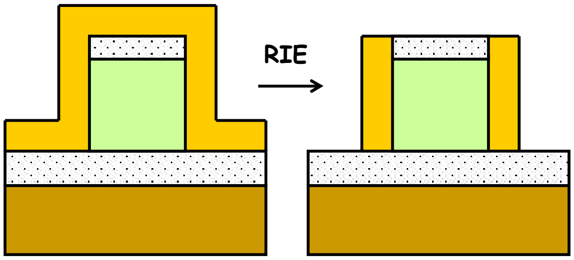
- Degradation of lithographic resolution
  - PR step coverage, streaking

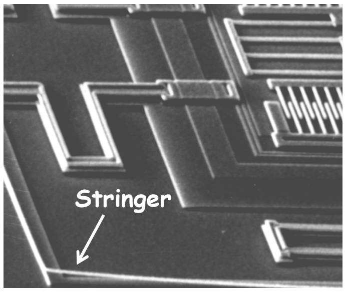


Thickness differences pose problems for reduction steppers



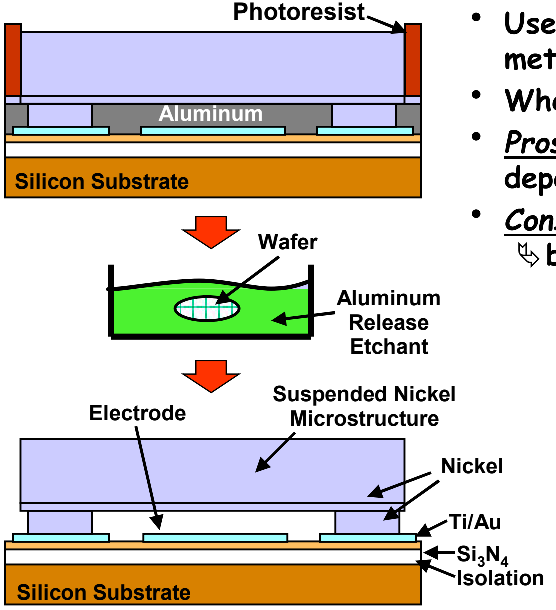
- Stringers
  - Problematic when using anisotropic etching, e.g., RIE



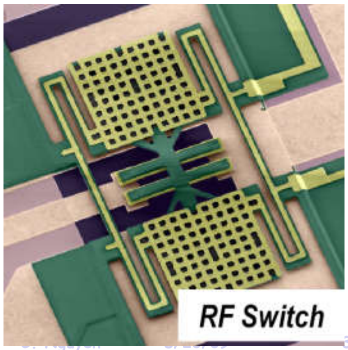


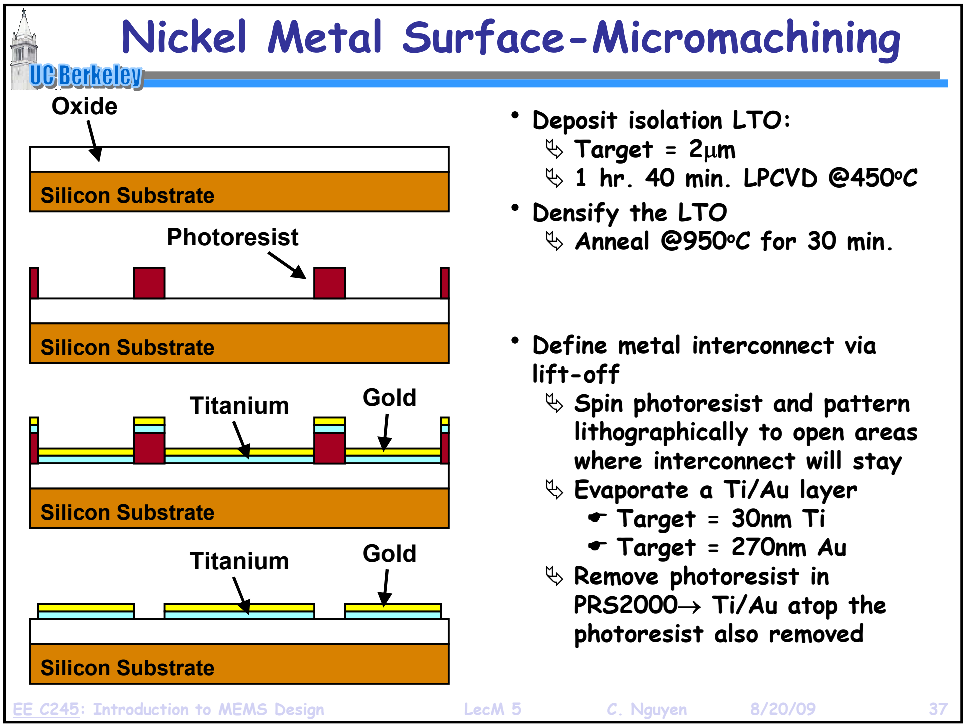
Nickel Surface-Micromachining Process Flow

Electroplating: Metal MEMS



- Use electroplating to obtain metal µstructures
- When thick: call it "LIGA"
- *Pros*: fast low temp deposition, very conductive
- *Cons*: drift, low mech. Q
  - ↳ but may be solvable?





Nickel Metal Surface-Micromachining

- Deposit isolation LTO:
  - Target = $2\mu m$
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO
  - Anneal @950°C for 30 min.
- Define metal interconnect via lift-off
  - Spin photoresist and pattern lithographically to open areas where interconnect will stay
  - Evaporate a Ti/Au layer
    - Target = 30nm Ti
    - Target = 270nm Au
  - Remove photoresist in PRS2000→ Ti/Au atop the photoresist also removed

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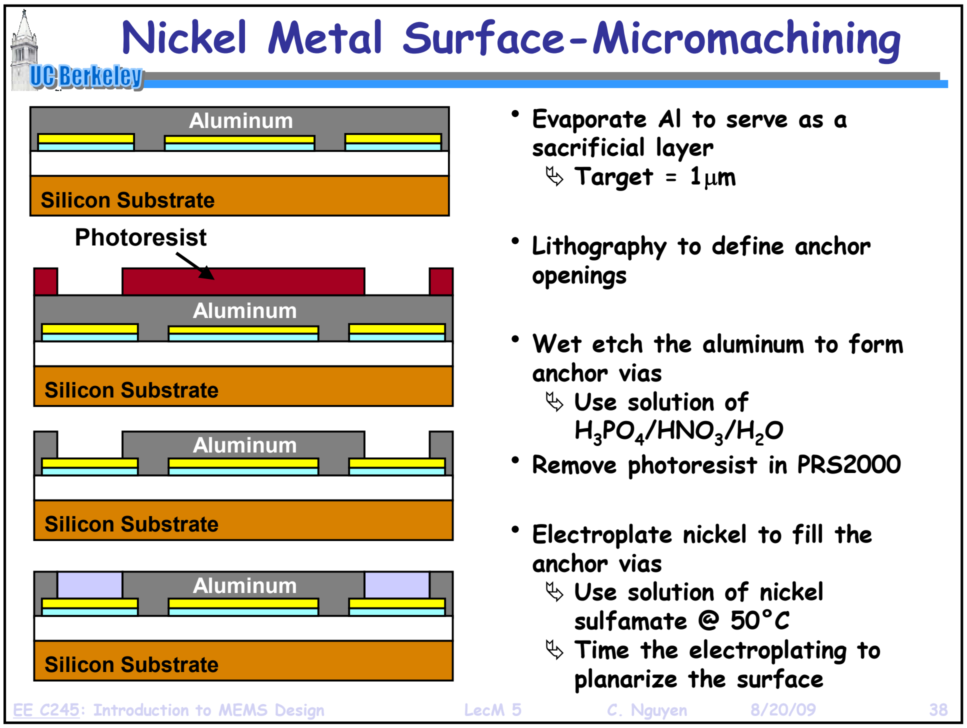

Nickel Metal Surface-Micromachining

- Evaporate Al to serve as a sacrificial layer
  - Target = $1\mu m$
- Lithography to define anchor openings
- Wet etch the aluminum to form anchor vias
  - Use solution of $H_3PO_4/HNO_3/H_2O$
- Remove photoresist in PRS2000
- Electroplate nickel to fill the anchor vias
  - Use solution of nickel sulfamate @ 50°C
  - Time the electroplating to planarize the surface

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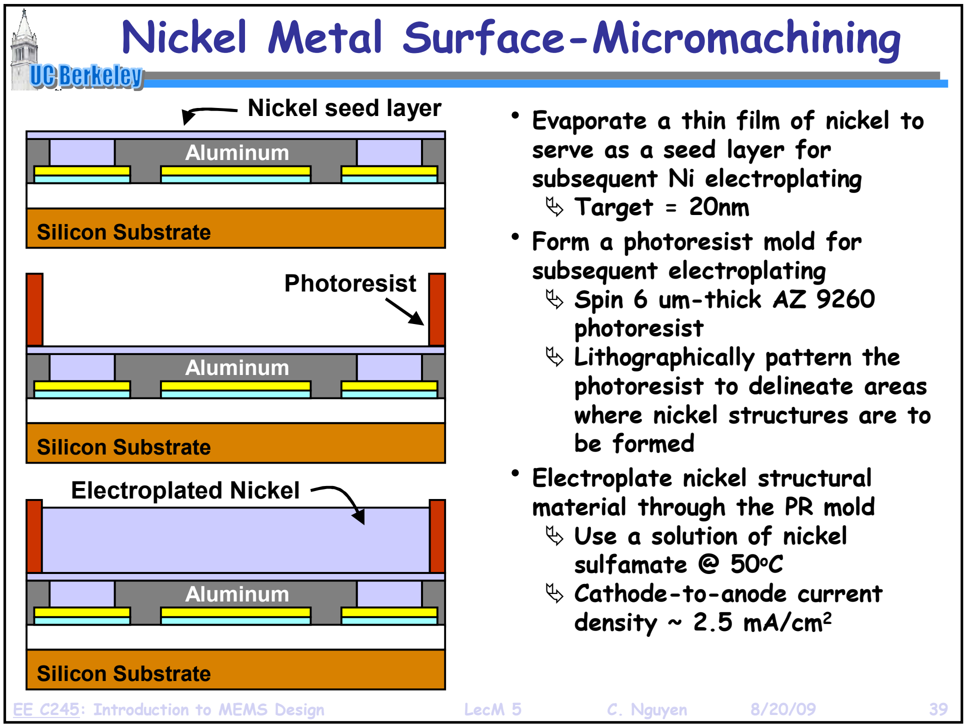
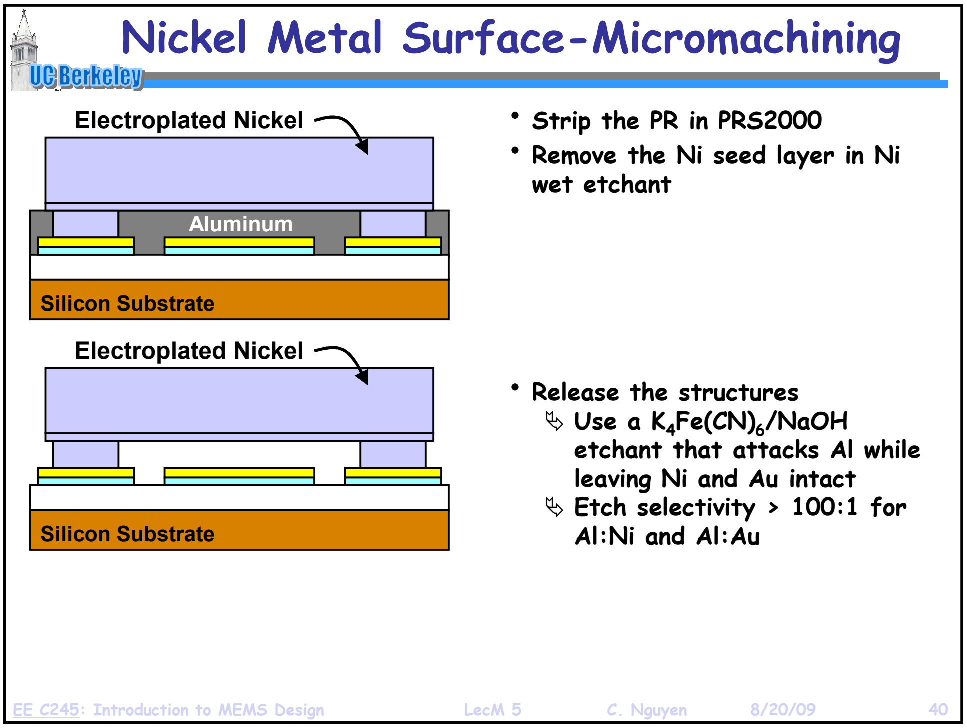


Nickel Metal Surface-Micromachining

- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm^2



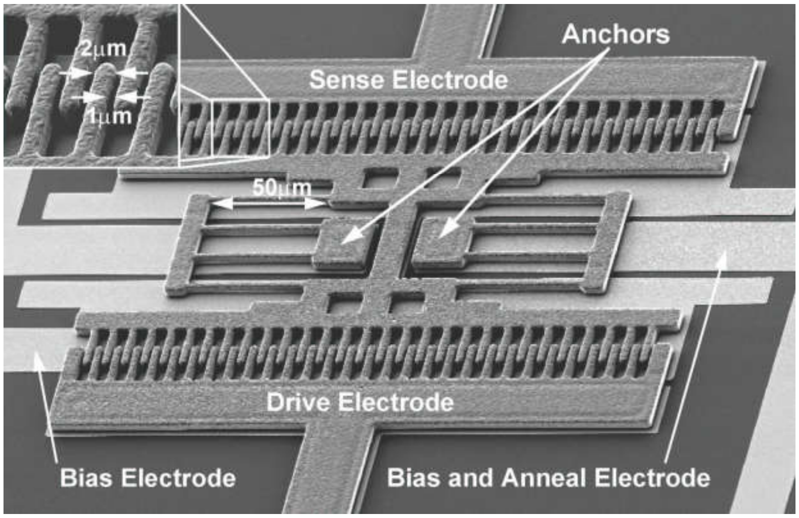
Nickel Metal Surface-Micromachining

- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant

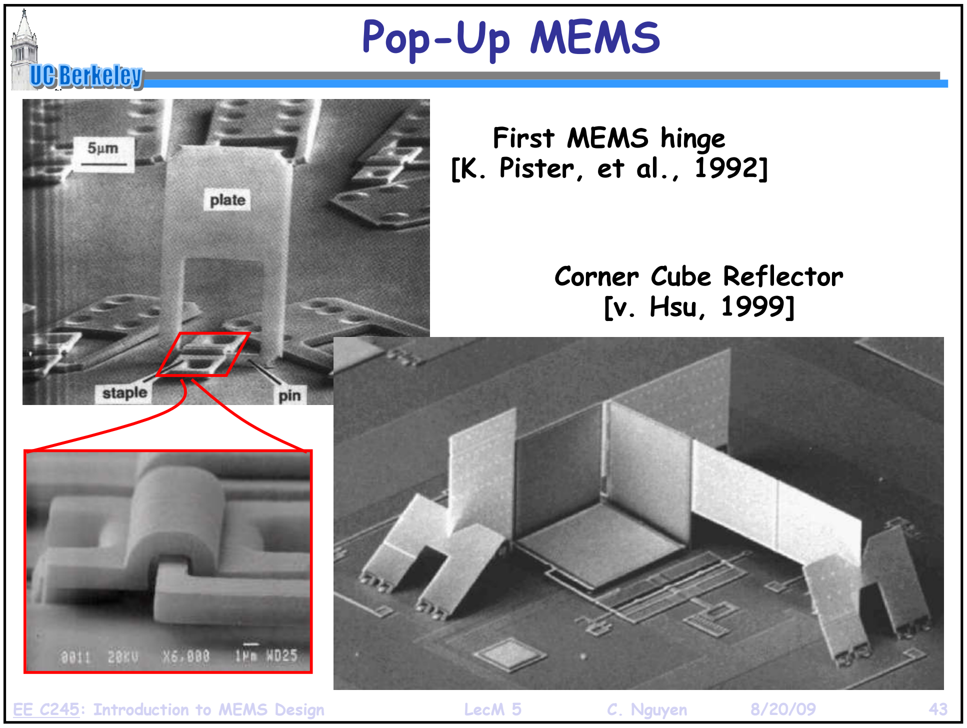
- Release the structures
  - Use a $K_4Fe(CN)_6$/NaOH etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au

Nickel Surface-Micromachining Example

- **Below**: Surface-micromachined in nickel using the described process flow



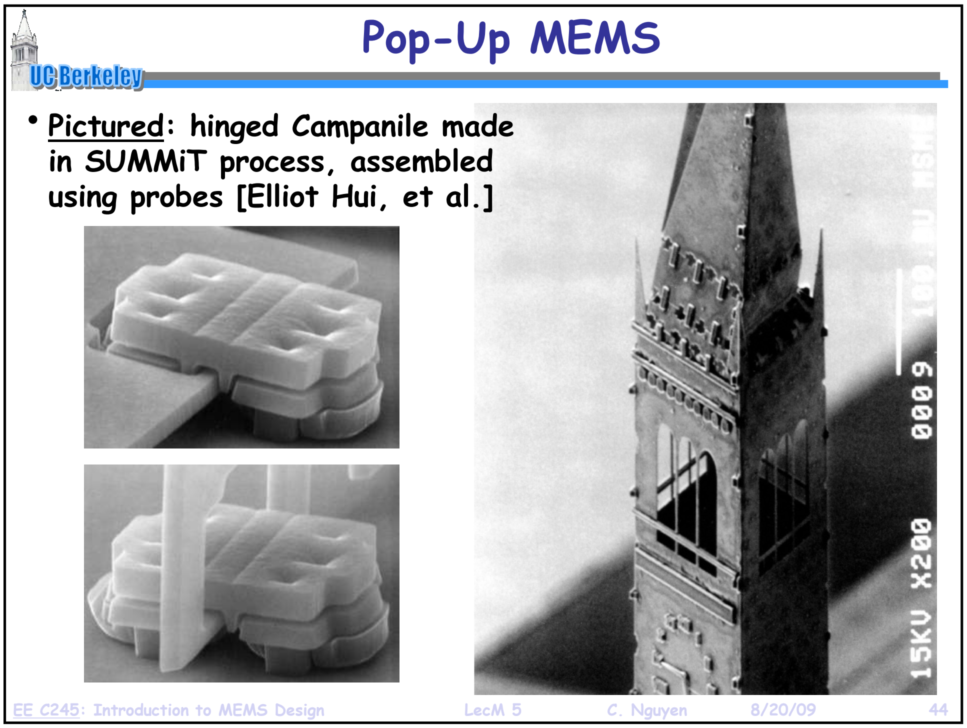
3D "Pop-up" MEMS



Pop-Up MEMS

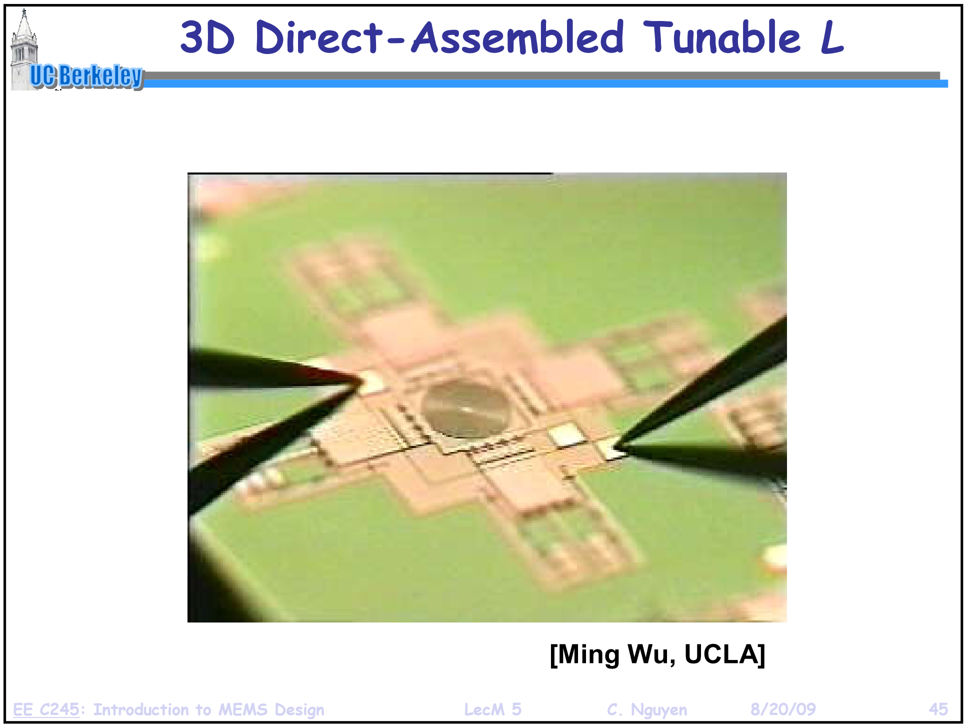
First MEMS hinge
[K. Pister, et al., 1992]

Corner Cube Reflector
[v. Hsu, 1999]



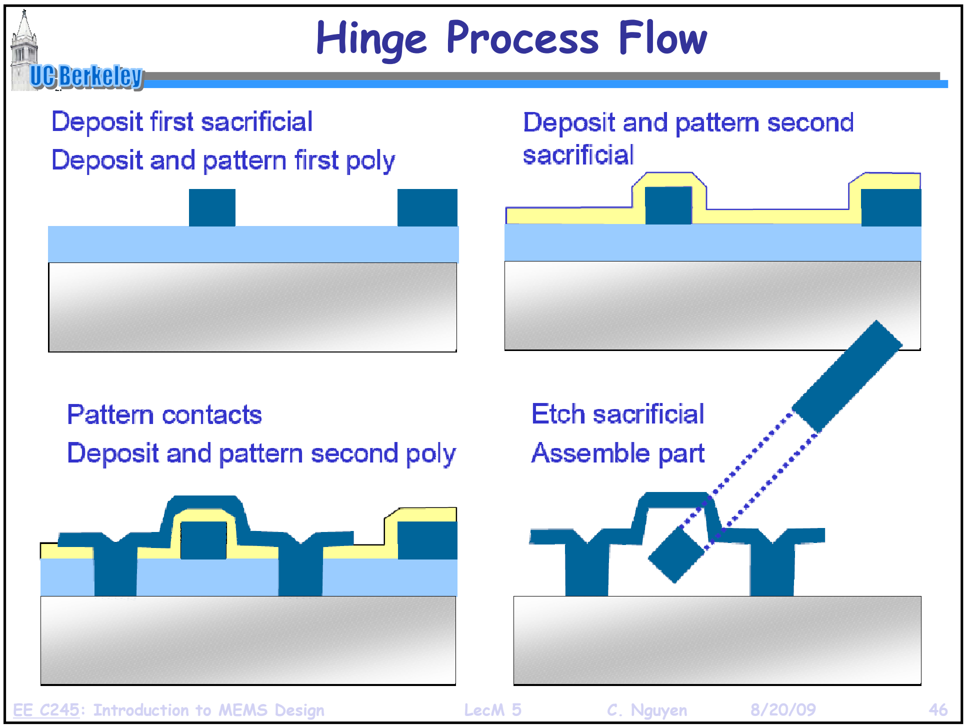
Pop-Up MEMS

- <u>Pictured</u>: hinged Campanile made in SUMMiT process, assembled using probes [Elliot Hui, et al.]



3D Direct-Assembled Tunable L

[Ming Wu, UCLA]



Hinge Process Flow

Deposit first sacrificial
Deposit and pattern first poly

Deposit and pattern second sacrificial

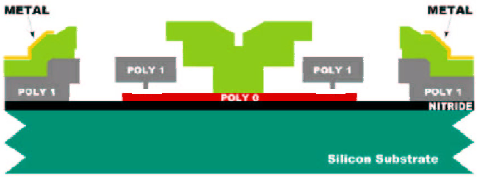
Pattern contacts
Deposit and pattern second poly

Etch sacrificial
Assemble part

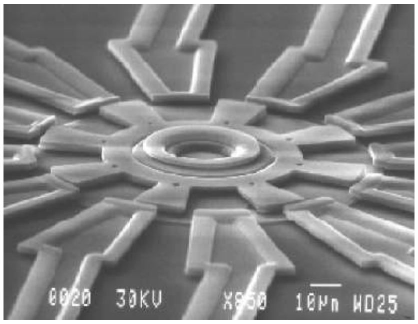
"Foundry" MEMS: The MUMPS Process

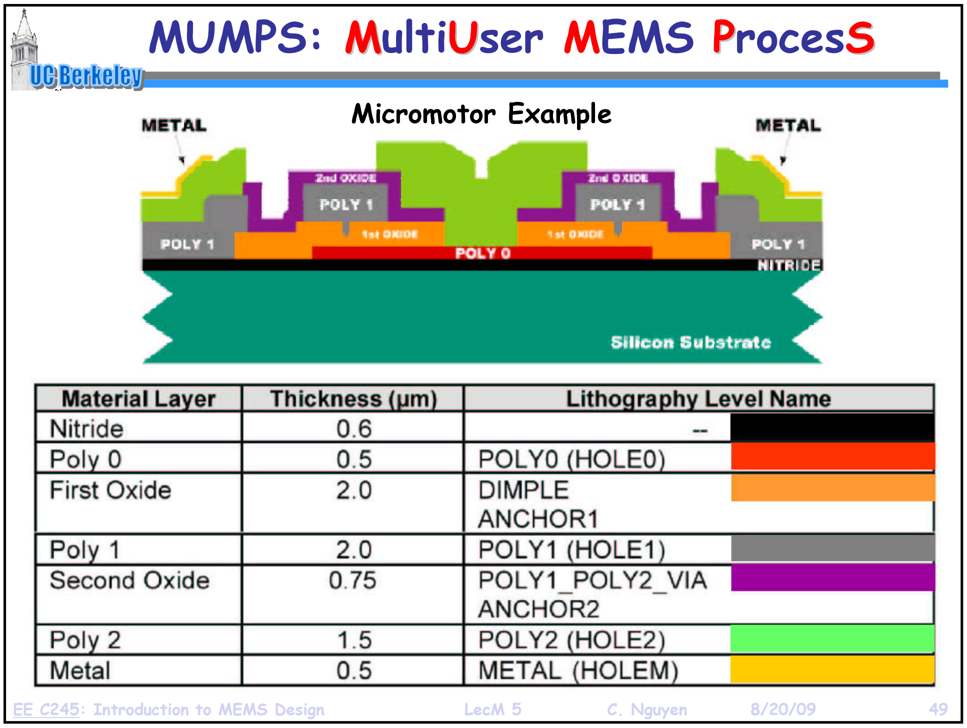
MUMPS: MultiUser MEMS ProcesS

- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm^2 dies



Micromotor fabricated via MUMPS

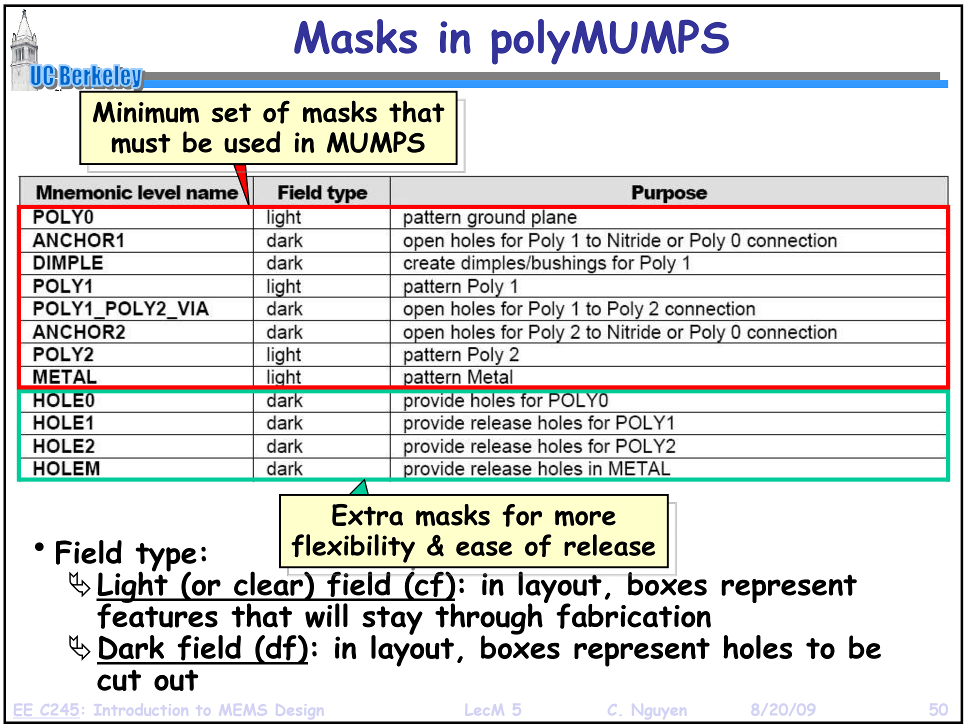




MUMPS: MultiUser MEMS ProcesS

Micromotor Example

Material Layer	Thickness (μm)	Lithography Level Name	
Nitride	0.6	--	⬛
Poly 0	0.5	POLY0 (HOLE0)	🟥
First Oxide	2.0	DIMPLE ANCHOR1	🟧
Poly 1	2.0	POLY1 (HOLE1)	▨
Second Oxide	0.75	POLY1_POLY2_VIA ANCHOR2	🟪
Poly 2	1.5	POLY2 (HOLE2)	🟩
Metal	0.5	METAL (HOLEM)	🟨



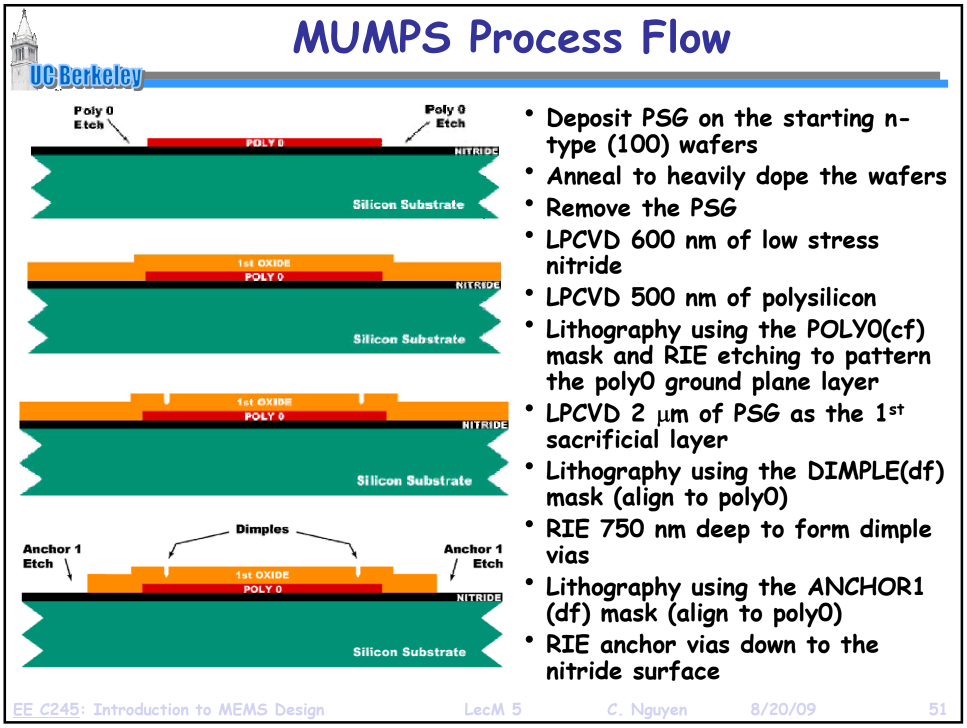
Masks in polyMUMPS

Minimum set of masks that must be used in MUMPS

Mnemonic level name	Field type	Purpose
POLY0	light	pattern ground plane
ANCHOR1	dark	open holes for Poly 1 to Nitride or Poly 0 connection
DIMPLE	dark	create dimples/bushings for Poly 1
POLY1	light	pattern Poly 1
POLY1_POLY2_VIA	dark	open holes for Poly 1 to Poly 2 connection
ANCHOR2	dark	open holes for Poly 2 to Nitride or Poly 0 connection
POLY2	light	pattern Poly 2
METAL	light	pattern Metal
HOLE0	dark	provide holes for POLY0
HOLE1	dark	provide release holes for POLY1
HOLE2	dark	provide release holes for POLY2
HOLEM	dark	provide release holes in METAL

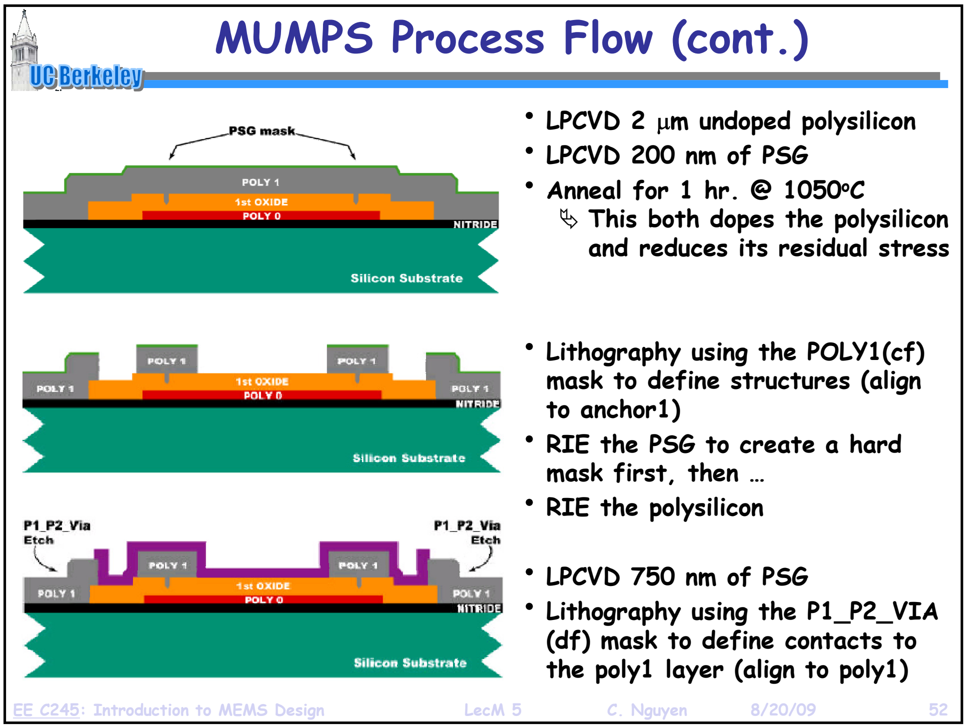
Extra masks for more flexibility & ease of release

- Field type:
  - Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
  - Dark field (df): in layout, boxes represent holes to be cut out



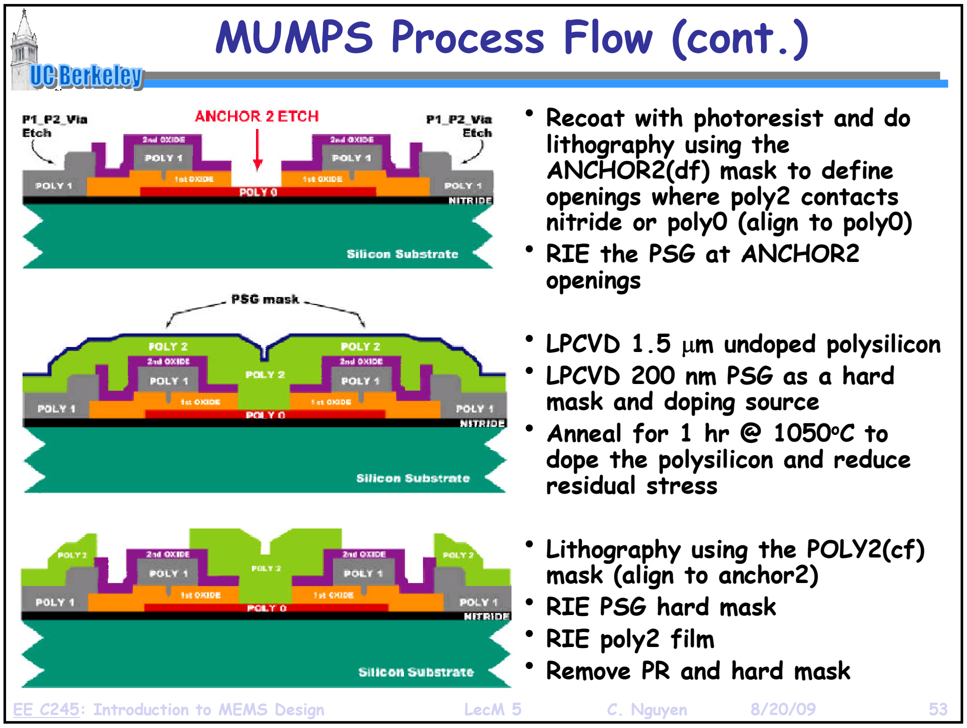
MUMPS Process Flow

- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 μm of PSG as the 1st sacrificial layer
- Lithography using the DIMPLE(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1 (df) mask (align to poly0)
- RIE anchor vias down to the nitride surface



MUMPS Process Flow (cont.)

- LPCVD 2 μm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  - ↳ This both dopes the polysilicon and reduces its residual stress
- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then …
- RIE the polysilicon
- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA (df) mask to define contacts to the poly1 layer (align to poly1)

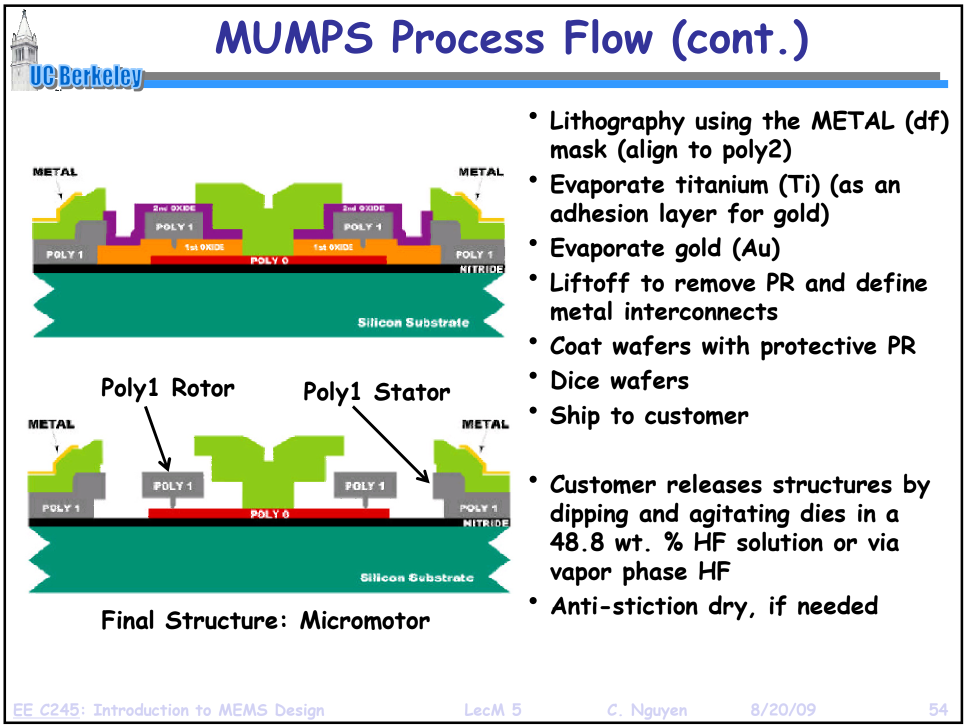


MUMPS Process Flow (cont.)

- Recoat with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings

- LPCVD 1.5 μm undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress

- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask



MUMPS Process Flow (cont.)

Final Structure: Micromotor

- Lithography using the METAL (df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer

- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed

MUMPS: MultiUser MEMS ProcesS

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- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
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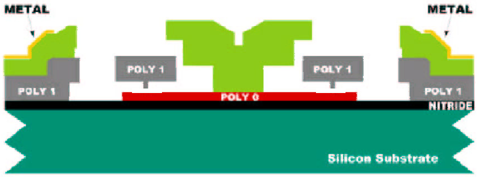
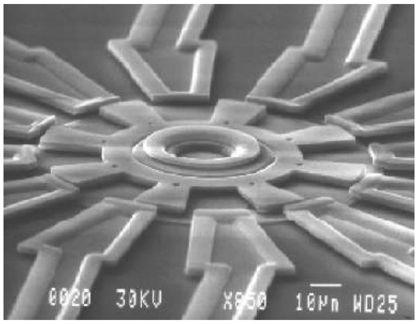


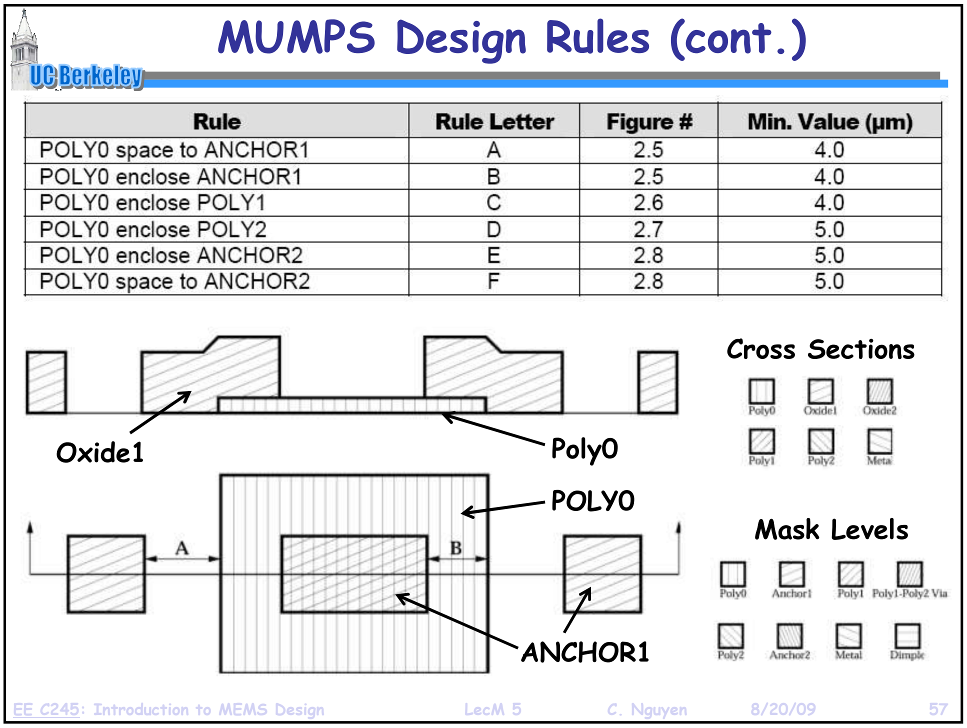
Micromotor fabricated via MUMPS



polyMUMPS Minimum Feature Constraints

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

	Nominal [µm]	Min Feature [µm]	Min Spacing [µm]
POLY0, POLY1, POLY2	3	2	2
POLY1_POLY2_VIA	3	2	2
ANCHOR1, ANCHOR2	3	3	2
DIMPLE	3	2	3
METAL	3	3	3
HOLE1, HOLE2	4	3	3
HOLEM	5	4	4



MUMPS Design Rules (cont.)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0

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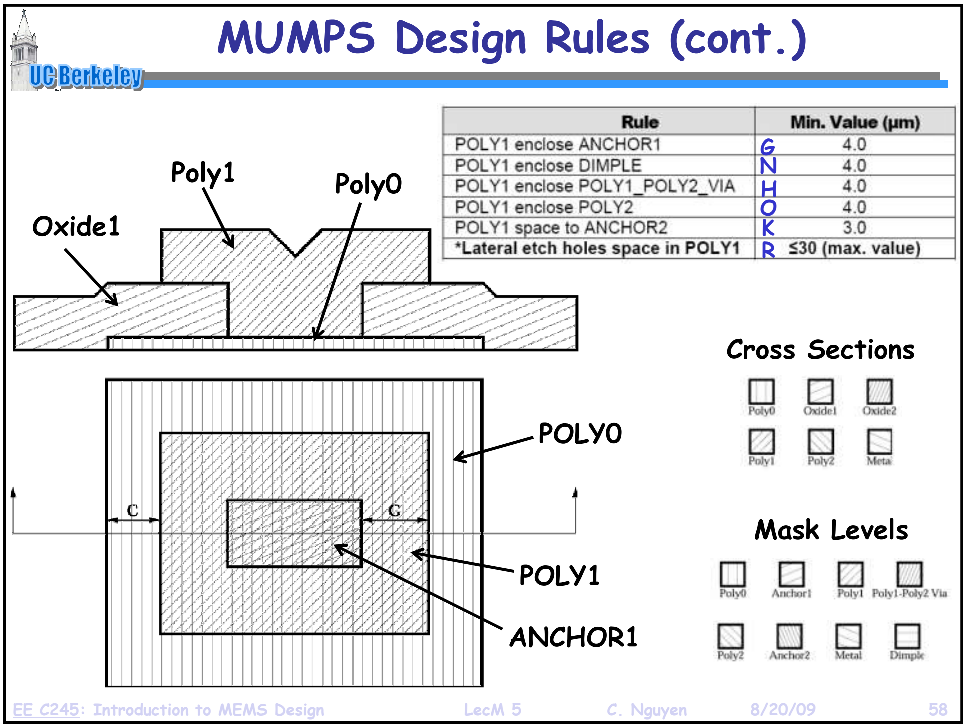

MUMPS Design Rules (cont.)

Rule		Min. Value (μm)
POLY1 enclose ANCHOR1	G	4.0
POLY1 enclose DIMPLE	N	4.0
POLY1 enclose POLY1_POLY2_VIA	H	4.0
POLY1 enclose POLY2	O	4.0
POLY1 space to ANCHOR2	K	3.0
*Lateral etch holes space in POLY1	R	≤30 (max. value)

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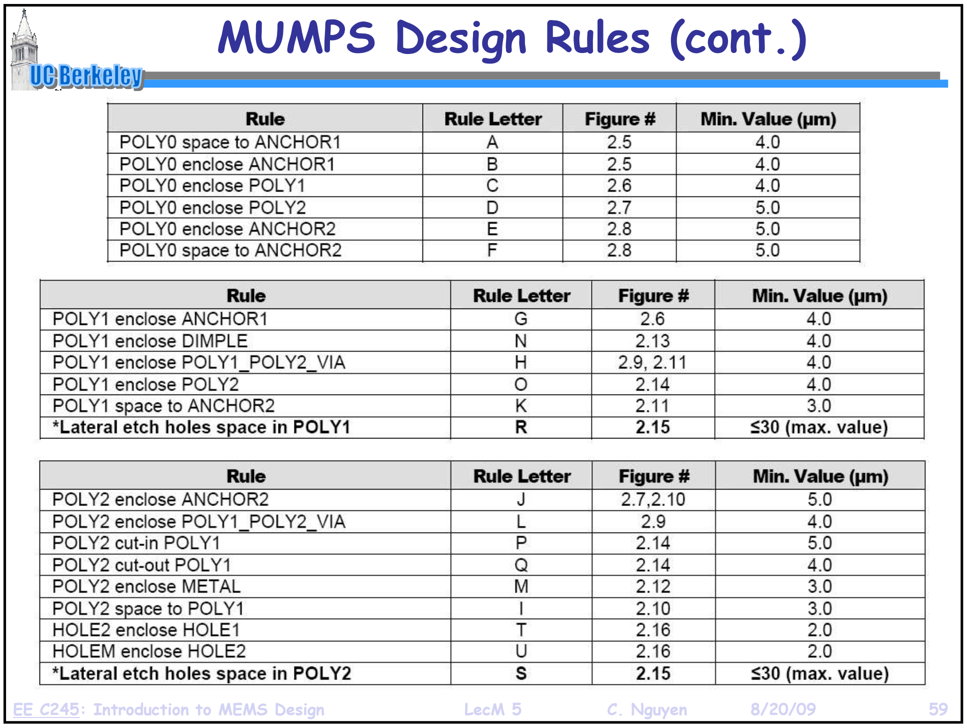
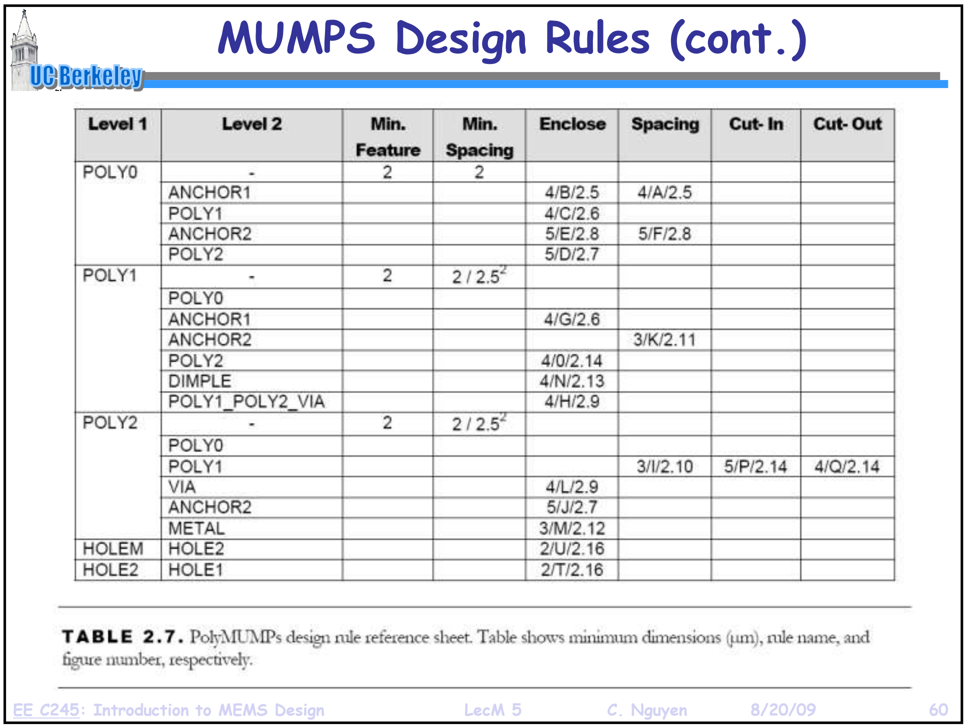


MUMPS Design Rules (cont.)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY1 enclose ANCHOR1	G	2.6	4.0
POLY1 enclose DIMPLE	N	2.13	4.0
POLY1 enclose POLY1_POLY2_VIA	H	2.9, 2.11	4.0
POLY1 enclose POLY2	O	2.14	4.0
POLY1 space to ANCHOR2	K	2.11	3.0
***Lateral etch holes space in POLY1**	**R**	**2.15**	**≤30 (max. value)**

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY2 enclose ANCHOR2	J	2.7,2.10	5.0
POLY2 enclose POLY1_POLY2_VIA	L	2.9	4.0
POLY2 cut-in POLY1	P	2.14	5.0
POLY2 cut-out POLY1	Q	2.14	4.0
POLY2 enclose METAL	M	2.12	3.0
POLY2 space to POLY1	I	2.10	3.0
HOLE2 enclose HOLE1	T	2.16	2.0
HOLEM enclose HOLE2	U	2.16	2.0
***Lateral etch holes space in POLY2**	**S**	**2.15**	**≤30 (max. value)**

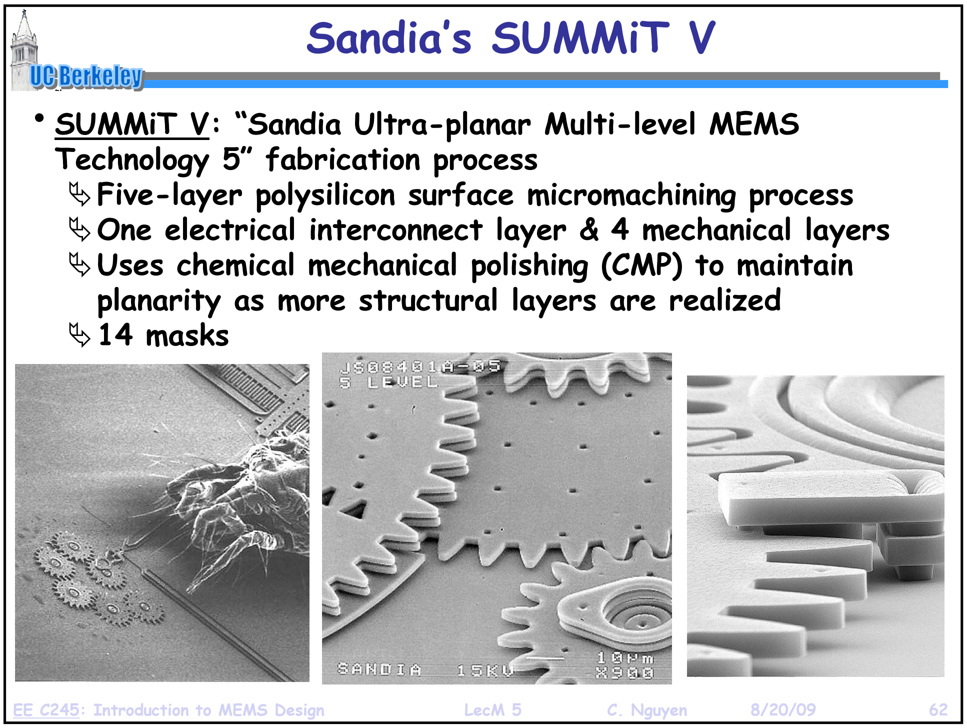


MUMPS Design Rules (cont.)

Level 1	Level 2	Min. Feature	Min. Spacing	Enclose	Spacing	Cut- In	Cut- Out
POLY0	-	2	2				
	ANCHOR1			4/B/2.5	4/A/2.5		
	POLY1			4/C/2.6			
	ANCHOR2			5/E/2.8	5/F/2.8		
	POLY2			5/D/2.7			
POLY1	-	2	$2 / 2.5^2$				
	POLY0						
	ANCHOR1			4/G/2.6			
	ANCHOR2				3/K/2.11		
	POLY2			4/0/2.14			
	DIMPLE			4/N/2.13			
	POLY1_POLY2_VIA			4/H/2.9			
POLY2	-	2	$2 / 2.5^2$				
	POLY0						
	POLY1				3/I/2.10	5/P/2.14	4/Q/2.14
	VIA			4/L/2.9			
	ANCHOR2			5/J/2.7			
	METAL			3/M/2.12			
HOLEM	HOLE2			2/U/2.16			
HOLE2	HOLE1			2/T/2.16			

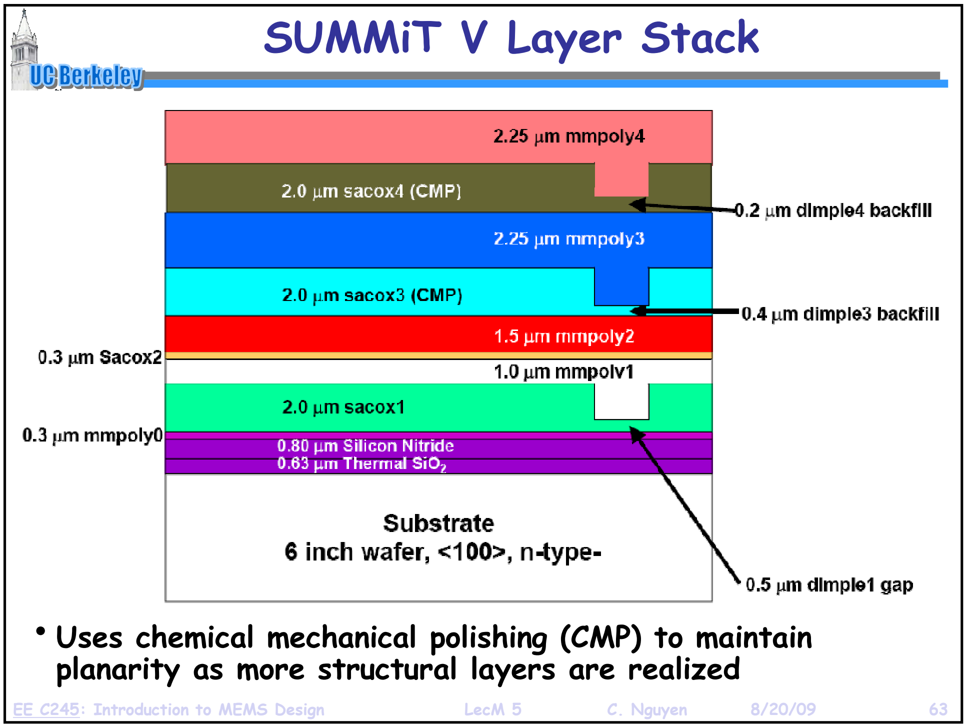
TABLE 2.7. PolyMUMPs design rule reference sheet. Table shows minimum dimensions (μm), rule name, and figure number, respectively.

The Sandia SUMMIT Process



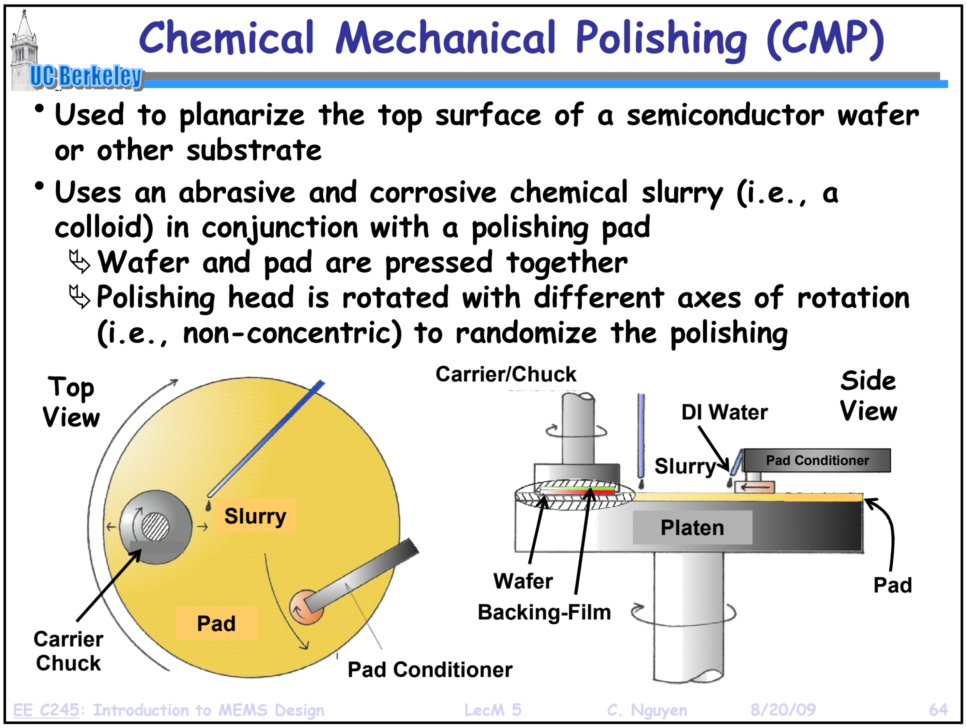
Sandia's SUMMiT V

- SUMMiT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process
  - Five-layer polysilicon surface micromachining process
  - One electrical interconnect layer & 4 mechanical layers
  - Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  - 14 masks



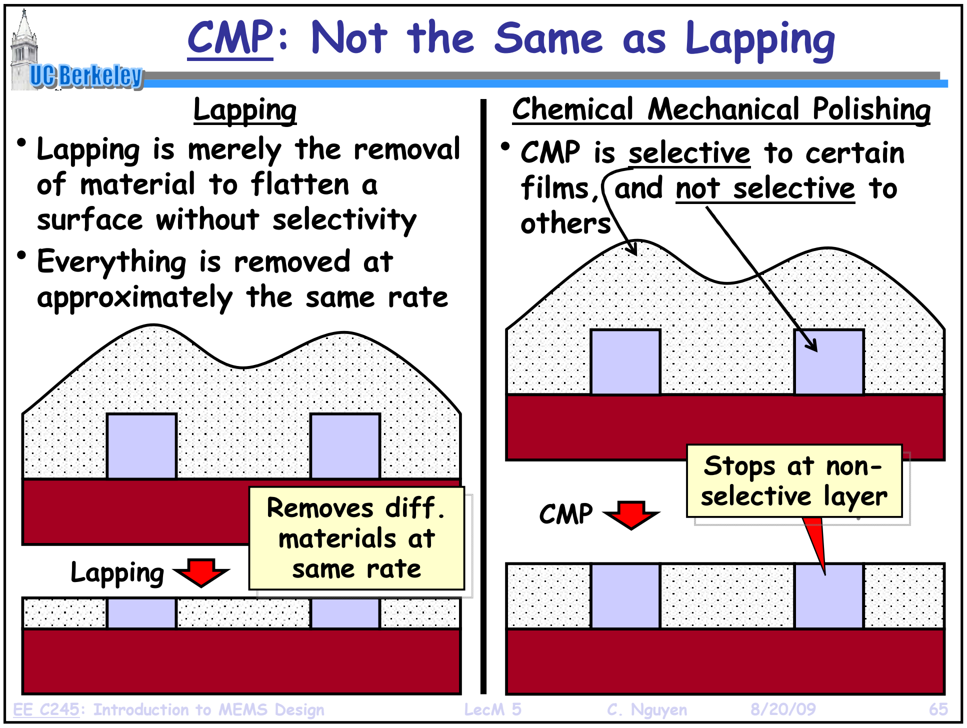
SUMMiT V Layer Stack

- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized



Chemical Mechanical Polishing (CMP)

- Used to planarize the top surface of a semiconductor wafer or other substrate
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad
  - Wafer and pad are pressed together
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing



CMP: Not the Same as Lapping

Lapping

- Lapping is merely the removal of material to flatten a surface without selectivity
- Everything is removed at approximately the same rate

Removes diff. materials at same rate

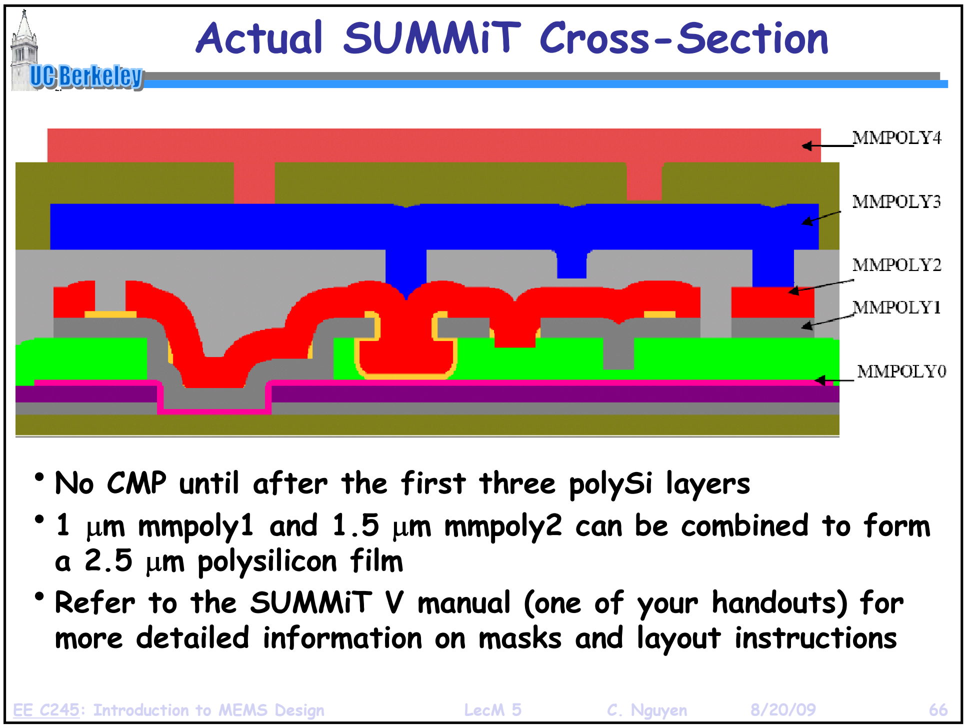
Lapping

Chemical Mechanical Polishing

- CMP is selective to certain films, and not selective to others

Stops at non-selective layer

CMP



Actual SUMMiT Cross-Section

- No CMP until after the first three polySi layers
- 1 μm mmpoly1 and 1.5 μm mmpoly2 can be combined to form a 2.5 μm polysilicon film
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions