Lecture Module 5: Surface Micromachining

Lecture Outline

* Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: “Surface Micromachining for Microelectromechanical Systems”

* Lecture Topics:
  - Polysilicon surface micromachining
  - Stiction
  - Residual stress
  - Topography issues
  - Nickel metal surface micromachining
  - 3D “pop-up” MEMS
  - Foundry MEMS: the “MUMPS” process
  - The Sandia SUMMIT process
Polysilicon Surface-Micromachining

- Uses IC fabrication instrumentation exclusively
- Variations: sacrificial layer thickness, fine- vs. large-grained polysilicon, in situ vs. POCL$_3$-doping

300 kHz Folded-Beam Micromechanical Resonator

Polysilicon
Why Polysilicon?

- Compatible with IC fabrication processes
  - Process parameters for gate polysilicon well known
  - Only slight alterations needed to control stress for MEMS applications
- Stronger than stainless steel: fracture strength of polySi ~ 2-3 GPa, steel ~ 0.2GPa-1GPa
- Young's Modulus ~ 140-190 GPa
- Extremely flexible: maximum strain before fracture ~ 0.5%
- Does not fatigue readily

- Several variations of polysilicon used for MEMS
  - LPCVD polysilicon deposited undoped, then doped via ion implantation, PSG source, POCl₃, or B-source doping
  - In situ-doped LPCVD polysilicon
  - Attempts made to use PECVD silicon, but quality not very good (yet) → etches too fast in HF, so release is difficult

Polysilicon Surface-Micromachining Process Flow
Layout and Masking Layers

- At Left: Layout for a folded-beam capacitive comb-driven micromechanical resonator
- Masking Layers:
  - 1\textsuperscript{st} Polysilicon: POLY1(cf)
  - 2\textsuperscript{nd} Polysilicon: POLY2(cf)
  - Anchor Opening: ANCHOR(df)
  - Capacitive comb-drive for linear actuation
  - Folded-beam support structure for stress relief

Surface-Micromachining Process Flow

1. Deposit isolation LTO (or PSG):
   - Target = 2\textmu m
   - 1 hr. 40 min. LPCVD @450\degree C

2. Densify the LTO (or PSG):
   - Anneal @950\degree C for 30 min.

3. Deposit nitride:
   - Target = 100nm
   - 22 min. LPCVD @800\degree C

4. Deposit interconnect polySi:
   - Target = 300nm
   - In-situ Phosphorous-doped
   - 1 hr. 30 min. LPCVD @650\degree C

5. Lithography to define poly1 interconnects using the POLY1(cf) mask

6. RIE polysilicon interconnects:
   - CCl\textsubscript{4}/He/O\textsubscript{2} @300W, 280mTorr

7. Remove photoresist in PRS2000
Surface-Micromachining Process Flow

- Deposit sacrificial PSG:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the PSG
- Anneal @950°C for 30 min.
- Lithography to define anchors using the ANCHOR(df) mask
  - Align to the poly1 layer
- Etch anchors
  - RIE using CHF₃/CF₄/He @350W, 2.8Torr
  - Remove PR in PRS2000
  - Quick wet dip in 10:1 HF to remove native oxide
- Deposit structural polySi
  - Target = 2μm
  - In-situ Phosphorous-doped
  - 11 hrs. LPCVD @650°C

Surface-Micromachining Process Flow

- Deposit oxide hard mask
  - Target = 500nm
  - 25 min. LPCVD @450°C
- Stress Anneal
  - 1 hr @ 1050°C
  - Or RTA for 1 min. @ 1100°C in 50 sccm N₂
- Lithography to define poly2 structure (e.g., shuttle, springs, drive & sense electrodes) using the POLY2(cf) mask
  - Align to the anchor layer
  - Hard bake the PR longer to make it stronger
- Etch oxide mask first
  - RIE using CHF₃/CF₄/He @350W, 2.8Torr
  - Etch structural polyisilicon
    - RIE using CCl₄/He/O₂ @300W, 280mTorr
    - Use 1 min. etch/1 min. rest increments to prevent excessive temperature
Surface-Micromachining Process Flow

- Remove PR (more difficult)
  - Ash in O$_2$ plasma
  - Soak in PRS2000
- Release the structures
  - Wet etch in HF for a calculated time that insures complete undercutting
    - If 5:1 BHF, then ~ 30 min.
    - If 48.8 wt. % HF, ~ 1 min.
- Keep structures submerged in DI water after the etch
- Transfer structures to methanol
- Supercritical CO$_2$ dry release

Polysilicon Surface-Micromachined Examples

- Below: All surface-micromachined in polysilicon using variants of the described process flow

- Free-Free Beam Resonator
- Folded-Beam Comb-Driven Resonator
- Three-Resonator Micromechanical Filter
### Structural/Sacrificial Material Combinations

<table>
<thead>
<tr>
<th>Structural Material</th>
<th>Sacrificial Material</th>
<th>Etchant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-Si</td>
<td>SiO₂, PSG, LTO</td>
<td>HF, BHF</td>
</tr>
<tr>
<td>Al</td>
<td>Photoresist</td>
<td>O₂ plasma</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Poly-Si</td>
<td>XeF₂</td>
</tr>
<tr>
<td>Al</td>
<td>Si</td>
<td>TMAH, XeF₂</td>
</tr>
<tr>
<td>Poly-SiGe</td>
<td>Poly-Ge</td>
<td>H₂O₂, hot H₂O</td>
</tr>
</tbody>
</table>

- Must consider other layers, too, as release etchants generally have a finite E.R. on any material
- Ex: concentrated HF (48.8 wt. %)
  - Polysilicon E.R. ~ 0
  - Silicon nitride E.R. ~ 1-14 nm/min
  - Wet thermal SiO₂ ~ 1.8-2.3 μm/min
  - Annealed PSG ~ 3.6 μm/min
  - Aluminum (Si rich) ~ 4 nm/min (much faster in other Al)

### Wet Etch Rates (f/K. Williams)

<table>
<thead>
<tr>
<th>Material</th>
<th>Etch Rate (μm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-Si</td>
<td>1.8-2.3</td>
</tr>
<tr>
<td>Silicon nitride</td>
<td>3.6</td>
</tr>
<tr>
<td>Aluminum (Si rich)</td>
<td>4</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>~ 0</td>
</tr>
<tr>
<td>Wet thermal SiO₂</td>
<td>~ 1.8-2.3</td>
</tr>
<tr>
<td>Annealed PSG</td>
<td>3.6</td>
</tr>
<tr>
<td>TMAH</td>
<td>~ 0.6</td>
</tr>
<tr>
<td>XeF₂</td>
<td>~ 0.5</td>
</tr>
<tr>
<td>HF</td>
<td>~ 0.2</td>
</tr>
</tbody>
</table>

- Must consider other layers, too, as release etchants generally have a finite E.R. on any material
- Ex: concentrated HF (48.8 wt. %)
  - Polysilicon E.R. ~ 0
  - Silicon nitride E.R. ~ 1-14 nm/min
  - Wet thermal SiO₂ ~ 1.8-2.3 μm/min
  - Annealed PSG ~ 3.6 μm/min
  - Aluminum (Si rich) ~ 4 nm/min (much faster in other Al)
Film Etch Chemistries

* For some popular films:

<table>
<thead>
<tr>
<th>Material</th>
<th>Wet etchant</th>
<th>Etch rate [nm/min]</th>
<th>Dry etchant</th>
<th>Etch rate [nm/min]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polysilicon</td>
<td>HNO₃:H₂O:NH₄F</td>
<td>120-600</td>
<td>SF₆ + He</td>
<td>170-920</td>
</tr>
<tr>
<td>Silicon nitride</td>
<td>H₃PO₄</td>
<td>5</td>
<td>SF₆</td>
<td>150-250</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>HF</td>
<td>20-2000</td>
<td>CHF₃ + O₂</td>
<td>50-150</td>
</tr>
<tr>
<td>Aluminum</td>
<td>H₃PO₄:HNO₃:CH₃COOH</td>
<td>660</td>
<td>Cl₂ + SiCl₄</td>
<td>100-150</td>
</tr>
<tr>
<td>Photoresist</td>
<td>Acetone</td>
<td>&gt;4000</td>
<td>O₂</td>
<td>35-3500</td>
</tr>
<tr>
<td>Gold</td>
<td>KI</td>
<td>40</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Issues in Surface Micromachining

* Stiction: sticking of released devices to the substrate or to other on-chip structures
  - Difficult to tell if a structure is stuck to substrate by just looking through a microscope
* Residual Stress in Thin Films
  - Causes bending or warping of microstructures
  - Limits the sizes (and sometimes geometries) of structures
* Topography
  - Stringers can limit the number of structural levels
Microstructure Stiction

- **Stiction**: the unintended sticking of MEMS surfaces
- **Release stiction**:
  - Occurs during drying after a wet release etch
  - Capillary forces of droplets pull surfaces into contact
  - Very strong sticking forces, e.g., like two microscope slides w/ a droplet between
- **In-use stiction**: when device surfaces adhere during use due to:
  - Capillary condensation
  - Electrostatic forces
  - Hydrogen bonding
  - Van der Waals forces

Diagram:
- Stiff Beam
- Rinse Liquid
- Wide Beam
- Anchor
- Substrate
- Beam
- Stiction
Hydrophilic Versus Hydrophobic

- **Hydrophilic**: 
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle $\theta_{water} < 90^\circ$

- **Hydrophobic**: 
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle $\theta_{water} > 90^\circ$

Microstructure Stiction

- Thin liquid layer between two solid plates $\Rightarrow$ adhesive
- If the contact angle between liquid and solid $\theta_c < 90^\circ$
  - Pressure inside the liquid is lower than outside
  - Net attractive force between the plates
- The pressure difference (i.e., force) is given by the Laplace equation
**Microstructure Stiction Modeling**

- Wetted Area
- Microstructures
- Contact Angle
- Force Applied to Maintain Equilibrium
- Liquid Layer Thickness
- Laplace Equation: $F = -\Delta P_{La} A = \frac{2\pi \Sigma_{La} \cos \Theta_c}{g}$
  - Surface Tension @ liquid-air interface
  - Pressure Difference @ liquid-air interface
  - Radius of curvature of the meniscus ($\sim$ if concave)

**Avoiding Stiction**

* Reduce droplet area via mechanical design approaches

- Standoff Bumps
- Meniscus-Shaping Features

* Avoid liquid-vapor meniscus formation
  - Use solvents that sublimate
  - Use vapor-phase sacrificial layer etch

* Modify surfaces to change the meniscus shape from concave (small contact angle) to convex (large contact angle)
  - Use teflon-like films
  - Use hydrophobic self-assembled monolayers (SAMs)
Supercritical CO₂ Drying

* A method for stictionless drying of released microstructures by immersing them in CO₂ at its supercritical point
* Basic Strategy: Eliminate surface tension-derived sticking by avoiding a liquid-vapor meniscus
* Procedure:
  - Etch oxide in solution of HF
  - Rinse thoroughly in DI water, but do not dry
  - Transfer the wafer from water to methanol
  - Displace methanol with liquid CO₂
  - Apply heat & pressure to take the CO₂ past its critical point
  - Vent to lower pressure and allow the supercritical CO₂ to revert to gas → liquid-to-gas Xsition
  - In supercritical region means no capillary forces to cause stiction

Hydrophilic Versus Hydrophobic

* Hydrophilic:
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle \( \theta_{\text{water}} < 90^\circ \)
* Hydrophobic:
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle \( \theta_{\text{water}} > 90^\circ \)
Tailoring Contact Angle Via SAM’s

- Can reduce stiction by tailoring surfaces so that they induce a water contact angle > 90°

Self-Assembled Monolayers (SAM’s):
- Monolayers of “stringy” molecules covalently bonded to the surface that then raise the contact angle
- Beneficial characteristics:
  - Conformal, ultrathin
  - Low surface energy
  - Covalent bonding makes them wear resistant
  - Thermally stable (to a point)

<table>
<thead>
<tr>
<th></th>
<th>$\theta_{\text{water}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODT SAM</td>
<td>112 ± 0.7°</td>
</tr>
<tr>
<td>$\text{SiO}_2$</td>
<td>&lt;10°</td>
</tr>
</tbody>
</table>

Dry Release

- Another way to avoid stiction is to use a dry sacrificial layer etch
- For an oxide sacrificial layer
  - Use HF vapor phase etching
  - Additional advantage: gas can more easily get into tiny gaps
  - Issue: not always completely dry → moisture can still condense → stiction → soln: add alcohol
- For a polymer sacrificial layer
  - Use an $O_2$ plasma etch (isotropic, so it can undercut well)
  - Issues:
    - Cannot be used when structural material requires high temperature for deposition
    - If all the polymer is not removed, polymer under the suspended structure can still promote stiction

Released via vapor phase HF
[Kenny, et al., Stanford]

[Kobayashi]
Residual Stress

Residual Stress in Thin Films

• After release, poorly designed microstructures might buckle, bend, or warp → often caused by residual film stress

• Origins of residual stress, $\sigma$
  - Growth processes
    - Non-equilibrium deposition
    - Grain morphology change
    - Gas entrapment
    - Doping
  - Thermal stresses
    - Thermal expansion
    - mismatch of materials → introduce stress during cool-down after deposition
    - Annealing

[Cu Top Electrode
bending
Lateral Spring
GSG Pads
Cu Bottom GND

Tunable Dielectric Capacitor
[Yoon, et al., U. Michigan]

Buckled
Double-Ended
Tuning Fork

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**Need to Control Film Stress**

- Resonance frequency expression for a lateral resonator:

\[ f_0 \approx \frac{1}{2\pi} \sqrt{\frac{4E_y W^3}{ML^3} + \frac{24\sigma_r W}{5ML}} \]

- Since \( W \ll L \), the stress term will dominate if \( \sigma_r \approx E_y \)

**Tensile Versus Compressive Stress**

- **Under tensile stress**, a film wants to shrink w/r to its substrate:
  - Caused, e.g., by differences in film vs. substrate thermal expansion coefficients
  - If suspended above a substrate and anchored to it at two points, the film will be "stretched" by the substrate

- **Under compressive stress**, a film wants to expand w/r to its substrate:
  - If suspended above a substrate and anchored to it at two points, the film will buckle over the substrate
Vertical Stress Gradients

- Variation of residual stress in the direction of film growth
- Can warp released structures in z-direction

Stress in Polysilicon Films

- Stress depends on crystal structure, which in turn depends upon the deposition temperature
- Temperature $\leq 600^\circ$C
  - Films are initially amorphous, then crystallize
  - Get equiaxed crystals, largely isotropic
  - Crystals have higher density $\rightarrow$ tensile stress
  - Small stress gradient
- Temperature $\geq 600^\circ$C
  - Columnar crystals grow during deposition
  - As crystals grow vertically and in-plane they push on neighbors $\rightarrow$ compressive stress
  - Positive stress gradient
### Annealing Out Polysilicon Stress

- Control polySi stress by annealing at high temperatures
  - Typical anneal temperatures: 900-1150°C
  - Grain boundaries move, relax
  - Can dope while annealing by sandwiching the polysilicon between similarly doped oxides (symmetric dopant drive-in), e.g. using 10-15 wt. % PSG

- Rapid thermal anneal (RTA) also effective (surprisingly)

### Topography Issues

- Degradation of lithographic resolution
  - PR step coverage, streaking
  - Thickness differences pose problems for reduction steppers

- Stringers
  - Problematic when using anisotropic etching, e.g., RIE
Nickel Surface-Micromachining Process Flow

Electroplating: Metal MEMS

- Use electroplating to obtain metal \( \mu \)structures
- When thick: call it “LIGA”
- Pros: fast low temp deposition, very conductive
- Cons: drift, low mech. \( Q \) but may be solvable?
Nickel Metal Surface-Micromachining

**Deposit isolation LTO:**
- Target = 2µm
- 1 hr., 40 min. LPCVD @450°C
**Densify the LTO**
- Anneal @950°C for 30 min.

**Define metal interconnect via lift-off**
- Spin photoresist and pattern lithographically to open areas where interconnect will stay
- Evaporate a Ti/Au layer
  - Target = 30nm Ti
  - Target = 270nm Au
- Remove photoresist in PRS2000

**Evaporate Al to serve as a sacrificial layer**
- Target = 1µm

**Lithography to define anchor openings**

**Wet etch the aluminum to form anchor vias**
- Use solution of \( \text{H}_3\text{PO}_4/\text{HNO}_3/\text{H}_2\text{O} \)

**Remove photoresist in PRS2000**

**Electroplate nickel to fill the anchor vias**
- Use solution of nickel sulfamate @ 50°C
- Time the electroplating to planarize the surface
Nickel Metal Surface-Micromachining

- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm²

Nickel Metal Surface-Micromachining

- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant
- Release the structures
  - Use a $\text{K}_4\text{Fe(CN)}_6/\text{NaOH}$ etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au
Nickel Surface-Micromachining Example

*Below: Surface-micromachined in nickel using the described process flow*

3D “Pop-up” MEMS
Pop-Up MEMS

First MEMS hinge
[K. Pister, et al., 1992]

Corner Cube Reflector
[v. Hsu, 1999]

* Pictured: hinged Campanile made in SUMMiT process, assembled using probes [Elliot Hui, et al.]
3D Direct-Assembled Tunable L

[Ming Wu, UCLA]

Hinge Process Flow

- Deposit first sacrificial
- Deposit and pattern first poly

- Deposit and pattern second sacrificial

- Pattern contacts
- Deposit and pattern second poly

- Etch sacrificial
- Assemble part
“Foundry” MEMS: The MUMPS Process

MUMPS: MultiUser MEMS ProcessS

- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and “foundry” services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm² dies

Micromotor fabricated via MUMPS
MUMPS: MultiUser MEMS ProcessS

Micromotor Example

<table>
<thead>
<tr>
<th>Material Layer</th>
<th>Thickness (µm)</th>
<th>Lithography Level Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nitride</td>
<td>0.6</td>
<td>--</td>
</tr>
<tr>
<td>Poly 0</td>
<td>0.5</td>
<td>POLY0 (HOLE0)</td>
</tr>
<tr>
<td>First Oxide</td>
<td>2.0</td>
<td>DIMPLE ANCHOR1</td>
</tr>
<tr>
<td>Poly 1</td>
<td>2.0</td>
<td>POLY1 (HOLE1)</td>
</tr>
<tr>
<td>Second Oxide</td>
<td>0.75</td>
<td>POLY1_POLY2_VIA ANCHOR2</td>
</tr>
<tr>
<td>Poly 2</td>
<td>1.5</td>
<td>POLY2 (HOLE2)</td>
</tr>
<tr>
<td>Metal</td>
<td>0.5</td>
<td>METAL (HOLEM)</td>
</tr>
</tbody>
</table>

Masks in polyMUMPS

Minimum set of masks that must be used in MUMPS

<table>
<thead>
<tr>
<th>Mnemonic level name</th>
<th>Field Type</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0</td>
<td>light</td>
<td>pattern ground plane</td>
</tr>
<tr>
<td>ANCHOR1</td>
<td>dark</td>
<td>open holes for Poly 1 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>DIMPLE</td>
<td>dark</td>
<td>create dimples/bushings for Poly 1</td>
</tr>
<tr>
<td>POLY1</td>
<td>light</td>
<td>pattern Poly 1</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>dark</td>
<td>open holes for Poly 1 to Poly 2 connection</td>
</tr>
<tr>
<td>ANCHOR2</td>
<td>dark</td>
<td>open holes for Poly 2 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>POLY2</td>
<td>light</td>
<td>pattern Poly 2</td>
</tr>
<tr>
<td>METAL</td>
<td>light</td>
<td>pattern Metal</td>
</tr>
<tr>
<td>HOLE0</td>
<td>dark</td>
<td>provide holes for POLY0</td>
</tr>
<tr>
<td>HOLE1</td>
<td>dark</td>
<td>provide release holes for POLY1</td>
</tr>
<tr>
<td>HOLE2</td>
<td>dark</td>
<td>provide release holes for POLY2</td>
</tr>
<tr>
<td>HOLEM</td>
<td>dark</td>
<td>provide release holes in METAL</td>
</tr>
</tbody>
</table>

Extra masks for more flexibility & ease of release

- Field type:
  - Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
  - Dark field (df): in layout, boxes represent holes to be cut out
MUMPS Process Flow

- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 μm of PSG as the 1st sacrificial layer
- Lithography using the Dimple(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1 (df) mask (align to poly0)
- RIE anchor vias down to the nitride surface

MUMPS Process Flow (cont.)

- LPCVD 2 μm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  - This both dopes the polysilicon and reduces its residual stress

- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then ...
- RIE the polysilicon

- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA (df) mask to define contacts to the poly1 layer (align to poly1)
MUMPS Process Flow (cont.)

- Recast with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings

- LPCVD 1.5 \(\mu\text{m}\) undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress

- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask

MUMPS Process Flow (cont.)

- Lithography using the METAL (df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer

- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed
MUMPS: MultiUser MEMS ProcessS

- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and “foundry” services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm² dies

Micromotor fabricated via MUMPS

polyMUMPS Minimum Feature Constraints

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

<table>
<thead>
<tr>
<th></th>
<th>Nominal [μm]</th>
<th>Min Feature [μm]</th>
<th>Min Spacing [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0, POLY1, POLY2</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>ANCHOR1, ANCHOR2</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>DIMPLE</td>
<td>3</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>METAL</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>HOLE1, HOLE2</td>
<td>4</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>HOLEM</td>
<td>5</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>
### MUMPS Design Rules (cont.)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Rule Letter</th>
<th>Figure #</th>
<th>Min. Value (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0 space to ANCHOR1</td>
<td>A</td>
<td>2.5</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose ANCHOR1</td>
<td>B</td>
<td>2.5</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose POLY1</td>
<td>C</td>
<td>2.6</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose POLY2</td>
<td>D</td>
<td>2.7</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY0 enclose ANCHOR2</td>
<td>E</td>
<td>2.8</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY0 space to ANCHOR2</td>
<td>F</td>
<td>2.8</td>
<td>5.0</td>
</tr>
</tbody>
</table>

**Cross Sections**

**Mask Levels**

---

### MUMPS Design Rules (cont.)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Min. Value (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY1 enclose ANCHOR1</td>
<td>G 4.0</td>
</tr>
<tr>
<td>POLY1 enclose DIMPLE</td>
<td>H 4.0</td>
</tr>
<tr>
<td>POLY1 enclose POLY1 POLY2 VIA</td>
<td>I 4.0</td>
</tr>
<tr>
<td>POLY1 enclose POLY2</td>
<td>J 4.0</td>
</tr>
<tr>
<td>POLY1 space to ANCHOR2</td>
<td>K 3.0</td>
</tr>
</tbody>
</table>

*Note: Lateral etch holes in POLY1 ≤ 30 (max. value)*

**Cross Sections**

**Mask Levels**
### MUMPS Design Rules (cont.)

#### Rule #1: POLY0 Space to ANCHOR1
- **Rule Letter:** A
- **Figure #:** 2.5
- **Min. Value (μm):** 4.0

#### Rule #2: POLY0 Enclose ANCHOR1
- **Rule Letter:** B
- **Figure #:** 2.5
- **Min. Value (μm):** 4.0

#### Rule #3: POLY0 Enclose POLY1
- **Rule Letter:** C
- **Figure #:** 2.6
- **Min. Value (μm):** 4.0

#### Rule #4: POLY0 Enclose POLY2
- **Rule Letter:** D
- **Figure #:** 2.7
- **Min. Value (μm):** 5.0

#### Rule #5: POLY0 Enclose ANCHOR2
- **Rule Letter:** E
- **Figure #:** 2.8
- **Min. Value (μm):** 5.0

#### Rule #6: POLY0 Space to ANCHOR2
- **Rule Letter:** F
- **Figure #:** 2.8
- **Min. Value (μm):** 5.0

#### Rule #7: POLY1 Enclose ANCHOR1
- **Rule Letter:** G
- **Figure #:** 2.6
- **Min. Value (μm):** 4.0

#### Rule #8: POLY1 Enclose DIMPLE
- **Rule Letter:** H
- **Figure #:** 2.13
- **Min. Value (μm):** 4.0

#### Rule #9: POLY1 Enclose POLY1_POLY2_VIA
- **Rule Letter:** I
- **Figure #:** 2.11
- **Min. Value (μm):** 4.0

#### Rule #10: POLY1 Enclose POLY2
- **Rule Letter:** J
- **Figure #:** 2.14
- **Min. Value (μm):** 4.0

#### Rule #11: POLY1 Space to ANCHOR2
- **Rule Letter:** K
- **Figure #:** 2.11
- **Min. Value (μm):** 3.0

#### Rule #12: Lateral etch hole space in POLY1
- **Rule Letter:** R
- **Figure #:** 2.15
- **Min. Value (μm):** ≤30 (max. value)

#### Rule #13: POLY2 Enclose ANCHOR2
- **Rule Letter:** S
- **Figure #:** 2.15
- **Min. Value (μm):** 5.0

#### Rule #14: POLY2 Enclose POLY1_POLY2_VIA
- **Rule Letter:** T
- **Figure #:** 2.14
- **Min. Value (μm):** 4.0

#### Rule #15: POLY2 Enclose METAL
- **Rule Letter:** U
- **Figure #:** 2.14
- **Min. Value (μm):** 4.0

#### Rule #16: POLY2 Space to POLY1
- **Rule Letter:** V
- **Figure #:** 2.14
- **Min. Value (μm):** 5.0

#### Rule #17: HOLE2 Enclose HOLE1
- **Rule Letter:** W
- **Figure #:** 2.14
- **Min. Value (μm):** 2.0

#### Rule #18: Lateral etch hole space in POLY2
- **Rule Letter:** X
- **Figure #:** 2.15
- **Min. Value (μm):** ≤30 (max. value)

---

### TABLE 2.7: PolyMUMPs design rule reference sheet. Table shows minimum dimensions (μm), rule name, and figure number, respectively.

<table>
<thead>
<tr>
<th>Level 1</th>
<th>Level 2</th>
<th>Min. Feature</th>
<th>Min. Spacing</th>
<th>Enclose</th>
<th>Spacing</th>
<th>Cut-In</th>
<th>Cut-Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ANCHOR1</td>
<td>-</td>
<td>2</td>
<td>2</td>
<td>4/B/2.5</td>
<td>4/A/2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POLY1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ANCHOR2</td>
<td>-</td>
<td>2</td>
<td>2 / 2.5&quot;</td>
<td>5/E/2.8</td>
<td>5/F/2.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POLY2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| POLY1   |         |              |              |         |         |        |         |
| POLY2   |         |              |              |         |         |        |         |
| DIMPLE  |         |              |              | 4/N/2.13 |         |        |         |
| POLY1_POLY2_VIA | | 2            | 2 / 2.5"     | 4/H/2.9 |         |        |         |

| POLY2   |         |              |              | 3/M/2.5 | 3/N/2.10 | 5/P/2.14 | 4/Q/2.14 |
| HOLEM   |         |              |              |         | 3/M/2.5 | 5/P/2.14 | 4/Q/2.14 |
| HOLE2   |         |              |              | 3/N/2.10 | 5/P/2.14 | 4/Q/2.14 |         |
| HOLE1   |         |              |              | 3/M/2.5 | 5/P/2.14 | 4/Q/2.14 |         |

---

**Notes:**
- **Level 1** and **Level 2** columns indicate the hierarchy of layers in the MEMS design.
- **Min. Feature** and **Min. Spacing** columns specify the minimum dimensions allowed.
- **Enclose** and **Spacing** columns describe the minimum required spacings.
- **Cut-In** and **Cut-Out** columns provide the minimum required cut-in and cut-out dimensions.
The Sandia SUMMIT Process

Sandia’s SUMMiT V

• SUMMiT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process
  - Five-layer polysilicon surface micromachining process
  - One electrical interconnect layer & 4 mechanical layers
  - Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  - 14 masks
**SUMMiT V Layer Stack**

- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized.

**Chemical Mechanical Polishing (CMP)**

- Used to planarize the top surface of a semiconductor wafer or other substrate.
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad.
  - Wafer and pad are pressed together.
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing.
**CMP: Not the Same as Lapping**

- **Lapping**
  - Lapping is merely the removal of material to flatten a surface without selectivity.
  - Everything is removed at approximately the same rate.

- **Chemical Mechanical Polishing (CMP)**
  - CMP is selective to certain films, and not selective to others.
  - Stops at a non-selective layer.

---

**Actual SUMMiT Cross-Section**

- No CMP until after the first three polySi layers.
- 1 μm mmpoly1 and 1.5 μm mmpoly2 can be combined to form a 2.5 μm polysilicon film.
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions.