PROBLEM SET #2

Issued: Thursday, February 7, 2019

Due: Thursday, February 21, 2019 at 9:00 a.m. on Gradescope.

1. Consider the cross-section shown in Fig. PS2.1-1 of a polydiamond beam with angled sidewalls upon which a conformal SiO_2 film was deposited. The wafer will be placed into an RIE chamber. Assume that chemicals inside the chamber will etch the structure at the rates listed in Table PS2.1-1. Carefully draw cross-sections of the structure after

(a) 10 minutes of etching

(b) 60 minutes of etching

Note that it is only necessary to draw half of the structure due to symmetry. Please specify all angles and dimensions for each cross-section. Round all dimensions to the nearest 10nm.

MATERIAL	VERTICAL	LATERAL	UNIT
SiO_2	50	10	nm/min
Polydiamond	10	0	nm/min
Si_3N_4	30	0	nm/min
Si	100	0	nm/min

Table PS2.1-1

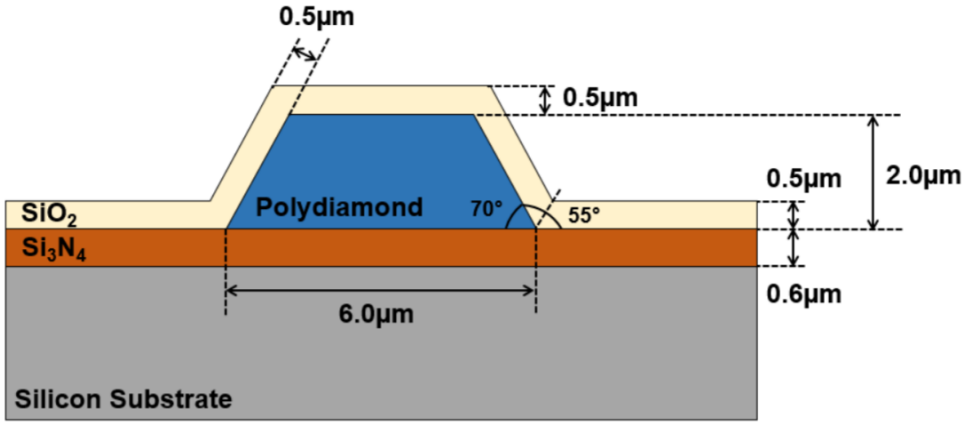

Fig. PS2.1-1

2. You are given the layout below along with the process traveler to follow. In the layout each box corresponds to 1μm^2. In the mask legend, cf = "clear field" and df = "dark field". In the process traveler, assume that all lithography steps use positive photoresist, except when otherwise indicated, and that all etch steps are 100% selective to intended film. Also, assume that RIE etches are anisotropic, but any other type of etch has some degree of isotropy. Follow the instructions after the process traveler.

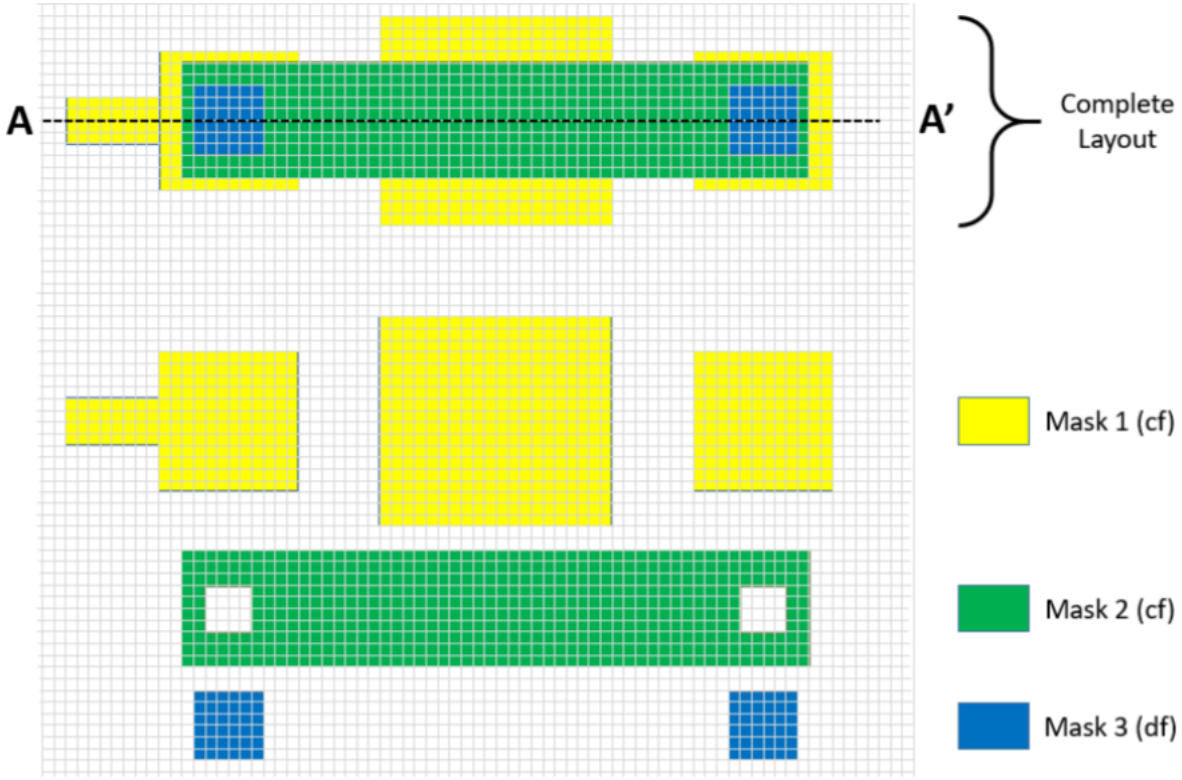

Fig PS2.2-1

Process Traveler:

(i) Deposit 1.5μm of LTO via LPCVD.

(ii) Deposit 300nm of silicon rich nitride via LPCVD

(iii) Deposit 300nm of in situ-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.

(iv) Lithography via Mask 1.

(v) Etch polysilicon via RIE and stop on nitride.

(vi) Remove photoresist.

(vii) Deposit 500nm of LTO via LPCVD.

(viii) Deposit 1μm of in situ-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.

(ix) Deposit 1μm of LTO via LPCVD.

(x) Lithography via Mask 2.

(xi) Etch oxide via RIE and stop on polysilicon.

(xii) Etch polysilicon via RIE and stop on oxide.

(xiii) Remove photoresist.

(xiv) Lithography via Mask 3.

(xv) Etch oxide via RIE and stop when the etch reaches polysilicon or nitride on the substrate.

(xvi) Remove photoresist.

(xvii) Deposit 2μm of in situ-phosphorus-doped polycrystalline silicon via LPCVD at 610°C.

(xviii) CMP the polysilicon and stop on oxide.

(xix) Lithography via Mask 3 using a negative resist.

(xx) Etch polysilicon via RIE and stop on oxide.

(xxi) Remove photoresist.

(xxii) Dip in HF until structures are fully released.

Instructions:

(a) Draw the cross-section through step (xiii) along the AA' axis.

(b) Draw the final cross-section along the AA' axis.

3. Figure PS2.2-1 presents a 2μm-thick polysilicon film atop a 2μm-thick sacrificial oxide film. The polysilicon beam is initially uniformly doped with phosphorous to a concentration $N_D = 1 \times 10^{15}$ cm^{-3}. Suppose you want to make the beam more conductive by diffusing boron atoms into the n-type polysilicon material. To do so, you first place the wafer into a predeposition furnace alongside solid-source boron wafers for 40 min at 1000°C. You then drive in the dopants (with no boron source) for 50 min at the same temperature.

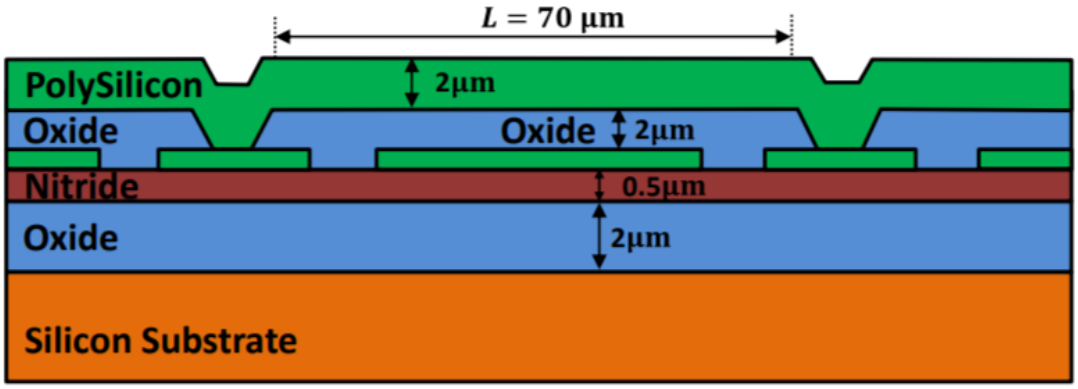

Fig PS2.2-1

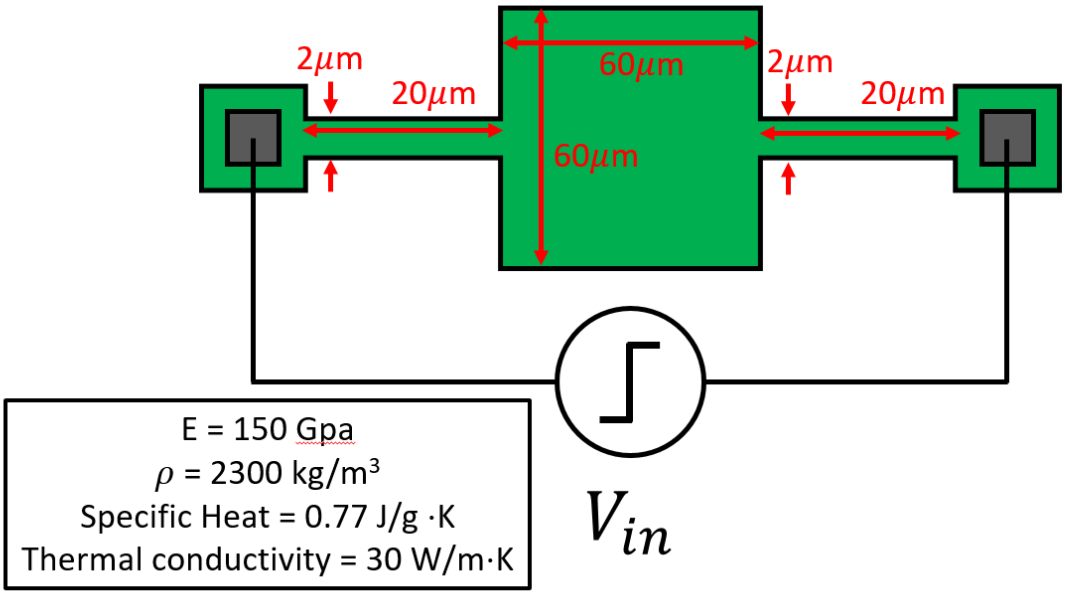

Fig PS2.2-2

Assume for this problem that the diffusion coefficient D_0 of poly-silicon is 10 times larger than that of single crystal silicon (SCS). Page 37 of module 4 has a table of diffusion coefficients for different impurities in SCS.

(a) Derive an expression for the distribution of boron atoms after the pre-deposition step. What is the total number of dopant atoms per unit area?

(b) Derive an expression for the distribution of boron atoms after the drive-in step. As discussed in lecture, you can assume the pre-deposition step equates to a thin layer of highly doped silicon at the surface of the wafer and then use the total number of dopant atoms per unit area to find the Gaussian function.

(c) The depth at which the concentration of diffused dopant atoms is the same as the background concentration is defined to be the junction depth. What is the junction depth at the end of the process?

(d) Suppose the above drive-in process is not the only high-temperature step in your process, but entails the following subsequent steps:

1. An LTO deposition at a temperature of 400°C over a time period of 150 min.
2. Polysilicon deposition at a temperature of 600°C over a time period of 90 min.
3. A rapid thermal anneal at temperature of 1050°C over a time period of 2 min.

    i. Rank the four thermal steps from the greatest effect on the boron diffusion profile to the least.

    ii. What is the new doping depth after these additional three steps?

(e) Using the doping depth you get from (c), what is the sheet resistance of the doped polysilicon layer? Remember that the dopant concentration is a function of depth, so use the distribution function derived in (b) to find the exact sheet resistance. Assume the hole mobility in polysilicon is constant at 450 cm^2/V at room temperature and the pn-junction depletion width is negligible in comparison to junction depth.

(f) Suppose we use the layout as shown in Figure PS2.2-2 to pattern the polysilicon film to generate a MEMS accelerometer. If we apply a 300 mV voltage across the two anchors, what is the steady state temperature of the proof mass? Assume the temperature of the silicon substrate and the anchors of the structure is constant at 25°C.