

Anisotropic Wet Etching

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Anisotropic etches are available for single crystal Si:

- Orientation-dependent etching: $\langle 111 \rangle$ -plane more densely packed than $\langle 100 \rangle$ -plane

Faster E.R. Slower E.R.

...in some solvents

One such solvent: KOH + isopropyl alcohol
(e.g., 23.4 wt% KOH, 13.3 wt% isopropyl alcohol, 63 wt% H₂O)

⇒ E.R. _{$\langle 100 \rangle$} = 100 × E.R. _{$\langle 111 \rangle$}

Anisotropic Etching of Silicon

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- Etching of Si w/ KOH

$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$

$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$
- Crystal orientation dependent etch rates
 - {110}:{100}:{111}=600:400:1
 - {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
 - {111} plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
 - {111} forms protective oxide
 - {111} smoother than other crystal planes → good for optical MEMS (mirrors)

Self-limiting etches

Membrane

Front side mask

Back side mask

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Anisotropic Wet Etching (cont.)

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Can get the following:

(on a $\langle 100 \rangle$ - wafer)

(on a $\langle 110 \rangle$ - wafer)

⇒ Quite anisotropic!

Anisotropic Wet Etching of Silicon

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- Deposit nitride:
 - Target = 100nm
 - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
 - RIE using SF₆
 - Remove PR in PRS2000
- Etch the silicon
 - Use 1:2 KOH:H₂O (wt.), stirred bath @ 80°C
 - Etch Rates:
 - (100) Si → 1.4 μm/min
 - Si₃N₄ → ~ 0 nm/min
 - SiO₂ → 1-10 nm/min
 - Photoresist, Al → fast
- Micromasking by H₂ bubbles leads to roughness
 - Stir well to displace bubbles
 - Can also use oxidizer for (111) surfaces
 - Or surfactant additives to suppress bubble formation

Bubble → bad news!

Solubility

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Silicon Wafers

{100} type wafer

[Maluf]

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Silicon Crystallography

Miller Indices (h k l):

- Planes**
 - Reciprocal of plane intercepts with axes
 - e.g., for (110), intercepts: (x,y,z) = (1,1,∞); reciprocals: (1,1,0) → (110)
 - (unique), {family}
- Directions**
 - One endpoint of vector @ origin
 - {unique}, <family>

{111}

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Determining Angles Between Planes

The angle between vectors [abc] and [xyz] is given by:

$$ax + by + cz = |(a, b, c)| \cdot |(x, y, z)| \cdot \cos \theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1} \left[\frac{ax + by + cz}{|(a, b, c)| \cdot |(x, y, z)|} \right]$$

- For {100} and {110} → 45°
- For {100} and {111} → 54.74°
- For {110} and {111} → 35.26°, 90°, and 144.74°

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Silicon Crystal Origami

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions

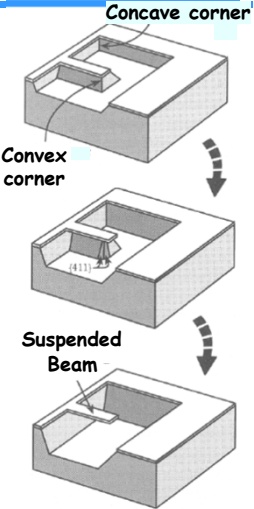
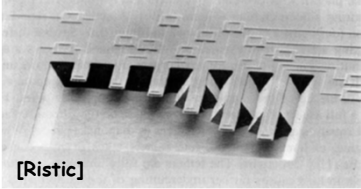
[Judy, UCLA]

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Undercutting Via Anisotropic Si Etching

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- Concave corners bounded by {111} are not attacked
- ... but convex corners bounded by {111} are attacked
 - ↳ Two {111} planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
 - ↳ Result: can undercut regions around convex corners

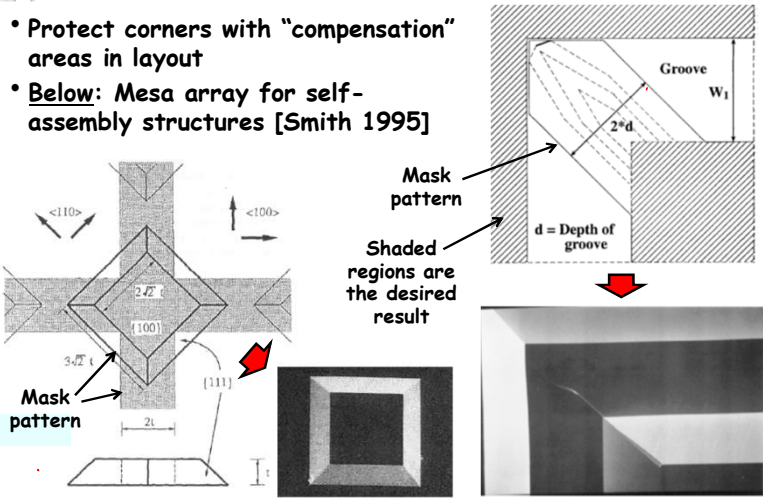
[Ristic]

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Corner Compensation

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- Protect corners with "compensation" areas in layout
- Below: Mesa array for self-assembly structures [Smith 1995]



Mask pattern

Mask pattern

Shaded regions are the desired result

Groove W_1

2^*d

$d = \text{Depth of groove}$

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Other Anisotropic Silicon Etchants

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- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
 - ↳ Etch rate (100) = 0.5-1.5 $\mu\text{m}/\text{min}$
 - ↳ Attacks Al
 - ↳ Si-doped Al safe & IC compatible
 - ↳ Etch ratio (100)/(111) = 10-35
 - ↳ Etch masks: SiO_2 , $\text{Si}_3\text{N}_4 \sim 0.05\text{-}0.25 \text{ nm}/\text{min}$
 - ↳ Boron doped etch stop, up to 40x slower
- EDP (115°C)
 - ↳ Carcinogenic, corrosive
 - ↳ Etch rate (100) = 0.75 $\mu\text{m}/\text{min}$
 - ↳ Al may be etched
 - ↳ $R(100) > R(110) > R(111)$
 - ↳ Etch ratio (100)/(111) = 35
 - ↳ Etch masks: $\text{SiO}_2 \sim 0.2 \text{ nm}/\text{min}$, $\text{Si}_3\text{N}_4 \sim 0.1 \text{ nm}/\text{min}$
 - ↳ Boron doped etch stop, 50x slower

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Boron-Doped Etch Stop

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Boron-Doped Etch Stop

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- Control etch depth precisely with boron doping (p++)
 - [B] > 10²⁰ cm⁻³ reduces KOH etch rate by 20-100x
 - Can use gaseous or solid boron diffusion
 - Recall etch chemistry:

$$\text{Si} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2^{2-} + 4\text{e}^-$$
~~$$4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2$$~~
 - At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH⁻
- Result:**
 - Beams, suspended films
 - 1-20 μm layers possible

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Ex: Micronozzle

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- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

1. Pattern mask 2. Etch circle in p++
3. Mask front side 4. Anisotropic etch

[Maluf]

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Ex: Microneedle

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- Below: micro-neurostimulator**
 - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan

Sharp Probe Tip

Multi-Channel Recording Array Structure

- Selectively diffuse p++ into substrate
- Deposit interconnect pattern and insulate conductors
- Pattern dielectric and metallize recording sites
- Dissolve away the wafer (no mask needed)

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Ex: Microneedles (cont.)

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64-Site Multiplexed Stimulating Array

Probe Shanks With Four Sites per Shank

[Wise, U. of Michigan]

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400 μm site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

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Electrochemical Etch Stop

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Electrochemical Etch Stop

- When silicon is biased with a sufficiently large anodic potential relative to the etchant → get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented → no oxide growth, and etching can proceed
 - Can prevent current flow by adding a reverse-biased diode structure

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Electrochemical Etch Stop

- Electrochemical etch stop**
 - n-type epitaxial layer grown on p-type wafer forms p-n junction diode
 - $V_p > V_n$ → electrical conduction (current flow)
 - $V_p < V_n$ → reverse bias current (very little current flow)
- Passivation potential:** potential at which thin SiO_2 film forms
 - different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- Setup:**
 - p-n diode in reverse bias
 - p-substrate floating → etched
 - n-layer above passivation potential → not etched

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Electrochemical Etching of CMOS

- N-type Si well with circuits suspended f/ SiO_2 support beam
- Thermally and electrically isolated
- If use TMAH etchant, doped (w/Si) Al bond pads safe

[Reay, et al. (1994)]
[Kovacs Group, Stanford]

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Ex: Bulk Micromachined Pressure Sensors

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- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection $< 1 \mu\text{m}$

[Maluf]

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Ex: Pressure Sensors

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- Below: catheter tip pressure sensor [Lucas NovaSensor]
↳ Only $150 \times 400 \times 900 \mu\text{m}^3$

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Deep Reactive-Ion Etching (DRIE)

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The Bosch process:

- Inductively-coupled plasma
- Etch Rate: $1.5\text{--}4 \mu\text{m}/\text{min}$
- Two main cycles in the etch:
 - ↳ Etch cycle (5–15 s): SF_6 (SF_x^+) etches Si
 - ↳ Deposition cycle (5–15 s): C_4F_8 deposits fluorocarbon protective polymer (CF_2^-)_n
- Etch mask selectivity:
 - ↳ $\text{SiO}_2 \sim 200:1$
 - ↳ Photoresist $\sim 100:1$
- Issue: finite sidewall roughness
↳ scalloping $< 50 \text{ nm}$
- Sidewall angle: $90^\circ \pm 2^\circ$

[Maluf]

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DRIE Issues: Etch Rate Variance

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20 μm

- Etch rate is diffusion-limited and drops for narrow trenches
 - ↳ Adjust mask layout to eliminate large disparities
 - ↳ Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

Etch Rate ($\mu\text{m}/\text{min}$)

Trench Width (μm)

Aspect Ratio

∞ 15 7.5 5.0 3.8 3.0 2.5 2.1 1.9

Etch rate decreases with trench width

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DRIE Issues: "Footing"

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- Etch depth precision
 - Etch stop: buried layer of SiO_2
 - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- Problem:** Lateral undercut at Si/SiO_2 interface \rightarrow "footing"
 - Caused by charge accumulation at the insulator

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Recipe-Based Suppression of "Footing"

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- Use **higher process pressure** to reduce ion charging [Nozawa]
 - High operating pressure \rightarrow concentration of (-) charge increases and can neutralize (+) surface charge
 - Issue:** must introduce as a separate recipe when the etch reaches the Si -insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe** to reduce overetching [Schmidt]
 - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
 - Issue:** Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
 - Low frequency \rightarrow more ions with low directionality and kinetic energy \rightarrow neutralizes (-) potential barrier at trench entrance
 - Allows e^- 's to reach the trench base and neutralize (+) charge \rightarrow maintain charge balance inside the trench

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Metal Interlayer to Prevent "Footing"

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Pre-defined metal interlayer grounded to substrate supplies e^- 's to neutralize (+) charge and prevent charge accumulation at the Si -insulator interface

(a) Photolithography 1 (sacrificial)	(f) Silicon Thinning
(b) Preparatory trenches	(g) Photolithography 2
(c) Metal interlayer deposition	(h) DRIE
(d) Lift-off (remove PR)	(i) Remove metal interlayer
(e) Anodic Bonding	(j) Metallize

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Footing Prevention (cont.)

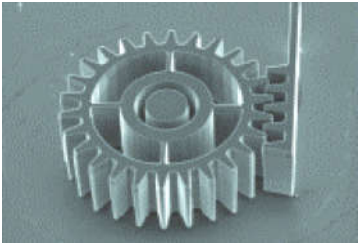
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- Below:** DRIE footing over an oxide stop layer
- Right:** efficacy of the metal interlayer footing prevention approach [Kim, Stanford]

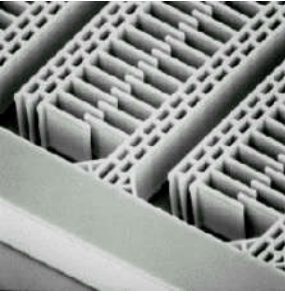
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DRIE Examples

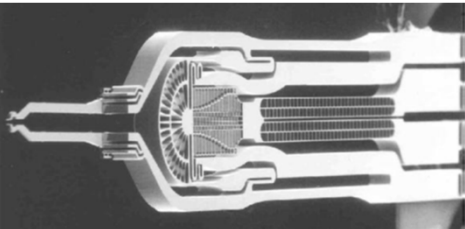
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High aspect-ratio gear



Tunable Capacitor
[Yao, Rockwell]



Microgripper
[Keller, MEMS Precision Instruments]


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Vapor Phase Etching of Silicon

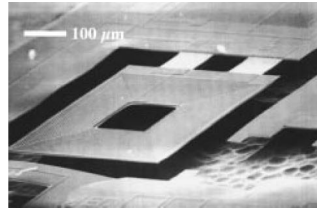
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- Vapor phase Xenon Difluoride (XeF_2)

$$2\text{XeF}_{2(g)} + \text{Si}_{(s)} \rightarrow 2\text{Xe}_{(g)} + \text{SiF}_{4(g)}$$
- Set-up:
 - ↳ Xe sublimates at room T
 - ↳ Closed chamber, 1-4 Torr
 - ↳ Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 $\mu\text{m}/\text{min}$, isotropic
- Etch masks: photoresist, SiO_2 , Si_3N_4 , Al, other metals
- Issues:
 - ↳ Etched surfaces have granular structure, 10 μm roughness
 - ↳ Hazard: XeF_2 reacts with H_2O in air to form Xe and HF



Xactix XeF_2 Etcher



100 μm

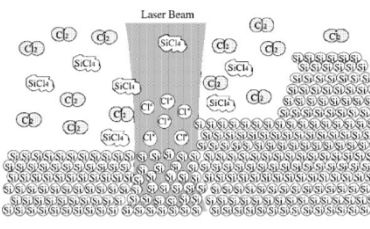
Inductor w/ no substrate [Pister]

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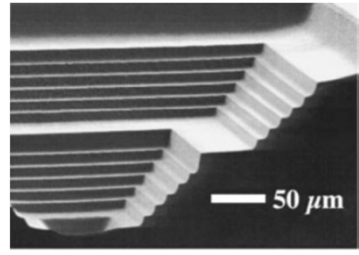
Laser-Assisted Chemical Etching

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- Laser creates Cl radicals from $\text{Cl}_2 \rightarrow$ reaction forms SiCl_2
- Etch rate: 100,000 $\mu\text{m}^3/\text{s}$
 - ↳ Takes 3 min. to etch 500x500x125 μm^3 trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file



Laser Beam



50 μm

- At right:
 - ↳ Laser assisted etching of a 500x500 μm^2 terraced silicon well
 - ↳ Each step is 6 μm -deep

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Wafer Bonding

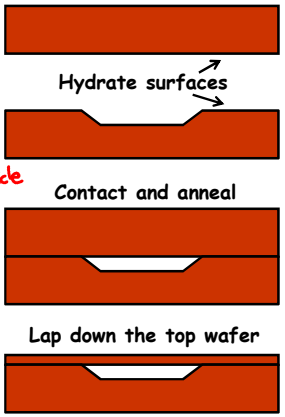
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Fusion Bonding

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- Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces
- Procedure:**
 - Prepare surfaces: must be smooth and particle-free
 - Clean & hydrate: O₂ plasma, hydration, or HF dip
 - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
 - Anneal at 600-1200°C to bring the bond to full strength
- Result:** a bond as strong as the silicon itself!



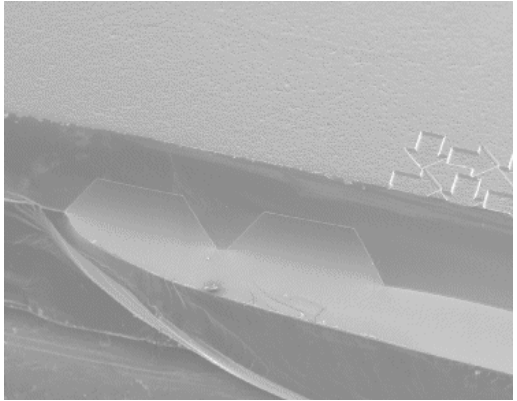
Works for Si-to-Si bonding and Si-to-SiO₂ bonding

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Fusion Bonding Example

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- Below:** capacitive pressure sensor w/ fusion-bonded features



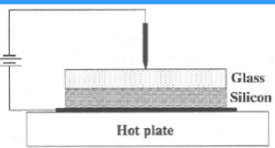
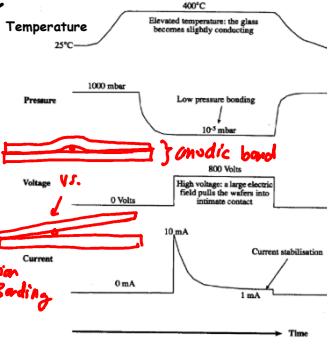
[Univ. of Southampton]

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Anodic Bonding

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- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:**
 - Press Si and glass together
 - Elevate temperature: 180-500°C
 - Apply (+) voltage to Si: 200-1500V
 - (+) voltage repels Na⁺ ions from the glass surface
 - Get net (-) charge at glass surface
 - Attractive force between (+) Si and (-) glass → intimate contact allows fusing at elevated temp.
 - Current drops to zero when bonding is complete

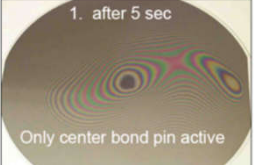
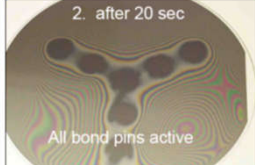
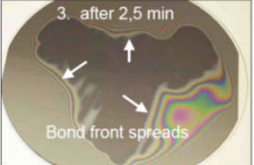
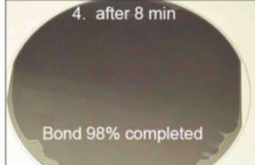



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Anodic Bonding (cont.)

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- Advantage:** high pressure of electrostatic attraction smoothes out defects
- Below:** 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N₂ @ 1000 mbar

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Metal Layer Bonding

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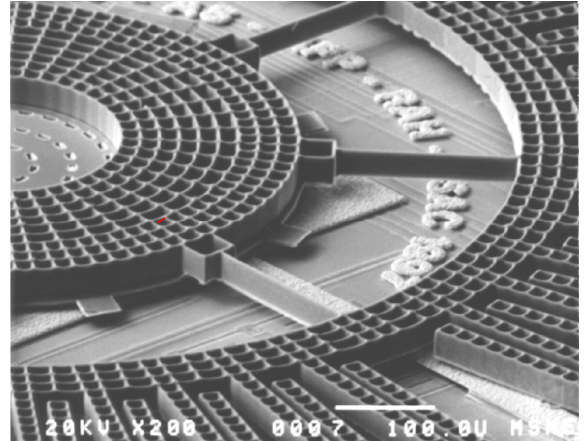
- Pattern seal rings and bond pads photolithographically
- **Eutectic bonding**
 - ↳ Uses eutectic point in metal-Si phase diagrams to form silicides
 - ↳ Au and Si have eutectic point at 363°C
 - ↳ Low temperature process
 - ↳ Can bond slightly rough surfaces
 - ↳ **Issue:** Au contamination of CMOS
- **Solder bonding**
 - ↳ PbSn (183°C), AuSn (280°C)
 - ↳ Lower-T process
 - ↳ Can bond very rough surfaces
 - ↳ **Issue:** outgassing (not good for encapsulation)
- **Thermocompression**
 - ↳ Commonly done with electroplated Au or other soft metals
 - ↳ Room temperature to 300°C
 - ↳ Lowest-T process
 - ↳ Can bond rough surfaces with topography

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Thermocompression Bonding

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- **Below:** Transfer of hexsil actuator onto CMOS wafer

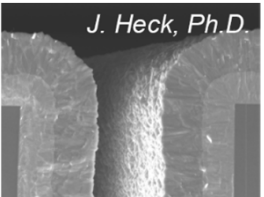
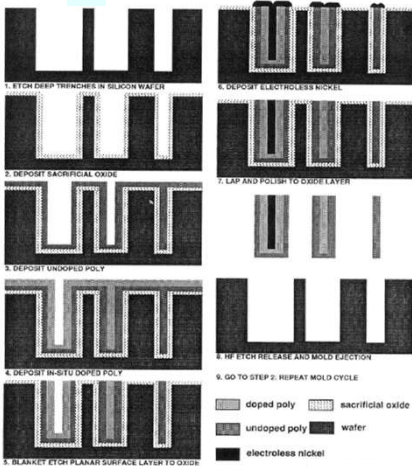


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Hexsil MEMS

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- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength

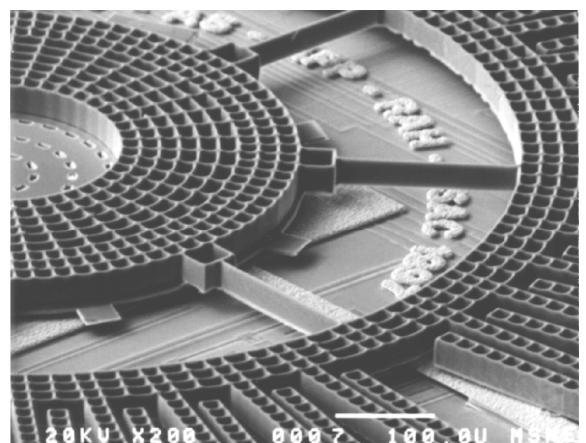



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Hexsil MEMS Actuator

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- **Below:** Transfer of hexsil actuator onto CMOS wafer



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Silicon-on-Insulator (SOI) MEMS

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- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

	Cross Section	Top View
Silicon SiO ₂		
Silicon Nitride		
Integrated Circuitry		
Structure definition and release		

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SOI MEMS Examples

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[Brosnihan]

Micromirror
[Analog Devices]

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The SCREAM Process

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- SCREAM: Single Crystal Reactive Etching and Metallization process**

- Deposit oxide and photoresist
- Lithography and oxide etch
- Silicon etch
- Coat sidewalls with PECVD oxide
- Remove oxide at bottom and etch silicon
- Plasma etch in SF₆ to release structures

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