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Position Sensing Circuits

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Position-to-Voltage Conversion

- To sense position (i.e., displacement), use a capacitive load

Again, have port-to-port I/O symmetry:

Brute force approach:

$$\frac{N_0}{V_i}(s) = \frac{1}{R_x + \frac{1}{sC_x} + sL_x + \frac{1}{sC_D}}$$

$$\frac{N_0}{V_i}(s) = \frac{\frac{sC_x}{sR_x C_x + 1 + s^2 L_x C_x + \frac{sC_x}{sC_D}}{\frac{sC_x}{sR_x C_x + 1 + s^2 L_x C_x + \frac{sC_x}{sC_D}}} = \frac{C_x/C_D}{1 + C_x/C_D} \frac{1}{1 + \frac{sR_x C_x}{1 + C_x/C_D} + s^2 \frac{L_x C_x}{1 + C_x/C_D}}$$

$$= \frac{C_x/C_D}{1 + C_x/C_D} \frac{1 + C_x/C_D}{s^2 + s \left(\frac{R_x}{L_x} \right) + \left(\frac{1 + C_x/C_D}{L_x C_x} \right)}$$

$\omega_0^2 = \frac{1}{L_x C_x} \rightarrow (\omega_0')^2 = \omega_0^2 (1 + C_x/C_D)$
 $Q' = \frac{\omega_0' L_x}{R_x} \rightarrow \frac{R_x}{L_x} = \frac{\omega_0'}{Q'}$, $Q' = Q \sqrt{1 + C_x/C_D}$

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$$\frac{N_0}{V_i}(s) = \frac{C_x/C_D}{1 + C_x/C_D} \frac{(\omega_0')^2}{s^2 + \left(\frac{\omega_0'}{Q'} \right) s + (\omega_0')^2}$$

DC Gain Term Low-Pass Biquad

To maximize gain $\rightarrow 1$, need $C_D \ll C_x$ (must minimize C_D)

Note: Can we similar short-cut to the R case.

- Get DC response $\rightarrow C$'s dominate.
- Then:

$$\frac{N_0}{V_i}(s) = (\text{DC Gain}) \cdot \frac{1}{s} \cdot \text{LP}(s, \omega_0', Q') \cdot \omega_0'^2$$

Voltage Representing Position

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Problems With Pure-C Position Sensing

- To sense position (i.e., displacement), use a capacitive load

Interconnect Bond Pad

$$\frac{N_0}{V_i}(s) = \frac{C_x/C_D}{1 + C_x/C_D} \cdot \frac{1}{s} \cdot \text{LP}(s, \omega_0', Q') \cdot \omega_0'^2$$

Integration yields displacement.

To maximize gain, minimize C_D .

\Rightarrow Problem: parasitic capacitance

$$C_D \rightarrow C_D + C_{p_i} + C_{p_b}$$

\Rightarrow DC Gain: $\frac{C_x / (C_D + C_{p_i} + C_{p_b})}{1 + C_x / (C_D + C_{p_i} + C_{p_b})}$

Output will get smaller.

Remedy: Suppress C_p Via use of op amps.

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The Op Amp Integrator Advantage

• The virtual ground provided by the ideal op amp eliminates the parasitic capacitance C_p

$R_2 \gg \frac{1}{sC_2}$ (for biasing)

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Differential Position Sensing

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Differential Position Sensing

• Example: ADXL-50

Proof Mass

Sense Finger

Tethers with fixed ends

Applied Acceleration

Fixed Electrodes

Suspension Beam in Tension

Issue: Parasitic Capacitance

$$V_0 = -V_p + (2V_p) \frac{C_1}{C_1 + C_2}$$

$$= -\frac{V_p C_1 - V_p C_2 + 2V_p C_1}{C_1 + C_2} = V_p \frac{C_1 - C_2}{C_1 + C_2} = V_0$$

Ar baffles, C_p reducer gain \rightarrow Soln: use op amp!

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Buffer-Bootstrapped Position Sensing

Includes capacitance from interconnects, bond pads, and C_{gs} of the op amp

Unity Gain Buffer

C_{gd} = gate-to-drain capacitance of the input MOS transistor

• Bootstrap the ground lines around the interconnect and bond pads

- No voltage across C_p
- It's effectively not there!

Interconnect Ground Plane

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