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Non-Ideal Operational Amplifiers

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Integrator-Based Diff. Position Sensing

$i_o = i_1 + i_2 = N_p(sC_1) - N_p(sC_2)$
 $= V_p s(C_1 - C_2)$
 $\therefore V_o = -i_o \left(\frac{1}{sC_F} \right) = -N_p \left(\frac{C_1 - C_2}{C_F} \right)$

$\frac{V_o}{V_p} = - \frac{C_1 - C_2}{C_F}$

\Rightarrow A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...
 Can drive next stages R_1 w/o interference to transfer function!

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Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they ...
 - ☞ Generate noise
 - ☞ Have finite gain, A_o
 - ☞ Have finite bandwidth, ω_b
 - ☞ Have finite input resistance, R_i
 - ☞ Have finite input capacitance, C_i
 - ☞ Have finite output resistance, R_o
 - ☞ Have an offset voltage V_{OS} between their (+) and (-) terminals
 - ☞ Have input bias currents
 - ☞ Have an offset I_{OS} between the bias currents into the (+) and (-) terminals
 - ☞ Have finite slew rate
 - ☞ Have finite output swing (governed by the supply voltage used, -L to +L)
- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!

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Finite Op Amp Gain and Bandwidth

- For an ideal op amp: $A = \infty$
- In reality, the gain is given by: $A(s) = \frac{A_o}{1 + \frac{s}{\omega_b}}$
 - A_o ← Finite Gain
 - ω_b ← Finite Bandwidth
- For $\omega \gg \omega_b$:

$$A(s) \approx \frac{A_o}{\left(\frac{s}{\omega_b} \right)} = \frac{A_o \omega_b}{s} = \frac{\omega_T}{s} \rightarrow \text{Integrator w/ time const. } 1/\omega_T$$

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Op Amp Non-Idealities

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Op Amp Non-Idealities → R_i & R_o

Input resistance R_i and Output Resistance R_o :

With finite R_i and R_o , and finite gain and BW, the op amp equivalent circuit becomes:

⇒ Basically reduces down to a voltage-amplifier model
 ⇒ Add an output CO to model a single pole response, where

$$w_b = \frac{1}{R_o C_o}$$

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Input Offset Voltage V_{OS}

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Input Offset Voltage, V_{OS} :

$v_o = A(v_+ - v_-)$

Ideal case: $v_o = 0$
Reality: $v_o \neq 0$ (usually, $v_o = L^+$ or L^- : it rails out!)

Why? Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage V_{OS} .

Typically, $V_{OS} = 1mV - 5mV$

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Effect of V_{OS} on Op Amp Circuits

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Example: Non-Inverting Amplifier

$$V_o = V_{OS} \left(1 + \frac{R_2}{R_1} \right)$$

e.g., $\frac{R_2}{R_1} = 9$, $V_{OS} = 5mV \rightarrow V_o = 50mV$
 (not so bad ...)

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Effect of V_{OS} on Op Amp Circuits (cont.)

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Example: Integrator

To fix this, place a resistor in shunt with the C → then:

$$v_o = V_{OS} \left(1 + \frac{R_f}{R} \right)$$

$$v_o = V_{OS} + \frac{1}{C} \int_0^t i_1 dt$$

$$= V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt$$

$$= V_{OS} \left(1 + \frac{t}{RC} \right) + v_C|_{t=0}$$

Will continue to increase until op amp saturates

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Integrator-Based Diff. Position Sensing

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$+V_P$
 $-V_P$

i_1
 i_2

C_1
 C_2

i_o

$R_2 \gg \frac{1}{sC_2}$ (for biasing)

C_F

$R_0 = 0\Omega$

Can drive next stage's R_1 w/o interference to transfer function!

$i_o = i_1 + i_2 = N_p(sC_1) - N_p(sC_2) = N_p s(C_1 - C_2)$

$\therefore v_o = -i_o \left(\frac{1}{sC_F} \right) = -N_p \left(\frac{C_1 - C_2}{C_F} \right)$

$\frac{v_o}{v_p} = -\frac{C_1 - C_2}{C_F} \Rightarrow$ A seemingly perfect differential sensor/amplifier output! ... but only when the op amp is ideal...

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Buffer-Bootstrapped Position Sensing

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$+V_P$
 $-V_P$

Includes capacitance from interconnects, bond pads, and C_{gs} of the op amp

v_o

Unity Gain Buffer

C_p

C_{gd} = gate-to-drain capacitance of the input MOS transistor

• Bootstrap the ground lines around the interconnect and bond pads

- ⊗ No voltage across C_p
- ⊗ It's effectively not there!

Interconnect
 Ground Plane
 1x

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Effect of Finite Op Amp Gain

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$+V_P$
 $-V_P$

Total ADXL-50 Sense $C \sim 100\text{fF}$

z_i

N_i

i_i

C_p

C_{gd}

Unity Gain Buffer

v_o

$v_o = A_0(v_i - v_o) \Rightarrow v_o(1 + A_0) = A_0 v_i \Rightarrow \frac{v_o}{v_i} = \frac{A_0}{1 + A_0}$

Get $z_i = \frac{v_i}{i_i}$: $i_i = (N_i - v_o) sC_p = N_i \left(1 - \frac{A_0}{1 + A_0} \right) sC_p = N_i \frac{1}{1 + A_0} sC_p$

$\therefore \frac{N_i}{i_i} = z_i = \frac{1}{s \left[\frac{C_p}{1 + A_0} \right]}$ $C_{eff} = \frac{C_p}{1 + A_0}$

No longer zero!

Ex: $A_0 = 100$, $C_p = 2\text{pF}$
 $\Rightarrow C_{eff} = \frac{2\text{pF}}{101} = 20\text{fF}$
 Not negligible compared w/ ADXL-50 $C_{tot} \sim 100\text{fF}$!

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Integration of MEMS and Transistors

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Integrate or Not?

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- Benefits:**
 - Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
 - Better reliability
 - Reduced size → lower cost?
 - Reduced packaging complexity → integration is a form of packaging → lower cost?
 - Higher integration density supports greater functionality
- Challenges:**
 - Temperature ceilings imposed by the transistors or MEMS
 - Protecting one process from the other
 - Surface topography of MEMS
 - Material incompatibilities
 - Multiplication of yield losses (versus non-integrated)
 - Acceptance by transistor foundries

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250 nm CMOS Cross-Section

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Labels in diagram: D, G, Sub, 2nd Level Metal Interconnect (e.g., Cu), S, 1st Level Metal Interconnect (e.g., Al), Polysilicon Gate, LPCVD SiO₂, CVD Tungsten, TiN Local Interconnect, LOCOS Oxidation, N Well - PMOS Substrate, P Well - NMOS Substrate, Lightly Doped Drain (LDD), TiSi₂ Contact Barrier, Silicon Substrate.

28 masks and a lot more complicated than MEMS!

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Merged MEMS/Transistor Technologies (Process Philosophy)

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```

    graph LR
        subgraph MEMS-Last
            C1[Circuits] --> P1[Pass./Prot.] --> M1[μMechanics]
        end
        subgraph Mixed
            C2[Circuits] --> P2[Pass./Prot.] --> M2[μMechanics] --> P3[Pass./Prot.]
            C3[Circuits] --> P4[Pass./Prot.] --> M3[μMechanics] --> P5[Pass./Prot.]
        end
        subgraph MEMS-First
            M4[μMechanics] --> P6[Pass./Prot.] --> C4[Circuits]
        end
        M1 --> IO[Fully Integrated μMechanical Resonator Oscillator]
        P3 --> IO
        P5 --> IO
        C4 --> IO
    
```

- Mixed:**
 - problem: multiple passivation/protection steps ⇒ large number of masks required
 - problem: custom process for each product
- MEMS-first or MEMS-last:**
 - adv.: modularity ⇒ flexibility ⇒ less development time
 - adv.: low pass./protection complexity ⇒ fewer masks

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Analog Devices BiMEMS Process

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- Interleaved MEMS and 4 μm BiMOS processes (28 masks)
- Diffused n+ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers

Legend:

SILICON	LPCVD NITRIDE	SPACER LTO	PLASMA OXIDE
OXIDE	BPSG	SENSOR POLYSI	PLASMA NITRIDE
POLYSI	LTO	METAL	

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Analog Devices BiMEMS Process (cont)

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• **Examples:**

Old → New

Analog Devices ADXL 78

Analog Devices ADXL-202 Multi-Axis Accelerometer

• Can you list the advances in the process from old to new?

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Merged MEMS/Transistor Technologies (Process Philosophy)

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Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. → Fully Integrated μMechanical Resonator Oscillator

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

• **Mixed:**

- ⊘ **problem:** multiple passivation/protection steps ⇒ large number of masks required
- ⊘ **problem:** custom process for each product

• **MEMS-first or MEMS-last:**

- ⊘ **adv.:** modularity ⇒ flexibility ⇒ less development time
- ⊘ **adv.:** low pass./protection complexity ⇒ fewer masks

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MEMS-First Integration

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- **Modular technology** minimizes product updating effort
 - ⊘ **Module 1:** micromachining process (planar technology)
 - ⊘ **Module 2:** transistor process (planar IC technology)
- **Adv.:** (ideally) no changes needed to the transistor process
- **Adv.:** high temperature ceiling for some MEMS materials
- **Challenges:**
 - ⊘ Reducing topography after MEMS processing so transistors can be processed
 - ⊘ Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
 - ⊘ Getting transistor foundries to accept pre-processed wafers

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MEMS-First Integration

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- **Problem:** μstructural topography interferes with lithography
 - ⊘ difficult to apply photoresist for submicron circuits

- **Soln.:** build μmechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]

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MEMS-First Ex: Sandia's iMEMS

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- Used to demonstrate functional fully integrated oscillators
- Issues:
 - lithography and etching may be difficult in trench \Rightarrow may limit dimensions (not good for RF MEMS)
 - μ mechanical material must stand up to IC temperatures ($>1000^\circ\text{C}$) \Rightarrow problem for some metal materials
 - might be contamination issues for foundry IC's

[Smith et al, IEDM'95]

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Bosch/Stanford MEMS-First Process

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- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

[Kim, Kenny Trans'05]

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Problems With MEMS-First

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- Many masking steps needed, plus CMP required \rightarrow cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
 - Precludes the use of structural materials with low temperature req'ts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
 - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

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Foundry Acceptance of MEMS-First?

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- Is a CMP'ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP'ed surface and removed via a wet etch to yield a "pristine" surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
 - Feature sizes on the nm scale for billions of devices
 - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
 - Many foundries will not accept any pre-processed wafers, MEMS or not \rightarrow just can't guarantee working transistor circuits with unknowns in starting silicon

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Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. → Circuits

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

Fully Integrated μMechanical Resonator Oscillator

- Mixed:**
 - problem: multiple passivation/protection steps ⇒ large number of masks required
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- MEMS-first or MEMS-last:**
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MEMS-Last Integration

- Modular technology minimizes product updating effort
 - Module 1: transistor process (planar IC technology)
 - Module 2: micromachining process (planar technology)
- Adv.: foundry friendly
 - Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- Issue: limited thermal budget limits the set of usable structural materials
 - Metallization goes bad if temperature gets too high
 - Aluminum grows hillocks and spikes junctions if $T > 500^{\circ}\text{C}$
 - Copper diffusion can be an issue at high temperature
 - Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C

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Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
 - Polysilicon dep. $T \sim 600^{\circ}\text{C}$; nitride dep. $T \sim 835^{\circ}\text{C}$
 - 1100°C RTA stress anneal for 1 min.
 - metal and junctions must withstand temperatures $\sim 835^{\circ}\text{C}$
 - tungsten metallization used with TiSi_2 contact barriers
 - in situ doped structural polySi; rapid thermal annealing

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Surface Micromachining

Structural Material (e.g., polysilicon, nickel, etc.)

Release Etch Barrier

Sacrificial Oxide

Silicon Substrate

pwell

Hydrofluoric Acid Release Solution

Free-Standing Resonator Beam

Silicon Substrate

pwell

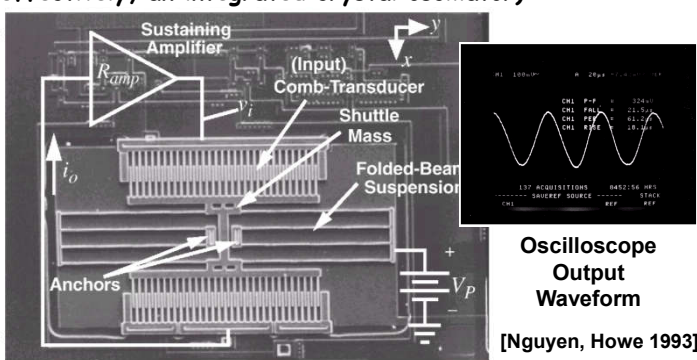
- Fabrication steps compatible with planar IC processing

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Single-Chip Ckt/MEMS Integration

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- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)



300 μm

Sustaining Amplifier
Input Comb-Transducer
Shuttle Mass
Folded-Bear Suspension
Anchors

R_{amp}
 i_o
 V_p

Oscilloscope Output Waveform

CH1	P-P	F	224.00
CH1	P-P	F	22.12
CH1	P-P	F	82.20
CH1	P-P	F	18.20

[Nguyen, Howe 1993]

- To allow the use of $>600^\circ\text{C}$ processing temperatures, tungsten (instead of aluminum) is used for metallization

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