

### Merged MEMS/Transistor Technologies (Process Philosophy)

Post-Circuits: Circuits → Pass./Prot. → μMechanics

Mixed: Circuits → Pass./Prot. → μMechanics → Pass./Prot. → Circuits

Pre-Circuits: μMechanics → Pass./Prot. → Circuits

Fully Integrated μMechanical Resonator Oscillator

- Mixed:**
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product
- MEMS-first or MEMS-last:**
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks

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### MEMS-Last Integration

- Modular technology minimizes product updating effort
  - Module 1: transistor process (planar IC technology)
  - Module 2: micromachining process (planar technology)
- Adv.: foundry friendly
  - Virtually any foundry can be used → can use the lowest cost transistor circuits (big advantage)
- Adv.: topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers
- Issue: limited thermal budget limits the set of usable structural materials
  - Metallization goes bad if temperature gets too high
  - Aluminum grows hillocks and spikes junctions if  $T > 500^\circ\text{C}$
  - Copper diffusion can be an issue at high temperature
  - Low-k dielectrics used around metals may soon lower the temperature ceiling to only  $320^\circ\text{C}$

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### Berkeley Polysilicon MICS Process

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep.  $T \sim 600^\circ\text{C}$ ; nitride dep.  $T \sim 835^\circ\text{C}$
  - $1100^\circ\text{C}$  RTA stress anneal for 1 min.
  - metal and junctions must withstand temperatures  $\sim 835^\circ\text{C}$
  - tungsten metallization used with  $\text{TiSi}_2$  contact barriers
  - in situ* doped structural polySi; rapid thermal annealing

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### Surface Micromachining

- Release Etch Barrier
- Structural Material (e.g., polysilicon, nickel, etc.)
- Sacrificial Oxide
- Silicon Substrate
- pwell
- Hydrofluoric Acid Release Solution
- Free-Standing Resonator Beam

- Fabrication steps compatible with planar IC processing

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### Single-Chip Ckt/MEMS Integration

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- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)

Oscilloscope Output Waveform  
 [Nguyen, Howe 1993]

- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

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### Usable MEMS-Last Integration

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- Problem:** tungsten is not an accepted primary interconnect metal
- Challenge:** retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al, MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable

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### Poly-SiGe MICS Process

UC Berkeley

- MICS = "Modular Integration of Circuits and Structures"
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe ~450°C
  - Adv.: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

[Franke, Howe 2001]

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### Polysilicon Germanium

UC Berkeley

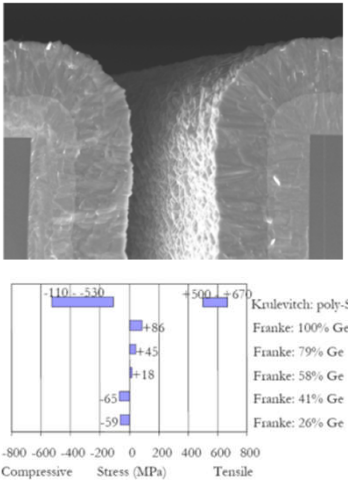
- Deposition**
  - LPCVD thermal decomposition of GeH<sub>4</sub> and SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub>
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation
- Dry Etching**
  - Similar to poly-Si, use F, Cl, and Br<sup>-</sup> containing plasmas
  - Rate ~0.4 μm/min
- Wet Etching**
  - H<sub>2</sub>O<sub>2</sub> @ 90°C: can get 4 orders of magnitude selectivity between >80% and <60% Ge content
  - Good release etchant

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### Poly-SiGe Mechanical Properties

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- Conformal deposition
- Low as-deposited stress (when its done right)
- Young's modulus  $\sim 146$  GPa (for poly-Si<sub>0.35</sub>Ge<sub>0.65</sub>)
- Density  $\sim 4280$  kg/m<sup>3</sup>
- Acoustic velocity  $\sim 5840$  m/s (25% lower than polysilicon)
  - Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q=30,000 for n-type poly-Ge in vacuum



Stress (MPa) values: -110, -530, -65, -59, +86, +45, +18, +500, +670

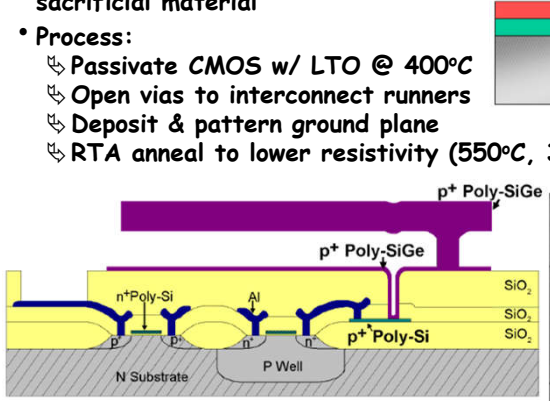
Legend for Krulevitch: poly-Si  
 Franke: 100% Ge  
 Franke: 79% Ge  
 Franke: 58% Ge  
 Franke: 41% Ge  
 Franke: 26% Ge

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### UCB Poly-SiGe MICS Process

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- 2  $\mu\text{m}$  standard CMOS process w/ Al metallization
- P-type poly-Si<sub>0.35</sub>Ge<sub>0.65</sub> structural material; poly-Ge sacrificial material
- Process:
  - Passivate CMOS w/ LTO @ 400°C
  - Open vias to interconnect runners
  - Deposit & pattern ground plane
  - RTA anneal to lower resistivity (550°C, 30s)



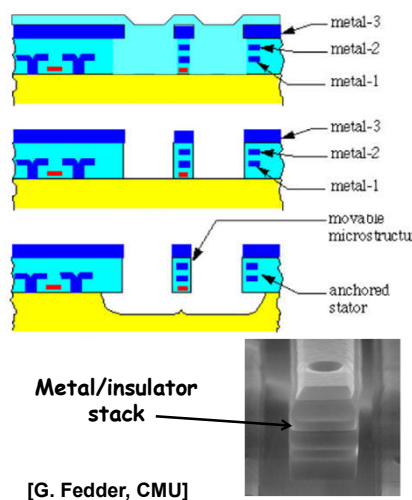
Transistor Circuits

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### ASIMPS Ckt/MEMS Integration Process

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- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF<sub>3</sub>/O<sub>2</sub> oxide etch
- Structures released via a final SF<sub>6</sub> isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky
  - Must design defensively against warping



Labels: metal-3, metal-2, metal-1, movable microstructure, anchored stator, Metal/insulator stack

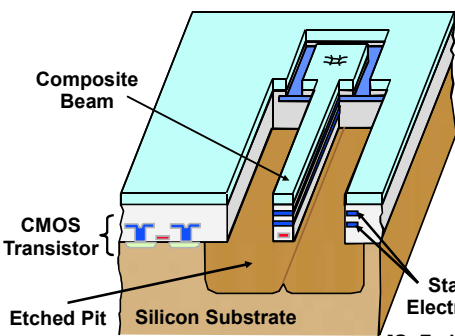
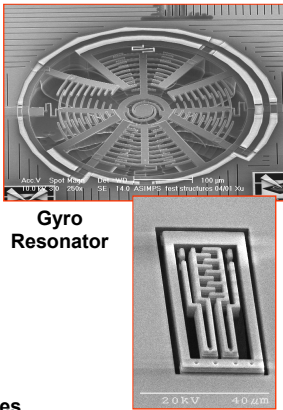
[G. Fedder, CMU]

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### ASIMPS Ckt/MEMS Integration Process

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- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

Labels: Composite Beam, CMOS Transistor, Etched Pit, Silicon Substrate, Stator Electrodes

Gyro Resonator  
Uncooled IR Detector Element

[G. Fedder, CMU]

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### Effect of Finite Op Amp Gain

Total ADXL-50 Sense C ~ 100ff

$N_0 = A_0(N_i - N_-) = A_0(N_i - N_0) \rightarrow N_0(1 + A_0) = A_0 N_i \rightarrow \frac{N_0}{N_i} = \frac{A_0}{1 + A_0}$

Get  $Z_i = \frac{V_i}{i_i}$ :  $i_i = (N_i - N_0) s C_p = N_i \left(1 - \frac{A_0}{1 + A_0}\right) s C_p = N_i \frac{1}{1 + A_0} s C_p$

$\therefore \frac{N_i}{i_i} = Z_i = \frac{1}{s \left[ \frac{C_p}{1 + A_0} \right]} \rightarrow C_{eff} = \frac{C_p}{1 + A_0}$

No longer zero!

Ex:  $A_0 = 100, C_p = 2 \text{ pF}$   
 $\Rightarrow C_{eff} = \frac{2 \text{ pF}}{101} = 20 \text{ ff}$   
 Not negligible compared w/ ADXL-50 Ctot ~ 100 ff!

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