EE C247B – ME C218
Introduction to MEMS Design
Spring 2019

Prof. Clark T.-C. Nguyen

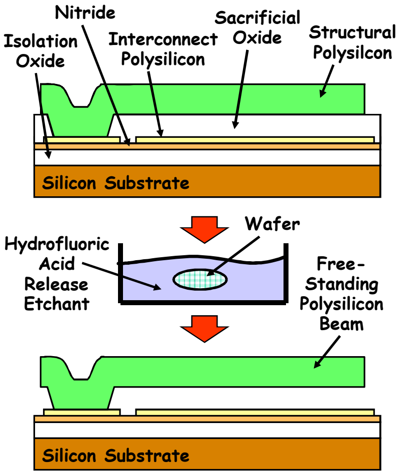
Dept. of Electrical Engineering & Computer Sciences
University of California at Berkeley
Berkeley, CA 94720

Lecture Module 5: Surface Micromachining

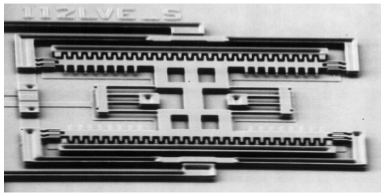
Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: "Surface Micromachining for Microelectromechanical Systems"
- Lecture Topics:
  - Polysilicon surface micromachining
  - Stiction
  - Residual stress
  - Topography issues
  - Nickel metal surface micromachining
  - 3D "pop-up" MEMS
  - Foundry MEMS: the "MUMPS" process
  - The Sandia SUMMIT process

Polysilicon Surface-Micromachining



- Uses IC fabrication instrumentation exclusively
- *Variations*: sacrificial layer thickness, fine- vs. large-grained polysilicon, *in situ* vs. $POCL_3$-doping



300 kHz Folded-Beam Micromechanical Resonator

Polysilicon

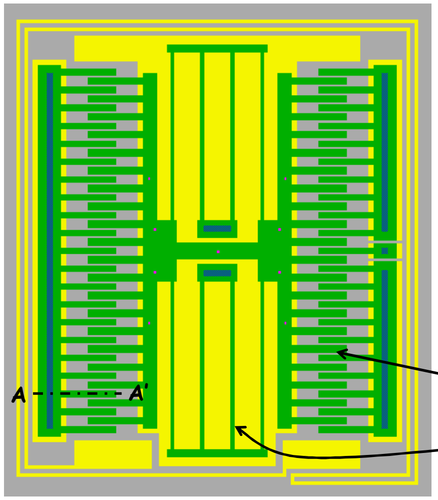
Why Polysilicon?

- Compatible with IC fabrication processes
  - Process parameters for gate polysilicon well known
  - Only slight alterations needed to control stress for MEMS applications
- Stronger than stainless steel: fracture strength of polySi ~ 2-3 GPa, steel ~ 0.2GPa-1GPa
- Young's Modulus ~ 140-190 GPa
- Extremely flexible: maximum strain before fracture ~ 0.5%
- Does not fatigue readily

- Several variations of polysilicon used for MEMS
  - LPCVD polysilicon deposited undoped, then doped via ion implantation, PSG source, $POCl_3$, or B-source doping
  - In situ-doped LPCVD polysilicon
  - Attempts made to use PECVD silicon, but quality not very good (yet) → etches too fast in HF, so release is difficult

Polysilicon Surface-Micromachining Process Flow

Layout and Masking Layers



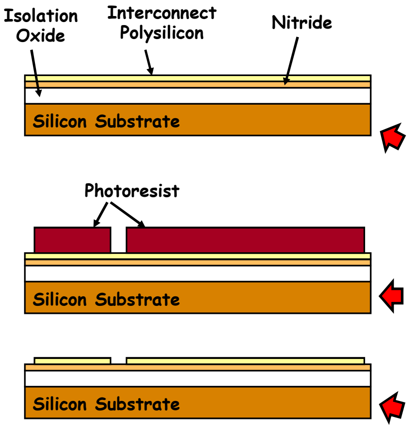
- At Left: Layout for a folded-beam capacitive comb-driven micromechanical resonator
- Masking Layers:
  - 🟨 1st Polysilicon: POLY1(cf) ← clear field
  - 🟦 Anchor Opening: ANCHOR(df) ← dark field
  - 🟩 2nd Polysilicon: POLY2(cf)

Capacitive comb-drive for linear actuation

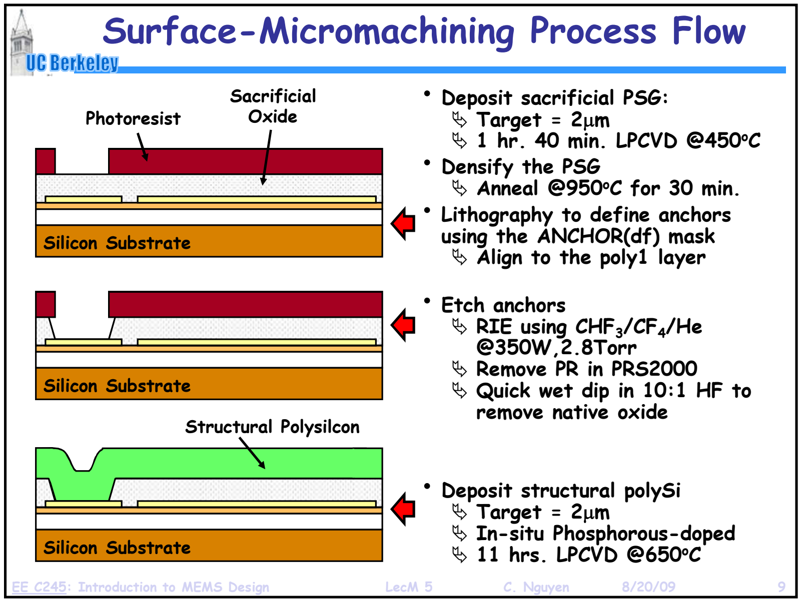
Folded-beam support structure for stress relief

Surface-Micromachining Process Flow

Cross-sections through A-A'

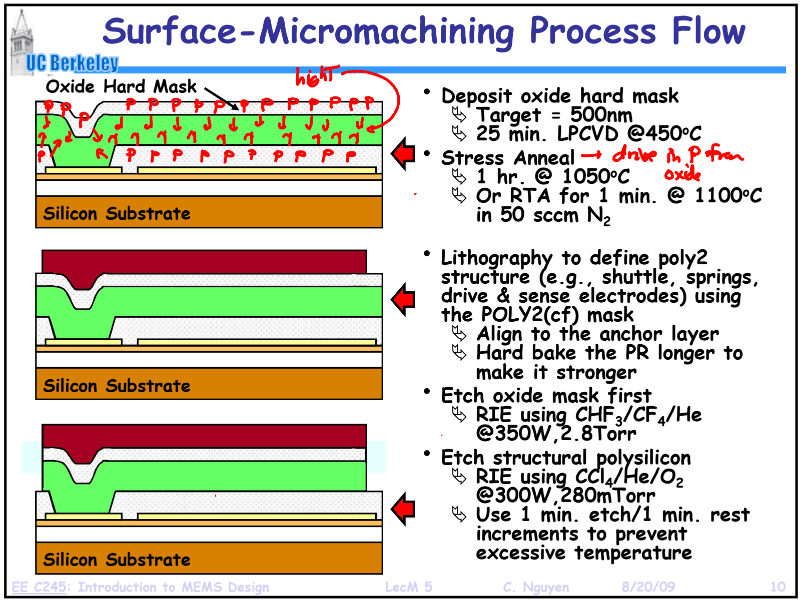


- Deposit isolation LTO (or PSG):
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO (or PSG)
  - Anneal @950°C for 30 min.
- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Deposit interconnect polySi:
  - Target = 300nm
  - In-situ Phosphorous-doped
  - 1 hr. 30 min. LPCVD @650°C
- Lithography to define poly1 interconnects using the POLY1(cf) mask
- RIE polysilicon interconnects:
  - $CCl_4/He/O_2$ @300W, 280mTorr
- Remove photoresist in PRS2000



Surface-Micromachining Process Flow

- Deposit sacrificial PSG:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the PSG
  - Anneal @950°C for 30 min.
- Lithography to define anchors using the ANCHOR(df) mask
  - Align to the poly1 layer
- Etch anchors
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr
  - Remove PR in PRS2000
  - Quick wet dip in 10:1 HF to remove native oxide
- Deposit structural polySi
  - Target = 2μm
  - In-situ Phosphorous-doped
  - 11 hrs. LPCVD @650°C



Surface-Micromachining Process Flow

- Deposit oxide hard mask
  - Target = 500nm
  - 25 min. LPCVD @450°C
- Stress Anneal → drive in P from oxide
  - 1 hr. @ 1050°C
  - Or RTA for 1 min. @ 1100°C in 50 sccm N_2
- Lithography to define poly2 structure (e.g., shuttle, springs, drive & sense electrodes) using the POLY2(cf) mask
  - Align to the anchor layer
  - Hard bake the PR longer to make it stronger
- Etch oxide mask first
  - RIE using $CHF_3/CF_4/He$ @350W,2.8Torr
- Etch structural polysilicon
  - RIE using $CCl_4/He/O_2$ @300W,280mTorr
  - Use 1 min. etch/1 min. rest increments to prevent excessive temperature