Residual Stress

After release, poorly designed microstructures might buckle, bend, or warp → often caused by residual film stress

Origins of residual stress, \( \sigma \)

- Non-equilibrium deposition
- Grain morphology change
- Gas entrapment
- Doping
- Thermal stresses
  - Thermal expansion mismatch of materials → introduce stress during cool-down after deposition
  - Annealing

Need to Control Film Stress

* Resonance frequency expression for a lateral resonator:

\[
f_0 = \frac{1}{2\pi} \sqrt{\frac{4E_y\tau W^3}{ML^3} + \frac{24\sigma_t W}{5ML}}
\]

Since \( W \ll L \), the stress term will dominate if \( \sigma_t \approx E_y \)

Tensile Versus Compressive Stress

* Under tensile stress, a film wants to shrink w/r to its substrate
  - Caused, e.g., by differences in film vs. substrate thermal expansion coefficients
  - If suspended above a substrate and anchored to it at two points, the film will be "stretched" by the substrate

* Under compressive stress, a film wants to expand w/r to its substrate
  - If suspended above a substrate and anchored to it at two points, the film will buckle over the substrate
**Vertical Stress Gradients**

- Variation of residual stress in the direction of film growth
- Can warp released structures in z-direction

**Stress in Polysilicon Films**

- Stress depends on crystal structure, which in turn depends upon the deposition temperature
  - Temperature ≤ 600°C
    - Films are initially amorphous, then crystallize
    - Get equiaxed crystals, largely isotropic
    - Crystals can have higher density when cooled — tensile stress
    - Small stress gradient
  - Temperature ≥ 600°C
    - Columnar crystals grow during deposition
    - As crystals grow vertically and in-plane they effectively push on neighbors (when cooled to room temperature) → compressive stress
    - Positive stress gradient

**Annealing Out Polysilicon Stress**

- Control polySi stress by annealing at high temperatures
  - Typical anneal temperatures: 900-1150°C
  - Grain boundaries move, relax
  - Can dope while annealing by sandwiching the polysilicon between similarly doped oxides (symmetric dopant drive-in), e.g. using 10-15 wt. % PSG

- Rapid thermal anneal (RTA) also effective (surprisingly)

**Topography Issues**

- Degradation of lithographic resolution
  - PR step coverage, streaking
  - Stringers
    - Problematic when using anisotropic etching, e.g., RIE

Nickel Surface-Micromachining Process Flow

Nickel Metal Surface-Micromachining

* Deposit isolation LTO:
  * Target = 2μm
  * 1 hr, 40 min. LPCVD @450°C
* Densify the LTO
  * Anneal @950°C for 30 min.

* Define metal interconnect via lift-off
  * Spin photoresist and pattern lithographically to open areas where interconnect will stay
  * Evaporate a Ti/Au layer
    * Target = 30nm Ti
    * Target = 270nm Au
  * Remove photoresist in PRS2000
  * Electroplate nickel to fill the anchor vias
    * Use solution of nickel sulfamate @ 50°C

Electroplating: Metal MEMS

* Use electroplating to obtain metal structures
* When thick: call it “LIGA”
* Pros: fast low temp deposition, very conductive
* Cons: drift, low mech. Q but may be solvable?

Nickel Metal Surface-Micromachining

* Evaporate Al to serve as a sacrificial layer
  * Target < 1μm

* Lithography to define anchor openings

* Wet etch the aluminum to form anchor vias
  * Use solution of H₃PO₄/HNO₃/H₂O

* Remove photoresist in PRS2000

* Electroplate nickel to fill the anchor vias
  * Use solution of nickel sulfamate @ 50°C
  * Time the electroplating to planarize the surface
Nickel Metal Surface-Micromachining

- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm²

Nickel Metal Surface-Micromachining Example

- Below: Surface-micromachined in nickel using the described process flow

Nickel Surface-Micromachining Example

- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant

- Release the structures
  - Use a K₄Fe(CN)₆/NaOH etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au

3D “Pop-up” MEMS

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Pop-Up MEMS

First MEMS hinge
[K. Pister, et al., 1992]

Corner Cube Reflector
[v. Hsu, 1999]

3D Direct-Assembled Tunable L

[Ming Wu, UCLA]

Pop-Up MEMS

* Pictured: hinged Campanile made in SUMMiT process, assembled using probes [Elliot Hui, et al.]

Hinge Process Flow

Deposit first sacrificial
Deposit and pattern first poly

Deposit and pattern second sacrificial

Pattern contacts
Deposit and pattern second poly

Etch sacrificial
Assemble part
"Foundry" MEMS: The MUMPS Process

MUMPS: MultiUser MEMS Process

- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm² dies

Micromotor fabricated via MUMPS

MUMPS: MultiUser MEMS Process

Micromotor Example

Masks in polyMUMPS

- Minimum set of masks that must be used in MUMPS

<table>
<thead>
<tr>
<th>Membrane level name</th>
<th>Field type</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0</td>
<td>light</td>
<td>pattern ground plane</td>
</tr>
<tr>
<td>ANCHOR1</td>
<td>dark</td>
<td>open holes for Poly 1 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>DIMPLE</td>
<td>dark</td>
<td>create dimples/bushings for Poly 1</td>
</tr>
<tr>
<td>POLY1</td>
<td>light</td>
<td>pattern Poly 1</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>dark</td>
<td>open holes for Poly 1 to Poly 2 connection</td>
</tr>
<tr>
<td>ANCHOR2</td>
<td>dark</td>
<td>open holes for Poly 2 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>POLY2</td>
<td>light</td>
<td>pattern Poly 2</td>
</tr>
<tr>
<td>METAL</td>
<td>light</td>
<td>pattern Metal</td>
</tr>
<tr>
<td>HOLE0</td>
<td>dark</td>
<td>provide holes for POLY0</td>
</tr>
<tr>
<td>HOLE1</td>
<td>dark</td>
<td>provide release holes for POLY1</td>
</tr>
<tr>
<td>HOLE2</td>
<td>dark</td>
<td>provide release holes for POLY2</td>
</tr>
<tr>
<td>HOLEM</td>
<td>dark</td>
<td>provide release holes in METAL</td>
</tr>
</tbody>
</table>

- Field type:
  - Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
  - Dark field (df): in layout, boxes represent holes to be cut out

Extra masks for more flexibility & ease of release
MUMPS Process Flow

- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 µm of PSG as the 1st sacrificial layer
- Lithography using the DIMPLE(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1(df) mask (align to poly0)
- RIE anchor vias down to the nitride surface
- LPCVD 2 µm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  % This both dopeds the polysilicon and reduces its residual stress
- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then
- RIE the polysilicon
- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA(df) mask to define contacts to the poly1 layer (align to poly1)

MUMPS Process Flow (cont.)

- Recast with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings
- LPCVD 1.5 µm undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress
- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask

MUMPS Process Flow (cont.)

- Lithography using the METAL(df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer
- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed

Final Structure: Micromotor
**MUMPS: MultiUser MEMS Process**

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Micromotor fabricated via MUMPS

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**polyMUMPS Minimum Feature Constraints**

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

<table>
<thead>
<tr>
<th>Rule</th>
<th>Min Feature [μm]</th>
<th>Min Spacing [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0, POLY1, POLY2</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>ANCHOR1, ANCHOR2</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>DIMPLE</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>METAL</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>HOLE1, HOLE2</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>HOLEM</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

---

**MUMPS Design Rules (cont.)**

- POLY0 space to ANCHOR1
- POLY0 enclose ANCHOR1
- POLY0 enclose POLY1
- POLY0 enclose POLY2
- POLY0 enclose ANCHOR2
- POLY0 space to ANCHOR2

---

**MUMPS Design Rules (cont.)**

- POLY1 enclose ANCHOR1
- POLY1 enclose DIMPLE
- POLY1 enclose POLY1_POLY2_VIA
- POLY1 enclose POLY2
- POLY1 space to ANCHOR2

- Poly1 etch holes space in POLY1: 5 (max. value)

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The Sandia SUMMIT Process

Sandia's SUMMiT V

* SUMMIT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process
  - Five-layer polysilicon surface micromachining process
  - One electrical interconnect layer & 4 mechanical layers
  - Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  - 14 masks
**SUMMiT V Layer Stack**

- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized.

**Chemical Mechanical Polishing (CMP)**

- **Used to planarize the top surface of a semiconductor wafer or other substrate.**
- **Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad.**
  - Wafer and pad are pressed together.
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing.

**Actual SUMMiT Cross-Section**

- **No CMP until after the first three polySi layers.**
- **1 µm mmpoly1 and 1.5 µm mmpoly2 can be combined to form a 2.5 µm polysilicon film.**
- **Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions.**

**CMP: Not the Same as Lapping**

- **Lapping** is merely the removal of material to flatten a surface without selectivity.
- **Everything is removed at approximately the same rate.**

- **Chemical Mechanical Polishing** is selective to certain films and not selective to others.
- **Stops at non-selective layer.**

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