EE C247B – ME C218
Introduction to MEMS Design
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Module 16: Sensing Ckt. Non-Idealities & Integration

Lecture Outline

* Reading: Senturia Chpt. 14, 15
* Lecture Topics:
  - Ideal Op Amps
  - Op Amp Non-Idealities
  - MEMS-Transistor Integration
    - Mixed
    - MEMS-First
    - MEMS-Last
# Ideal Operational Amplifiers

## Equivalent Circuit of an Ideal Op Amp:

- **Single-ended output**
- **Differential input**
- **Voltage-Controlled Voltage Source (VCVS)**

## Properties of Ideal Op Amps:

1. \( R_{in} = \infty \)  
2. \( R_0 = 0 \)  
3. \( A = \infty \)  
4. \( i_+ = i_- = 0 \)  
5. \( v_+ = v_- \) (assuming \( v_0 = \text{finite} \))  

**Why?**
Ideal Op Amp (cont)

- Properties of Ideal Op Amps:
  1. \( R_{in} = \infty \)
  2. \( R_0 = 0 \)
  3. \( A = \infty \)
  4. \( i_+ = i_- = 0 \)
  5. \( v_+ = v_- \), assuming \( v_0 = \text{finite} \)

Why? Because for

\[ \infty (v_+ - v_-) = v_0 = \text{finite} \]

\[ \therefore v_+ - v_- = 0 \rightarrow v_+ = v_- \]

\[ v_0 \Rightarrow \text{virtual short circuit (virtual ground)} \]

- Big assumption! \((v_0 = \text{finite})\)
- How can we assume this? We can assume this only when there is an appropriate negative feedback path!

Inverting Amplifier

- Verify that there is negative FB.
- \( \because v_0 = \text{finite} \rightarrow v_+ = v_- \rightarrow \) node attached to (-) terminal is virtual ground.
- \( i_- = 0 \rightarrow i_1 = i_2 \)

\[ i_1 = \frac{v_0 - 0}{R_1} = \frac{v_0}{R_1} = i_2 \]

\[ v_0 = 0 - i_2 R_2 = -i_2 R_2 \]

\[ \Rightarrow v_0 = \left( \frac{v_1}{R_1} \right) R_2 = -\frac{R_2}{R_1} v_1 \]

\[ \therefore v_0 = -\frac{R_2}{R_1} v_1 \]

Benefit: Any shunt \( C \) at this node will be grounded out.

NOTE: Gain dependent only on \( R_1 \) & \( R_2 \) (external components), not on the op amp gain.
1. Verify that there is neg. FB \rightarrow yes, since same FB as inverting amplifier
2. Thus, \( v_o = \) finite \rightarrow \( v_+ = v_- \rightarrow (\text{-}) \) terminal is virtual ground
3. \( i_- = 0 \rightarrow i_1 = i_2 \)

\[
v_0 = -i_2 R_2 = -i R_2 \Rightarrow \quad \frac{v_0}{i} = -R_2
\]

An inverting amplifier is just a transresistance amplifier with an \( R_1 \) to convert voltage to current!
Actual Op Amps Are Not Ideal

- Actual op amps, of course, are not ideal; rather, they...
  - Generate noise
  - Have finite gain, \( A_o \)
  - Have finite bandwidth, \( \omega_b \)
  - Have finite input resistance, \( R_i \)
  - Have finite input capacitance, \( C_i \)
  - Have finite output resistance, \( R_o \)
  - Have an offset voltage \( V_{OS} \) between their (+) and (-) terminals
  - Have input bias currents
  - Have an offset \( I_{OS} \) between the bias currents into the (+) and (-) terminals
  - Have finite slew rate
  - Have finite output swing (governed by the supply voltage used, \(-L\) to \(+L\))

- And what's worse: All of the above can be temperature (or otherwise environmentally) dependent!
Finite Op Amp Gain and Bandwidth

- For an ideal op amp: \( A = \infty \)
- In reality, the gain is given by: \( A(s) = \frac{A_0}{\frac{1}{s} + \frac{s}{\omega_b}} \)
- For \( \omega >> \omega_b \):
  \[ A(s) \approx \frac{A_0}{s} = \frac{\omega_T}{\omega_b} \]

This pole actually designed in for some op amps.

Open-loop response of the amplifier.

\[ 20 \log(A_0) \]

3 dB frequency

Unity gain frequency: \( \omega_T = A_0 \omega_b \)

Op Amp Non-Idealities

Input resistance \( R_i \) and Output Resistance \( R_o \):

With finite \( R_i \) and \( R_o \), and finite gain and BW, the op amp equivalent circuit becomes:

\[ v_+ \quad R_i \quad v_- \quad R_o \quad v_0 \]

\[ A \left( v_+ - v_- \right) \]

⇒ Basically reduces down to a voltage-amplifier model
⇒ Add an output \( C_0 \) to model a single pole response, where

\[ w_b = \frac{1}{R_0 C_0} \]
Input Offset Voltage $V_{OS}$

**Input Offset Voltage, $V_{OS}$:**

$$v_0 = A(v_+ - v_-)$$

**Ideal case:** $v_0 = 0$

**Reality:** $v_0 \neq 0$ (usually, $v_0 = L^+$ or $L^-$: it rails out!)

**Why?** Internal mismatches within the op amp → cause a dc offset. Model this with an equivalent input offset voltage $V_{OS}$.

Typically, $V_{OS} = 1\text{mV} - 5\text{mV}$

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Effect of $V_{OS}$ on Op Amp Circuits

**Example:** Non-Inverting Amplifier

$$V_0 = V_{OS} \left(1 + \frac{R_2}{R_1}\right)$$

e.g., $\frac{R_2}{R_1} = 9, \quad V_{OS} = 5\text{mV} \rightarrow V_0 = 50\text{mV}$

(not so bad ...)

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Effect of $V_{OS}$ on Op Amp Circuits (cont.)

Example: Integrator

To fix this, place a resistor in shunt with the $C \rightarrow$ then:

$$v_0 = V_{OS} \left( 1 + \frac{R_f}{R} \right)$$

$$v_0 = V_{OS} + \int_0^t i \, dt$$

$$= V_{OS} + \frac{1}{C} \int_0^t V_{OS} \, dt$$

$$= V_{OS} \left( 1 + \frac{t}{RC} \right) + v_C \bigg|_{t=0}$$

Will continue to increase until op amp saturates

Integrator-Based Diff. Position Sensing

Can drive next stage's $R_2$ into interferer to transfer function!

$$\frac{i_0}{V_P} = \frac{sC_2}{sC_2 + 1/C_F}$$

$V_P : = \frac{C_1 - C_2}{C_F}$

$\Rightarrow$ A seemingly perfect differential sensor/amplifier output... but only when the op amp is ideal...
Effect of Finite Op Amp Gain

\[ +V_p \] Total ADXL-50 Sense C \( \sim \) 100fF

Unity Gain Buffer

\[ -V_p \]

\[ N_0 = A_0 (N_i - N_e) \times A_e (N_i - N_e) \rightarrow N_0 \left(1 + \frac{1}{A_0}\right) \times A_0 N_i \rightarrow \frac{N_0}{N_i} \cdot \frac{A_0}{1 + A_0} \]

\[ \Rightarrow \frac{N_0}{N_i} \cdot \frac{A_0}{1 + A_0} \]

\[ \text{No longer zero!} \]

\[ \text{Ex: } A_e = 100, \ C_p = 2pF \]

\[ \Rightarrow \text{Ceff} = \frac{C_p}{1 + A_0} \]

\[ \text{Not negligibly compared w/ ADXL-50 Ceff } \sim 100\text{-}ff! \]

Integration of MEMS and Transistors
Integrate or Not?

Benefits:
- Lower parasitic capacitance and resistance → improved sensitivity and resolution, higher operation frequency
- Better reliability
- Reduced size → lower cost?
- Reduced packaging complexity → integration is a form of packaging → lower cost?
- Higher integration density supports greater functionality

Challenges:
- Temperature ceilings imposed by the transistors or MEMS
- Protecting one process from the other
- Surface topography of MEMS
- Material incompatibilities
- Multiplication of yield losses (versus non-integrated)
- Acceptance by transistor foundries

250 nm CMOS Cross-Section

Polysilicon Gate
LOCOS Oxidation
TiSi₂ Contact Barrier
Silicon Substrate

28 masks and a lot more complicated than MEMS!
Mixed:
- **problem**: multiple passivation/protection steps ⇒ large number of masks required
- **problem**: custom process for each product

MEMS-first or MEMS-last:
- **adv.**: modularity ⇒ flexibility ⇒ less development time
- **adv.**: low pass./protection complexity ⇒ fewer masks

**Analog Devices BiMEMS Process**

- Interleaved MEMS and $4 \mu m$ BiMOS processes (28 masks)
- Diffused $n^+$ runners used to interconnect MEMS & CMOS
- Relatively deep junctions allow for MEMS poly stress anneal
- Used to manufacture the ADXL-50 accelerometer and Analog Devices family of accelerometers
Analog Devices BiMEMS Process (cont)

* Examples:

Old → New

- Analog Devices ADXL 78
- Analog Devices ADXL-202 Multi-Axis Accelerometer

Can you list the advances in the process from old to new?

Mixed MEMS/Transistor Technologies (Process Philosophy)

- Mixed:
  - problem: multiple passivation/protection steps ⇒ large number of masks required
  - problem: custom process for each product

- MEMS-first or MEMS-last:
  - adv.: modularity ⇒ flexibility ⇒ less development time
  - adv.: low pass./protection complexity ⇒ fewer masks
MEMS-First Integration

- Modular technology minimizes product updating effort
  - **Module 1**: micromachining process (planar technology)
  - **Module 2**: transistor process (planar IC technology)
- **Adv.**: (ideally) no changes needed to the transistor process
- **Adv.**: high temperature ceiling for some MEMS materials
- **Challenges**:
  - Reducing topography after MEMS processing so transistors can be processed
  - Maximizing the set of permissible MEMS materials; the materials must be able to withstand transistor processing temperatures
  - Getting transistor foundries to accept pre-processed wafers

MEMS-First Integration

- **Problem**: µstructural topography interferes with lithography and difficult to apply photoresist for submicron circuits

- **Soln.**: build µmechanics in a trench, then planarize before circuit processing [Smith et al, IEDM'95]
MEMS-First Ex: Sandia’s iMEMS

- Used to demonstrate functional fully integrated oscillators
- Issues:
  - Lithography and etching may be difficult in trench ⇒ may limit dimensions (not good for RF MEMS)
  - μmechanical material must stand up to IC temperatures (>1000°C) ⇒ problem for some metal materials
  - Might be contamination issues for foundry IC's

Bosch/Stanford MEMS-First Process

- Single-crystal silicon microstructures sealed under epi-poly encapsulation covers
- Many masking steps needed, but very stable structures

[Kim, Kenny Trans'05]
Problems With MEMS-First

- Many masking steps needed, plus CMP required → cost can grow if you're not careful
- Processes using trenches sacrifice lithographic resolution in microstructures
- MEMS must withstand transistor processing temperatures
  - Precludes the use of structural materials with low temperature req'mts: metals, polymers, etc.
- Exotic MEMS (e.g., ZnO) that can contaminate transistors during their processing are not permissible
  - thus, not truly modular
- Foundry acceptance not guaranteed and might be rare

Foundry Acceptance of MEMS-First?

- Is a CMP’ed silicon surface sufficiently pure for fabrication of aggressively scaled transistors? How about if an oxide is grown over the CMP’ed surface and removed via a wet etch to yield a “pristine” surface?
- Is epi silicon grown as part of a sealing process sufficiently pure for fabrication of aggressively scaled transistors?
- CMOS is many times more difficult to run than MEMS
  - Feature sizes on the nm scale for billions of devices
  - Contamination a big issue: many foundries may not accept pre-processed wafers for contamination reasons
  - Many foundries will not accept any pre-processed wafers, MEMS or not → just can’t guarantee working transistor circuits with unknowns in starting silicon
**Merged MEMS/Transistor Technologies (Process Philosophy)**

- **Post-Circuits:** Circuits → Pass./Prot. → μMechanics → Fully Integrated μMechanical Resonator Oscillator

- **Mixed:**
  - **problem:** multiple passivation/protection steps ⇒ large number of masks required
  - **problem:** custom process for each product

- **MEMS-first or MEMS-last:**
  - **adv.:** modularity ⇒ flexibility ⇒ less development time
  - **adv.:** low pass./protection complexity ⇒ fewer masks

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**MEMS-Last Integration**

- **Modular technology minimizes product updating effort**
  - **Module 1:** transistor process (planar IC technology)
  - **Module 2:** micromachining process (planar technology)

- **Adv.:** foundry friendly
  - Virtually any foundry can be used ⇒ can use the lowest cost transistor circuits (big advantage)

- **Adv.:** topography after circuit fabrication is quite small, especially given the use of CMP to planarize the metallization layers

- **Issue:** limited thermal budget limits the set of usable structural materials
  - Metallization goes bad if temperature gets too high
  - Aluminum grows hillocks and spikes junctions if T>500°C
  - Copper diffusion can be an issue at high temperature
  - Low-k dielectrics used around metals may soon lower the temperature ceiling to only 320°C
**Berkeley Polysilicon MICS Process**

- Uses surface-micromachined polysilicon microstructures with silicon nitride layer between transistors & MEMS
  - Polysilicon dep. T~600°C; nitride dep. T~835°C
  - 1100°C RTA stress anneal for 1 min.
  - Metal and junctions must withstand temperatures ~835°C
  - Tungsten metallization used with TiSi$_2$ contact barriers
  - In situ doped structural polySi; rapid thermal annealing

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**Surface Micromachining**

- Fabrication steps compatible with planar IC processing
**Single-Chip Ckt/MEMS Integration**

- Completely monolithic, low phase noise, high-Q oscillator (effectively, an integrated crystal oscillator)
- To allow the use of >600°C processing temperatures, tungsten (instead of aluminum) is used for metallization

**Usable MEMS-Last Integration**

- **Problem**: tungsten is not an accepted primary interconnect metal
- **Challenge**: retain conventional metallization
  - minimize post-CMOS processing temperatures
  - explore alternative structural materials (e.g., plated nickel, SiGe [Franke, Howe et al., MEMS'99])
  - Limited set of usable structural materials → not the best situation, but workable
Poly-SiGe MICS Process

- MICS = “Modular Integration of Circuits and Structures”
- MEMS-last process, where SiGe micromechanics are planar processed directly above conventional foundry circuits
  - enabled by lower deposition temperature of SiGe ~450°C
  - Adv.: alleviates contamination issues of pre-circuit processes, allowing a wider choice of IC technologies

![Diagram of Poly-SiGe MICS Process]

[Franke, Howe 2001]

Polysilicon Germanium

- Deposition
  - LPCVD thermal decomposition of GeH₄ and SiH₄ or Si₂H₆
  - Rate >50 Å/min, T < 475°C, P = 300-600 mT
  - At higher [Ge]: rate ↑, T ↓
  - In-situ doping, ion implantation

- Dry Etching
  - Similar to poly-Si, use F, Cl, and Br-containing plasmas
  - Rate ~0.4 μm/min

- Wet Etching
  - H₂O₂ @ 90°C: can get 4 orders of magnitude selectivity between >80% and <60% Ge content
  - Good release etchant
Poly-SiGe Mechanical Properties

- Conformal deposition
- Low as-deposited stress (when its done right)
- Young’s modulus ~ 146 GPa (for poly-Si$_{0.35}$Ge$_{0.65}$)
- Density ~4280 kg/m$^3$
- Acoustic velocity ~5840 m/s (25% lower than polysilicon)
  - Harder to achieve high frequency devices
- Fracture strain 1.7% (compared to 1.5% for MUMPS polySi)
- Q=30,000 for n-type poly-Ge in vacuum

UCB Poly-SiGe MICS Process

- 2 μm standard CMOS process w/ Al metallization
- P-type poly-Si$_{0.35}$Ge$_{0.65}$ structural material; poly-Ge sacrificial material

  - Process:
    - Passivate CMOS w/ LTO @ 400°C
    - Open vias to interconnect runners
    - Deposit & pattern ground plane
    - RTA anneal to lower resistivity (550°C, 30s)
ASIMPS Ckt/MEMS Integration Process

- MEMS constructed from metal/insulator laminates of foundry CMOS
- Top metal layer used as etch mask for CHF$_3$/O$_2$ oxide etch
- Structures released via a final SF$_6$ isotropic dry etch
- Independent electrostatic actuation possible due to multiple insulated metal layers
- Stress issues can be tricky. Must design defensively against warping

[Image: Metal/insulator stack image]

ASIMPS Ckt/MEMS Integration Process

- Direct integration of Al/oxide MEMS structure with silicon CMOS or SiGe BiCMOS circuits
- Multiple electrodes within structures
- Derivatives for bulk silicon structures

[Image: Gyro Resonator and Detector Element images]
Effect of Finite Op Amp Gain

Total ADXL-50 Sense C ~ 100fF

\[ +V_p \]

\[ \begin{align*}
   & N_v = A_o (N_i - N_d) \cdot A_o (N_i - N_d) \rightarrow N_v (1 + A_o) \cdot A_o N_i \rightarrow \frac{N_v}{N_i} = \frac{A_o}{1 + A_o} \\
   & \text{Get } Z_c = \frac{N_v}{A_o} = \frac{1}{N_i} (1 + A_o) \cdot C_p \rightarrow C_{eff} = \frac{C_p}{1 + A_o} \\
   & \text{Ex: } A_o = 100, C_p = 2pF \Rightarrow C_{eff} = \frac{2pF}{101} = 20fF \\
   & \text{Not negligibly compared with ADXL50 so Ceff ~ 100 ff!}
\end{align*} \]