Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handout: “Surface Micromachining for Microelectromechanical Systems”
- Lecture Topics:
  - Polysilicon surface micromachining
  - Stiction
  - Residual stress
  - Topography issues
  - Nickel metal surface micromachining
  - 3D “pop-up” MEMS
  - Foundry MEMS: the “MUMPS” process
  - The Sandia SUMMIT process
Polysilicon Surface-Micromachining

- Uses IC fabrication instrumentation exclusively
- Variations: sacrificial layer thickness, fine- vs. large-grained polysilicon, in situ vs. POCl$_3$-doping

Silicon Substrate

Polysilicon

Hydrofluoric Acid Release Etchant

Free-Standing Polysilicon Beam

300 kHz Folded-Beam Micromechanical Resonator
Why Polysilicon?

- Compatible with IC fabrication processes
  - Process parameters for gate polysilicon well known
  - Only slight alterations needed to control stress for MEMS applications
- Stronger than stainless steel: fracture strength of polySi ~ 2-3 GPa, steel ~ 0.2GPa-1GPa
- Young's Modulus ~ 140-190 GPa
- Extremely flexible: maximum strain before fracture ~ 0.5%
- Does not fatigue readily

- Several variations of polysilicon used for MEMS
  - LPCVD polysilicon deposited undoped, then doped via ion implantation, PSG source, POCl₃, or B-source doping
  - In situ-doped LPCVD polysilicon
  - Attempts made to use PECVD silicon, but quality not very good (yet) → etches too fast in HF, so release is difficult
**Layout and Masking Layers**

- **At Left**: Layout for a folded-beam capacitive comb-driven micromechanical resonator

- **Masking Layers**:
  - 1st Polysilicon: POLY1(cf)
  - 2nd Polysilicon: POLY2(cf)
  - Anchor Opening: ANCHOR(df)

- Capacitive comb-drive for linear actuation
- Folded-beam support structure for stress relief

**Surface-Micromachining Process Flow**

- Deposit isolation LTO (or PSG):
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO (or PSG):
  - Anneal @950°C for 30 min.
- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Deposit interconnect polySi:
  - Target = 300nm
  - In-situ Phosphorous-doped
  - 1 hr. 30 min. LPCVD @650°C
- Lithography to define poly1 interconnects using the POLY1(cf) mask
- RIE polysilicon interconnects:
  - CCl₄/He/O₂ @300W, 280mTorr
- Remove photoresist in PRS2000
Surface-Micromachining Process Flow

- Deposit sacrificial PSG:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the PSG
  - Anneal @950°C for 30 min.
- Lithography to define anchors using the ANCHOR(df) mask
  - Align to the poly1 layer

- Etch anchors
  - RIE using CHF₃/CF₄/He
  - Remove PR in PRS2000
  - Quick wet dip in 10:1 HF to remove native oxide

- Deposit structural polySi
  - Target = 2μm
  - In-situ Phosphorous-doped
  - 11 hrs. LPCVD @650°C

Surface-Micromachining Process Flow

- Deposit oxide hard mask
  - Target = 500nm
  - 25 min. LPCVD @450°C
- Stress Anneal
  - 1 hr @ 1050°C
  - Or RTA for 1 min. @ 1100°C in 50 sccm N₂

- Lithography to define poly2 structure (e.g., shuttle, springs, drive & sense electrodes) using the POLY2(cf) mask
  - Align to the anchor layer
  - Hard bake the PR longer to make it stronger

- Etch oxide mask first
  - RIE using CHF₃/CF₄/He
  - Use 1 min. etch/1 min. rest increments to prevent excessive temperature
### Surface-Micromachining Process Flow

- **Remove PR (more difficult)**
  - Ash in O$_2$ plasma
  - Soak in PRS2000

- **Release the structures**
  - Wet etch in HF for a calculated time that insures complete undercutting
    - If 5:1 BHF, then ~ 30 min.
    - If 48.8 wt. % HF, ~ 1 min.
  - Keep structures submerged in DI water after the etch
- **Transfer structures to methanol**
- **Supercritical CO$_2$ dry release**

### Polysilicon Surface-Micromachined Examples

- Below: All surface-micromachined in polysilicon using variants of the described process flow

- Folded-Beam Comb-Driven Resonator
- Free-Free Beam Resonator
- Three-Resonator Micromechanical Filter
### Structural/Sacrificial Material Combinations

<table>
<thead>
<tr>
<th>Structural Material</th>
<th>Sacrificial Material</th>
<th>Etchant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-Si</td>
<td>SiO₂, PSG, LTO</td>
<td>HF, BHF</td>
</tr>
<tr>
<td>Al</td>
<td>Photoresist</td>
<td>O₂ plasma</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Poly-Si</td>
<td>XeF₂</td>
</tr>
<tr>
<td>Al</td>
<td>Si</td>
<td>TMAH, XeF₂</td>
</tr>
<tr>
<td>Poly-SiGe</td>
<td>Poly-Ge</td>
<td>H₂O₂, hot H₂O</td>
</tr>
</tbody>
</table>

- Must consider other layers, too, as release etchants generally have a finite E.R. on any material
- Ex: concentrated HF (48.8 wt. %)
  - Polysilicon E.R. ~ 0
  - Silicon nitride E.R. ~ 1-14 nm/min
  - Wet thermal SiO₂ ~ 1.8-2.3 μm/min
  - Annealed PSG ~ 3.6 μm/min
  - Aluminum (Si rich) ~ 4 nm/min (much faster in other Al)

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**Wet Etch Rates (f/ K. Williams)**

<table>
<thead>
<tr>
<th>Material</th>
<th>Wet Etch Rates (μm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.8 – 2.3</td>
</tr>
<tr>
<td>SiO₂</td>
<td>1.8</td>
</tr>
<tr>
<td>PSG</td>
<td>3.6</td>
</tr>
<tr>
<td>Al</td>
<td>4</td>
</tr>
<tr>
<td>Ge</td>
<td>0.5</td>
</tr>
<tr>
<td>SiGe</td>
<td>0.5</td>
</tr>
<tr>
<td>XeF₂</td>
<td>0.5</td>
</tr>
<tr>
<td>H₂O₂</td>
<td>0.5</td>
</tr>
</tbody>
</table>

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Note: Values in parentheses (%): W = weight, n = number, f = frequency of cycle and rate of etch. Values are average etch rates and may vary depending on the conditions such as temperature, pressure, and concentration of the etchant.
Film Etch Chemistries

* For some popular films:

<table>
<thead>
<tr>
<th>Material</th>
<th>Wet etchant</th>
<th>Etch rate [nm/min]</th>
<th>Dry etchant</th>
<th>Etch rate [nm/min]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polysilicon</td>
<td>HNO₃:H₂O:NH₄F</td>
<td>120-600</td>
<td>SF₆ + He</td>
<td>170-920</td>
</tr>
<tr>
<td>Silicon nitride</td>
<td>H₃PO₄</td>
<td>5</td>
<td>SF₆</td>
<td>150-250</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>HF</td>
<td>20-2000</td>
<td>CHF₃ + O₂</td>
<td>50-150</td>
</tr>
<tr>
<td>Aluminum</td>
<td>H₃PO₄:HNO₃:CH₃COOH</td>
<td>660</td>
<td>Cl₂ + SiCl₄</td>
<td>100-150</td>
</tr>
<tr>
<td>Photoresist</td>
<td>Acetone</td>
<td>&gt;4000</td>
<td>O₂</td>
<td>35-3500</td>
</tr>
<tr>
<td>Gold</td>
<td>KI</td>
<td>40</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Issues in Surface Micromachining

* Stiction: sticking of released devices to the substrate or to other on-chip structures
  - Difficult to tell if a structure is stuck to substrate by just looking through a microscope
* Residual Stress in Thin Films
  - Causes bending or warping of microstructures
  - Limits the sizes (and sometimes geometries) of structures
* Topography
  - Stringers can limit the number of structural levels
Microstructure Stiction

*Stiction*: the unintended sticking of MEMS surfaces

*Release stiction:*
- Occurs during drying after a wet release etch
- Capillary forces of droplets pull surfaces into contact
- Very strong sticking forces, e.g., like two microscope slides w/ a droplet between

*In-use stiction*: when device surfaces adhere during use due to:
- Capillary condensation
- Electrostatic forces
- Hydrogen bonding
- Van der Waals forces
Hydrophilic Versus Hydrophobic

- **Hydrophilic**:
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle $\theta_{\text{water}} < 90^\circ$

- **Hydrophobic**:
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle $\theta_{\text{water}} > 90^\circ$

Microstructure Stiction

- Thin liquid layer between two solid plates $\Rightarrow$ adhesive
- If the contact angle between liquid and solid $\theta_c < 90^\circ$:
  - Pressure inside the liquid is lower than outside
  - Net attractive force between the plates
- The pressure difference (i.e., force) is given by the Laplace equation
### Microstructure Stiction Modeling

- **Wetted Area**
- **Contact Angle**
- **Liquid Layer Thickness**
- **Force Applied to Maintain Equilibrium**

**Laplace Equation:**
\[ \Delta P_{la} = \frac{\gamma_{lv}}{r} \]

- **Pressure Difference at the Liquid-Air Interface**
- **Meniscus (concave)**

**Force needed to keep the plates apart:**
\[ F = -\Delta P_{la} A = \frac{2\gamma_{lv} \cos \theta_c}{g} \]

- Force means a **Laplace pressure**

### Avoiding Stiction

- **Reduce droplet area via mechanical design approaches**
  - Reduce droplet area via mechanical design approaches
  - Avoid liquid-vapor meniscus formation
    - Use solvents that sublime
    - Use vapor-phase sacrificial layer etch
  - Modify surfaces to change the meniscus shape from concave (small contact angle) to convex (large contact angle)
    - Use teflon-like films
    - Use hydrophobic self-assembled monolayers (SAMs)

- **Standoff Bumps**
- **Meniscus-Shaping Features**
Supercritical CO\textsubscript{2} Drying

- A method for stictionless drying of released microstructures by immersing them in CO\textsubscript{2} at its supercritical point

- **Basic Strategy**: Eliminate surface tension-derived sticking by avoiding a liquid-vapor meniscus

- **Procedure**:
  - Etch oxide in solution of HF
  - Rinse thoroughly in DI water, but do not dry
  - Transfer the wafer from water to methanol
  - Displace methanol with liquid CO\textsubscript{2}
  - Apply heat & pressure to take the CO\textsubscript{2} past its critical point
  - Vent to lower pressure and allow the supercritical CO\textsubscript{2} to revert to gas → liquid-to-gas Xsition in supercritical region means no capillary forces to cause stiction

Hydrophilic Versus Hydrophobic

- **Hydrophilic**:
  - A surface that invites wetting by water
  - Get stiction
  - Occurs when the contact angle $\theta_{\text{water}} < 90^\circ$

- **Hydrophobic**:
  - A surface that repels wetting by water
  - Avoids stiction
  - Occurs when the contact angle $\theta_{\text{water}} > 90^\circ$
Tailoring Contact Angle Via SAM’s

- Can reduce stiction by tailoring surfaces so that they induce a water contact angle > 90°

Self-Assembled Monolayers (SAM’s):
- Monolayers of “stringy” molecules covalently bonded to the surface that then raise the contact angle
- Beneficial characteristics:
  - Conformal, ultrathin
  - Low surface energy
  - Covalent bonding makes them wear resistant
  - Thermally stable (to a point)

<table>
<thead>
<tr>
<th>Material</th>
<th>Water Contact Angle</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODT SAM</td>
<td>112 ± 0.7°</td>
</tr>
<tr>
<td>SiO₂</td>
<td>&lt;10°</td>
</tr>
</tbody>
</table>

Dry Release

- Another way to avoid stiction is to use a dry sacrificial layer etch
- For an oxide sacrificial layer
  - Use HF vapor phase etching
  - Additional advantage: gas can more easily get into tiny gaps
  - Issue: not always completely dry → moisture can still condense → stiction → soln: add alcohol
- For a polymer sacrificial layer
  - Use an O₂ plasma etch (isotropic, so it can undercut well)
  - Issues:
    - Cannot be used when structural material requires high temperature for deposition
    - If all the polymer is not removed, polymer under the suspended structure can still promote stiction
Residual Stress

Residual Stress in Thin Films

- After release, poorly designed microstructures might buckle, bend, or warp → often caused by residual film stress
- Origins of residual stress, \( \sigma \)
  - Growth processes
    - Non-equilibrium deposition
    - Grain morphology change
    - Gas entrapment
    - Doping
  - Thermal stresses
    - Thermal expansion
      - mismatch of materials → introduce stress during cool-down after deposition
    - Annealing

Tunable Dielectric Capacitor
[Yoon, et al., U. Michigan]

Buckled Double-Ended Tuning Fork
Need to Control Film Stress

- Resonance frequency expression for a lateral resonator:

\[
f_0 \approx \frac{1}{2\pi} \sqrt{\frac{4E_y t W^3}{ML^3}} + \frac{24\sigma_s t W}{5ML}
\]

- Since \( W < L \), the stress term will dominate if \( \sigma_s \sim E_y \)

- \( E_y = \) Young's modulus
- \( \sigma_s = \) stress
- \( t = \) thickness
- \( W = \) beam width
- \( L = \) beam length
- \( M = \) mass

Tensile Versus Compressive Stress

- Under tensile stress, a film wants to shrink w/r to its substrate
  - Caused, e.g., by differences in film vs. substrate thermal expansion coefficients
  - If suspended above a substrate and anchored to it at two points, the film will be "stretched" by the substrate

- Under compressive stress, a film wants to expand w/r to its substrate
  - If suspended above a substrate and anchored to it at two points, the film will buckle over the substrate
Vertical Stress Gradients

- Variation of residual stress in the direction of film growth
- Can warp released structures in z-direction

Stress in Polysilicon Films

- Stress depends on crystal structure, which in turn depends upon the deposition temperature
  - Temperature $\leq 600^\circ C$
    - Films are initially amorphous, then crystallize
    - Get equiaxed crystals, largely isotropic
    - Crystals have higher density $\rightarrow$ tensile stress
    - Small stress gradient
  - Temperature $\geq 600^\circ C$
    - Columnar crystals grow during deposition
    - As crystals grow vertically and in-plane they push on neighbors $\rightarrow$ compressive stress
    - Positive stress gradient
### Annealing Out Polysilicon Stress

- Control polySi stress by annealing at high temperatures
  - Typical anneal temperatures: 900-1150°C
  - Grain boundaries move, relax
  - Can dope while annealing by sandwiching the polysilicon between similarly doped oxides (symmetric dopant drive-in), e.g. using 10-15 wt. % PSG

- Rapid thermal anneal (RTA) also effective (surprisingly)

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### Topography Issues

- Degradation of lithographic resolution
  - PR step coverage, streaking

- Stringers
  - Problematic when using anisotropic etching, e.g., RIE
Nickel Surface-Micromachining Process Flow

Electroplating: Metal MEMS

- Use electroplating to obtain metal structures
- When thick: call it “LIGA”
- Pros: fast low temp deposition, very conductive
- Cons: drift, low mech. Q but may be solvable?
Nickel Metal Surface-Micromachining

- Deposit isolation LTO:
  - Target = 2μm
  - 1 hr, 40 min. LPCVD @450°C
- Densify the LTO
  - Anneal @950°C for 30 min.

- Define metal interconnect via lift-off
  - Spin photoresist and pattern lithographically to open areas where interconnect will stay
  - Evaporate a Ti/Au layer
    - Target = 30nm Ti
    - Target = 270nm Au
  - Remove photoresist in PRS2000
  - Electroplate nickel to fill the anchor vias
    - Use solution of nickel sulfamate @ 50°C
    - Time the electroplating to planarize the surface

Nickel Metal Surface-Micromachining

- Evaporate Al to serve as a sacrificial layer
  - Target = 1μm

- Lithography to define anchor openings

- Wet etch the aluminum to form anchor vias
  - Use solution of H₃PO₄/HNO₃/H₂O

- Remove photoresist in PRS2000

- Electroplate nickel to fill the anchor vias
  - Use solution of nickel sulfamate @ 50°C
  - Time the electroplating to planarize the surface
Nickel Metal Surface-Micromachining

- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm²

Nickel Metal Surface-Micromachining

- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant

- Release the structures
  - Use a $K_4Fe(CN)_6/NaOH$ etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au
Nickel Surface-Micromachining Example

*Below:* Surface-micromachined in nickel using the described process flow

3D “Pop-up” MEMS
Pop-Up MEMS

First MEMS hinge
[K. Pister, et al., 1992]

Corner Cube Reflector
[v. Hsu, 1999]

• Pictured: hinged Campanile made in SUMMiT process, assembled using probes [Elliot Hui, et al.]
### 3D Direct-Assembled Tunable L

![Image of a 3D direct-assembled tunable L structure](image)

[Ming Wu, UCLA]

### Hinge Process Flow

- **Deposit first sacrificial**
- **Deposit and pattern first poly**

- **Deposit and pattern second sacrificial**

- **Pattern contacts**
- **Deposit and pattern second poly**

- **Etch sacrificial**
- **Assemble part**

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*EE 247B/ME218: Introduction to MEMS Design*

*Module 5: Surface Micromachining*
"Foundry" MEMS: The MUMPS Process

MUMPS: MultiUser MEMS ProcessS

- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm² dies

Micromotor fabricated via MUMPS
MUMPS: MultiUser MEMS ProcesS

Micromotor Example

<table>
<thead>
<tr>
<th>Material Layer</th>
<th>Thickness (µm)</th>
<th>Lithography Level Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nitride</td>
<td>0.6</td>
<td>--</td>
</tr>
<tr>
<td>Poly 0</td>
<td>0.5</td>
<td>POLY0 (HOLE0)</td>
</tr>
<tr>
<td>First Oxide</td>
<td>2.0</td>
<td>DIMPLE ANCHOR1</td>
</tr>
<tr>
<td>Poly 1</td>
<td>2.0</td>
<td>POLY1 (HOLE1)</td>
</tr>
<tr>
<td>Second Oxide</td>
<td>0.75</td>
<td>POLY1_POLY2_VIA ANCHOR2</td>
</tr>
<tr>
<td>Poly 2</td>
<td>1.5</td>
<td>POLY2 (HOLE2)</td>
</tr>
<tr>
<td>Metal</td>
<td>0.5</td>
<td>METAL (HOLEM)</td>
</tr>
</tbody>
</table>

Masks in polyMUMPS

Minimum set of masks that must be used in MUMPS

<table>
<thead>
<tr>
<th>Mnemonic level name</th>
<th>Field type</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0</td>
<td>light</td>
<td>pattern ground plane</td>
</tr>
<tr>
<td>ANCHOR1</td>
<td>dark</td>
<td>open holes for Poly 1 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>DIMPLE</td>
<td>dark</td>
<td>create dimples/bushings for Poly 1</td>
</tr>
<tr>
<td>POLY1</td>
<td>light</td>
<td>pattern Poly 1</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>dark</td>
<td>open holes for Poly 1 to Poly 2 connection</td>
</tr>
<tr>
<td>ANCHOR2</td>
<td>dark</td>
<td>open holes for Poly 2 to Nitride or Poly 0 connection</td>
</tr>
<tr>
<td>POLY2</td>
<td>light</td>
<td>pattern Poly 2</td>
</tr>
<tr>
<td>METAL</td>
<td>light</td>
<td>pattern Metal</td>
</tr>
<tr>
<td>HOLE0</td>
<td>dark</td>
<td>provide holes for POLY0</td>
</tr>
<tr>
<td>HOLE1</td>
<td>dark</td>
<td>provide release holes for POLY1</td>
</tr>
<tr>
<td>HOLE2</td>
<td>dark</td>
<td>provide release holes for POLY2</td>
</tr>
<tr>
<td>HOLEM</td>
<td>dark</td>
<td>provide release holes in METAL</td>
</tr>
</tbody>
</table>

Field type:
- Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
- Dark field (df): in layout, boxes represent holes to be cut out

Extra masks for more flexibility & ease of release
MUMPS Process Flow

- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 µm of PSG as the 1st sacrificial layer
- Lithography using the DIMPLE(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1 (df) mask (align to poly0)
- RIE anchor vias down to the nitride surface

MUMPS Process Flow (cont.)

- LPCVD 2 µm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  This both dope the polysilicon and reduces its residual stress

- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then ...
- RIE the polysilicon

- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA (df) mask to define contacts to the poly1 layer (align to poly1)
MUMPS Process Flow (cont.)

- Recomb with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings
- LPCVD 1.5 μm undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress
- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask

MUMPS Process Flow (cont.)

- Lithography using the METAL (df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer
- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed
MUMPS: MultiUser MEMS Process

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Micromotor fabricated via MUMPS

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polyMUMPS Minimum Feature Constraints

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

<table>
<thead>
<tr>
<th>Feature Type</th>
<th>Nominal [µm]</th>
<th>Min Feature [µm]</th>
<th>Min Spacing [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0, POLY1, POLY2</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>POLY1_POLY2_VIA</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>ANCHOR1, ANCHOR2</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Dimple</td>
<td>3</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Metal</td>
<td>3</td>
<td>3</td>
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<td>HOLE1, HOLE2</td>
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<td>HOLEM</td>
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### MUMPS Design Rules (cont.)

**Table:**

<table>
<thead>
<tr>
<th>Rule</th>
<th>Rule Letter</th>
<th>Figure #</th>
<th>Min. Value (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY0 space to ANCHOR1</td>
<td>A</td>
<td>2.5</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose ANCHOR1</td>
<td>B</td>
<td>2.5</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose POLY1</td>
<td>C</td>
<td>2.8</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose POLY2</td>
<td>D</td>
<td>2.7</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY0 enclose ANCHOR2</td>
<td>E</td>
<td>2.8</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY0 space to ANCHOR2</td>
<td>F</td>
<td>2.8</td>
<td>5.0</td>
</tr>
</tbody>
</table>

**Cross Sections:**

- Oxide1
- Poly0
- Anchor1

**Mask Levels:**

- Poly0
- Anchor1
- Poly1
- Poly1-Poly2_Via
- Metal
- Dielectric

---

**Table:**

<table>
<thead>
<tr>
<th>Rule</th>
<th>Min. Value (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY1 enclose ANCHOR1</td>
<td>4.0</td>
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<tr>
<td>POLY1 enclose D_MPLE</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY1 enclose POLY1_POLY2_VIA</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY1 enclose POLY2</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY1 space to ANCHOR2</td>
<td>3.0</td>
</tr>
<tr>
<td>&quot;Lateral etch holes in POLY1&quot;</td>
<td>≤30 (max. value)</td>
</tr>
</tbody>
</table>

**Cross Sections:**

- Oxide1
- Poly1
- Anchor1

**Mask Levels:**

- Poly0
- Anchor1
- Poly1
- Poly1-Poly2_Via
- Metal
- Dielectric
MUMPS Design Rules (cont.)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Rule Letter</th>
<th>Figure #</th>
<th>Min. Value (μm)</th>
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<tbody>
<tr>
<td>POLY0 space to ANCHOR1</td>
<td>A</td>
<td>2.5</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY0 enclose ANCHOR1</td>
<td>B</td>
<td>2.6</td>
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<td>POLY0 enclose POLY1</td>
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<td>POLY0 enclose POLY2</td>
<td>D</td>
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<td>5.0</td>
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<td>POLY0 enclose ANCHOR2</td>
<td>E</td>
<td>2.8</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY0 space to ANCHOR2</td>
<td>F</td>
<td>2.8</td>
<td>5.0</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Rule</th>
<th>Rule Letter</th>
<th>Figure #</th>
<th>Min. Value (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY1 enclose ANCHOR1</td>
<td>G</td>
<td>2.6</td>
<td>4.0</td>
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<tr>
<td>POLY1 enclose DIMPLE</td>
<td>N</td>
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<td>POLY1 enclose POLY1_POLY2_VIA</td>
<td>H</td>
<td>2.9-2.11</td>
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<tr>
<td>POLY1 enclose POLY2</td>
<td>O</td>
<td>2.14</td>
<td>4.0</td>
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<tr>
<td>POLY1 space to ANCHOR2</td>
<td>K</td>
<td>2.11</td>
<td>3.0</td>
</tr>
<tr>
<td>*Lateral etch holes space in POLY1</td>
<td>R</td>
<td>2.15</td>
<td>≤30 (max. value)</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Rule</th>
<th>Rule Letter</th>
<th>Figure #</th>
<th>Min. Value (μm)</th>
</tr>
</thead>
<tbody>
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<td>POLY2 enclose ANCHOR2</td>
<td>J</td>
<td>2,7,2.10</td>
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<tr>
<td>POLY2 enclose POLY1_POLY2_VIA</td>
<td>L</td>
<td>2.9</td>
<td>4.0</td>
</tr>
<tr>
<td>POLY2 cut-in POLY1</td>
<td>P</td>
<td>2.14</td>
<td>5.0</td>
</tr>
<tr>
<td>POLY2 cut-out POLY1</td>
<td>Q</td>
<td>2.14</td>
<td>4.0</td>
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<tr>
<td>POLY2 enclose METAL</td>
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<td>2.10</td>
<td>3.0</td>
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<td>HOLE2 enclose HOLE1</td>
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<tr>
<td>HOLE2 enclose HOLE2</td>
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<td>S</td>
<td>2.15</td>
<td>≤30 (max. value)</td>
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</tbody>
</table>

**Table 2.7** PolyMUMP's design rule reference sheet. Table shows minimum dimensions (μm), rule name, and figure number, respectively.
The Sandia SUMMIT Process

Sandia’s SUMMiT V

• SUMMiT V: “Sandia Ultra-planar Multi-level MEMS Technology 5” fabrication process
  ▪ Five-layer polysilicon surface micromachining process
  ▪ One electrical interconnect layer & 4 mechanical layers
  ▪ Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  ▪ 14 masks
SUMMiT V Layer Stack

- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized

Chemical Mechanical Polishing (CMP)

- Used to planarize the top surface of a semiconductor wafer or other substrate
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad
  - Wafer and pad are pressed together
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing
**CMP: Not the Same as Lapping**

**Lapping**
- Lapping is merely the removal of material to flatten a surface without selectivity
- Everything is removed at approximately the same rate

**Chemical Mechanical Polishing (CMP)**
- CMP is selective to certain films, and not selective to others

**Actual SUMMiT Cross-Section**

- No CMP until after the first three polySi layers
- 1 µm mmpoly1 and 1.5 µm mmpoly2 can be combined to form a 2.5 µm polysilicon film
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions