Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - Bulk Micromachining
  - Anisotropic Etching of Silicon
  - Boron-Doped Etch Stop
  - Electrochemical Etch Stop
  - Isotropic Etching of Silicon
  - Deep Reactive Ion Etching (DRIE)
  - Wafer Bonding

Bulk Micromachining

- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - Isotropic vs. anisotropic
  - Reaction-limited
    - Etch rate dep. on temp.
  - Diffusion-limited
    - Etch rate dep. on mixing
    - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - Desired shape
  - Etch depth and uniformity
  - Surface roughness (e.g., sidewall roughness after etching)
  - Process compatibility (w/ existing layers)
  - Safety, cost, availability, environmental impact

Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm²)
  - Young's Modulus near that of stainless steel
  - \{100\} = 130 GPa; \{110\} = 169 GPa; \{111\} = 188 GPa
  - Mechanical properties uniform, no intrinsic stress
  - Mechanical integrity up to 500°C
  - Good thermal conductor
  - Low thermal expansion coefficient
  - High piezoresistivity
Anisotropic Wet Etching

Anisotropic etches are available for single crystal Si:

- Orientation-dependent etching: <111>-plane more densely packed than <100>-plane
  - Slower E.R.
  - Faster E.R.

One such solvent: KOH + isopropyl alcohol
(e.g., 23.4 wt% KOH, 13.3 wt% isopropyl alcohol, 63 wt% H₂O)

\[ \text{E.R.}_{<100>} = 100 \times \text{E.R.}_{<111>} \]

Anisotropic Wet Etching (cont.)

Can get the following:

- (on a <100>-wafer)
  - Si
  - SiO₂

- (on a <110>-wafer)

Anisotropic Etching of Silicon

- Etching of Si w/ KOH
  \[ \text{Si} + 2\text{OH}^- \rightarrow \text{Si(OH)}_2^{2-} + 4\text{e}^- \]
  \[ 4\text{H}_2\text{O} + 4\text{e}^- \rightarrow 4(\text{OH})^- + 2\text{H}_2 \]
- Crystal orientation dependent etch rates
  \{110\}:\{100\}:\{111\}=600:400:1
- {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
- {111} plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
- {111} forms protective oxide
- {111} smoother than other crystal planes → good for optical MEMS (mirrors)

Self-limiting etches

- Membrane
- Front side mask
- Back side mask

Anisotropic Wet Etching of Silicon (cont.)

- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - RIE using SF₆
  - Remove PR in PRS2000
- Etch the silicon
  - Use 1:2 KOH:H₂O (wt.), stirred bath @80°C
  - Etch Rates:
    - (100) Si → 1.4 μm/min
    - Si₃N₄ → ~0 nm/min
    - SiO₂ → 1-10 nm/min
    - Photoresist, Al → fast
- Micromasking by H₂ bubbles leads to roughness
  - Stir well to displace bubbles
  - Can also use oxidizer for (111) surfaces
  - Or surfactant additives to suppress bubble formation
Silicon Wafers

{110} plane
(100) planes
(100) plane
45°

{100} primary flat

{100} type wafer

Determining Angles Between Planes

* The angle between vectors \([abc]\) and \([xyz]\) is given by:

\[
ax + by + cz = \left(\frac{a}{x}, \frac{b}{y}, \frac{c}{z}\right) \cdot \left(\frac{x}{x}, \frac{y}{y}, \frac{z}{z}\right) = \cos \theta \\
\theta_{(a,b,c)}(x,y,z) = \cos^{-1} \left[ \frac{ax + by + cz}{\sqrt{a^2 + b^2 + c^2} \sqrt{x^2 + y^2 + z^2}} \right]
\]

* For \{100\} and \{110\} \(\rightarrow 45°\)
* For \{100\} and \{111\} \(\rightarrow 54.74°\)
* For \{110\} and \{111\} \(\rightarrow 35.26°, 90°, \text{ and } 144.74°\)

Silicon Crystallography

Miller Indices \((h k l)\):

* Planes
  * Reciprocal of plane intercepts with axes
  * e.g., for \{110\}, intercepts: \((x,y,z) = (1,1,\infty)\); reciprocals: \((1,1,0) \rightarrow \{110\}\)
  * \(\text{unique}, \{\text{family}\}\)

* Directions
  * One endpoint of vector \(@\) origin
  * \(\text{unique}, <\text{family}>\)

Silicon Crystal Origami

* Silicon fold-up cube
* Adapted from Profs. Kris Pister and Jack Judy
* Print onto transparency
* Assemble inside out
* Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]
Undercutting Via Anisotropic Si Etching

* Concave corners bounded by \{111\} are not attacked
* ... but convex corners bounded by \{111\} are attacked
  - Two \{111\} planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
  - Result: can undercut regions around convex corners

[Ristic]

Corner Compensation

* Protect corners with “compensation” areas in layout
* Below: Mesa array for self-assembly structures [Smith 1995]

Other Anisotropic Silicon Etchants

* TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - Etch rate (100) = 0.5-1.5 μm/min
  - Attacks Al
    - Si-doped Al safe & IC compatible
  - Etch ratio (100)/(111) = 10-35
  - Etch masks: SiO₂, Si₃N₄ ~ 0.05-0.25 nm/min
  - Boron doped etch stop, up to 40× slower

* EDP (115°C)
  - Carcinogenic, corrosive
  - Etch rate (100) = 0.75 μm/min
  - Al may be etched
  - R(100) > R(110) > R(111)
  - Etch ratio (100)/(111) = 35
  - Etch masks: SiO₂ ~ 0.2 nm/min, Si₃N₄ ~ 0.1 nm/min
  - Boron doped etch stop, 50× slower
**Boron-Doped Etch Stop**

- Control etch depth precisely with boron doping (p++)
- $[B] > 10^{20}$ cm$^{-3}$ reduces KOH etch rate by 20-100x
- Can use gaseous or solid boron diffusion
- Recall etch chemistry:
  \[ \text{Si} + 2\text{OH}^- \rightarrow \text{Si(OH)}_2^{2+} + 4e^- \]
  \[ 4\text{H}_2\text{O} + 4e^- \rightarrow 4\text{(OH)}^{	ext{-}} + 2\text{H}_2 \]
- At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH$^{-}$.  
- Result:
  - Beams, suspended films
  - 1-20 μm layers possible

**Ex: Micronozzle**

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

**Ex: Microneedle**

- Below: micro-neurostimulator
  - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan

**Ex: Microneedles (cont.)**

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400 μm site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system
Electrochemical Etch Stop

* When silicon is biased with a sufficiently large anodic potential relative to the etchant, it will oxidize (i.e., electrochemical passivation), which then prevents etching.
* For passivation to occur, current flow is required.
* If current flow can be prevented, there will be no oxide growth, and etching can proceed.

**Can prevent current flow by adding a reverse-biased diode structure**

**Electrochemical Etch Stop**

- *n*-type epitaxial layer grown on *p*-type wafer forms *p*-*n* diode
  - \( V_p > V_n \rightarrow \text{electrical conduction (current flow)} \)
  - \( V_p < V_n \rightarrow \text{reverse bias current (very little current flow)} \)

**Passivation potential**: potential at which thin \( \text{SiO}_2 \) film forms.
  - Different for *p*-Si and *n*-Si, but basically need the Si to be the anode in an electrolytic setup.

**Setup**:
  - *p*-*n* diode in reverse bias
  - *p*-substrate floating → etched
  - *n*-layer above passivation potential → not etched

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**Electrochemical Etching of CMOS**

- *N*-type Si well with circuits suspended from \( \text{SiO}_2 \) support beam
- Thermally and electrically isolated
- If use TMAH etchant, doped (w/Si) Al bond pads safe

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Ex: Bulk Micromachined Pressure Sensors

- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection < 1 μm

Deep Reactive-Ion Etching (DRIE)

The Bosch process:
- Inductively-coupled plasma
- Etch Rate: 1.5-4 μm/min
- Two main cycles in the etch:
  - Etch cycle (5-15 s): SF₆ (SF₆⁻) etches Si
  - Deposition cycle (5-15 s): C₄F₈ deposits fluorocarbon protective polymer (CF₂)ₐ
- Etch mask selectivity:
  - SiO₂ ~ 200:1
  - Photoresist ~ 100:1
- Issue: finite sidewall roughness
  - scalloping < 50 nm
- Sidewall angle: 90° ± 2°

DRIE Issues: Etch Rate Variance

- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

Ex: Pressure Sensors

- Below: catheter tip pressure sensor [Lucas NovaSensor]
  - Only 150×400×900 μm³

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**DRIE Issues: “Footing”**

- **Etch depth precision**
  - Etch stop: buried layer of SiO₂
  - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO₂

- **Problem:** Lateral undercut at Si/SiO₂ interface → “footing”
  - Caused by charge accumulation at the insulator

Charging-induced potential perturbs the E-field
- Distorts the ion trajectory
- Result: strong and localized damage to the structure at Si-SiO₂ interface → “footing”

**Poor charge relaxation and lack of neutralization by e⁻’s at insulator**
- Ion flux into substrate builds up (+) potential

**Recipe-Based Suppression of “Footing”**

- **Use higher process pressure** to reduce ion charging [Nazawa]
  - High operating pressure → concentration of (-) charge increases and can neutralize (+) surface charge
  - **Issue:** must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching

- **Adjust etch recipe** to reduce overetching [Schmidt]
  - Change C₄F₈ flow rate, pressure, etc., to enhance passivation and reduce overetching
  - **Issue:** Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches

- **Use lower frequency plasma** to avoid surface charging [Morioka]
  - Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - **Allows e⁻’s to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench**

**Metal Interlayer to Prevent “Footing”**

- Pre-defined metal interlayer grounded to substrate supplies e⁻’s to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

- **Below:** DRIE footing over an oxide stop layer
- **Right:** efficacy of the metal interlayer footing prevention approach

**Footing Prevention (cont.)**

- No metal interlayer
  - With metal interlayer
**DRIE Examples**

- High aspect-ratio gear
- Tunable Capacitor
- Microgripper

**Vapor Phase Etching of Silicon**

- **Vapor phase Xenon Difluoride (XeF₂)**
  \[ 2\text{XeF}_2(g) + \text{Si}(s) \rightarrow 2\text{Xe}(g) + \text{SiF}_4(g) \]
- **Set-up:**
  - Xe sublimes at room T
  - Closed chamber, 1-4 Torr
  - Pulsed to control exothermic heat of reaction
- **Etch rate:** 1-3 \( \mu \text{m/min} \), isotropic
- **Etch masks:** photoresist, \( \text{SiO}_2 \), \( \text{Si}_3\text{N}_4 \), Al, other metals
- **Issues:**
  - Etched surfaces have granular structure, 10 \( \mu \text{m} \) roughness
  - Hazard: \( \text{XeF}_2 \) reacts with \( \text{H}_2\text{O} \) in air to form Xe and HF

**Laser-Assisted Chemical Etching**

- Laser creates Cl radicals from
  \[ \text{Cl}_2 \rightarrow \text{reaction forms SiCl}_2 \]
- **Etch rate:** 100,000 \( \mu \text{m}^3/\text{s} \)
  - Takes 3 min. to etch
  - 500x500x125 \( \mu \text{m}^3 \) trench
- **Surface roughness:** 30 nm rms
- **Serial process:** patterned directly from CAD file

- **At right:**
  - Laser assisted etching of a 500x500 \( \mu \text{m}^2 \) terraced silicon well
  - Each step is 6 \( \mu \text{m} \)-deep