Wide output range power supply

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I Introduction - specifications

II $D^2$ dependant circuits

III Flyback
Goal / Constraints of the project

Offline power supply.

Constraints:
- cheap
- wide output range

application:
Power supply compatible with a wide range of devices

good point:
power loss is not a big issue for offline applications, it is just limited by the heat that the box can dissipate.
# Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Input Voltage</td>
<td>260 V – 390 V</td>
</tr>
<tr>
<td>Max Power</td>
<td>50 W</td>
</tr>
<tr>
<td>Output Current Limit</td>
<td>10 A</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>2.5 V – 30 V</td>
</tr>
<tr>
<td>Output Ripple Ratio (I and V)</td>
<td>±15%</td>
</tr>
<tr>
<td>PWM Frequency</td>
<td>200 kHz</td>
</tr>
</tbody>
</table>

\[
\Delta I = \frac{(D - 1) \cdot V_{out}}{L} \cdot \frac{1}{f}
\]

We want to limit L to 1mH
\[\Rightarrow f = 200 \text{ kHz}\]
Exploring the different topologies

Assumption:
Minimizing the range in which D varies will help us to reduce power dissipation.
# Introduction

- Specifications

## D² dependant circuits

<table>
<thead>
<tr>
<th>( D^2 )</th>
<th>( 0.010 &lt; D &lt; 0.35 )</th>
<th>( \frac{D^2}{D-1} )</th>
<th>( 0.010 &lt; D &lt; 0.30 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.26 &lt; D &lt; 0.93 with N=7</td>
<td>0.36 &lt; D &lt; 0.77 with N=20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Diagrams

1. **D² dependant circuits**
   - Circuit diagram with components labeled.

2. **Flyback circuits**
   - Circuit diagram with components labeled.
**D² dependant circuits**

**Flyback**

**Buck**

- **Vg**
- **L1**
- **C2**
- **L2**
- **C1**
D² dependant circuits - power dissipation

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor</td>
<td>25 W (23 W switching)</td>
</tr>
<tr>
<td>Diodes</td>
<td>6 W</td>
</tr>
<tr>
<td>Transformer</td>
<td>40 W</td>
</tr>
<tr>
<td>Inductors</td>
<td>2 W</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Neglectable</td>
</tr>
</tbody>
</table>

**Transistor**

\[ P_{\text{diss}} = t_{\text{sw}} \cdot V_{\text{ds}} \cdot I_{\text{sw}} \cdot f \]

\[ + \frac{C_{\text{gd}} \cdot V_{\text{ds}}^2 \cdot f}{2} \]

**Transformer**

\[ P_{\text{diss}} = \frac{1}{2} \cdot L_{\text{mag}} \cdot I^2 \cdot f \]

**Diodes**

\[ P_{\text{diss}} = V_{\text{drop}} \cdot I \]
Metrics of Comparison

Assume:
- ↑ Cost follows ↑ power dissipation
- ↑ Package and component size
- ↑ Cost follows ↑ switch stress

Why Flyback?
- Small parts count, single transistor
  - Cheap!
- DC isolation
- DCM operation for low power application
Switch Utilization

- Switch stress: \( S = \hat{V} \hat{I} \)
- Switch utilization: \( U(D) = \frac{P_{\text{load}}}{\sum S} \)

Starting Methodology

- Center D variation around max \( U(D) \)
- Bias voltage associated with max \( U(D) \) towards lower end of output range

Governing formula:
\[
U(D) = (1 - D) \sqrt{D}
\]

Maximum \( U(D) \) at \( D = 0.385 \)

Flyback converter switch utilization vs. duty cycle
Flyback converter

Governing equations:
\[
\frac{V_{out}}{V_{in}} = \frac{n \times D}{(1 - D)}
\]
\[
\frac{I_{out}}{I_{in}} = \frac{(1 - D)}{n}
\]

Introduction - specifications

D^2 dependant circuits

Flyback
### Implementation 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>.049 (20 turns on primary side)</td>
</tr>
<tr>
<td>D range</td>
<td>.12 - .70</td>
</tr>
<tr>
<td>U(D) range</td>
<td>.305 (low D) - .251 (high D)</td>
</tr>
<tr>
<td>Transistor stress</td>
<td>$I_{\text{MAX}} = 681 \text{mA}, V_{\text{MAX}} = 990 \text{V}$, $S = 675 \text{W}$</td>
</tr>
<tr>
<td>Diode Stress</td>
<td>$I_{\text{MAX}} = 23.9 \text{A}, V_{\text{MAX}} = 49.1 \text{V}$, $S = 1173 \text{W}$</td>
</tr>
<tr>
<td>Required Inductance</td>
<td>4.73 mH</td>
</tr>
</tbody>
</table>

**High $V_{\text{MAX}}$**:

- Look at flyback input
  - Transistor must block “stacked” voltage
  
  $V_{\text{in}} + V_{\text{out}} / n$

**Conclusions**:

- Look at “n” equation
  - N proportional to $V_{D,\text{opt}}$
  - To decrease transistor blocking voltage, increase $V_{D,\text{opt}}$ and n.
Implementation 2

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>0.075 (13 turns on primary side)</td>
</tr>
<tr>
<td>D range</td>
<td>0.079 - 0.606</td>
</tr>
<tr>
<td>U(D) range</td>
<td>0.260 (low D) - 0.306 (high D)</td>
</tr>
<tr>
<td>Transistor stress</td>
<td>$I_{\text{MAX}} = 942\text{mA}, V_{\text{MAX}} = 790\text{V}$, $S = 744\text{W}$</td>
</tr>
<tr>
<td>Diode Stress</td>
<td>$I_{\text{MAX}} = 22.56\text{A}, V_{\text{MAX}} = 63.8\text{V}$, $S = 1438\text{W}$</td>
</tr>
<tr>
<td>Required Inductance</td>
<td>3.24 mH</td>
</tr>
<tr>
<td>Overall max power dissipation</td>
<td>43.0 W</td>
</tr>
</tbody>
</table>

Conclusions:

- Sacrificing $\mathcal{S}$ in favor of reducing peak transistor voltage advantageous
  - Smaller, cheaper device with lower loss
  - U(D) just a general metric, not an end in itself

How to further push down peak transistor voltage and power dissipation?

- Cannot reduce $D_{\text{MIN}}$ too far, too much current stress
- Try to reduce $\mathcal{D}$...
Multiple secondary windings

- Each winding will supply a portion of total output range
- Will reduce $\Delta D$, but will require switching between windings

Questions:
- How to divide output range among secondary windings?
- How to optimize number of secondary windings?
Optimizing ranges

- Will minimize $\Delta D$ if:
  
  $$\Delta \frac{M(D)}{n} = \text{Constant}$$

- If output range divided equally, low secondary has largest $\Delta D$

Constant $\Delta$ \{  

Advantages

- $\Delta D$ equal for all ranges
  - $U(D)$ held closer to optimum
  - Reduce peak transistor voltage

Disadvantage

- Look at transformer inductance required for current ripple versus $D^o$
# Implementation 3

<table>
<thead>
<tr>
<th>Range</th>
<th>Voltage Range</th>
<th>( n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( 2.5V &lt; V_{out} &lt; 5.5V )</td>
<td>0.027</td>
</tr>
<tr>
<td>2</td>
<td>( 5.5V &lt; V_{out} &lt; 12.5V )</td>
<td>0.061</td>
</tr>
<tr>
<td>3</td>
<td>( 12.5V &lt; V_{out} &lt; 30.0V )</td>
<td>0.147</td>
</tr>
</tbody>
</table>

**D range**

\[0.179 < D < 0.440\]

**U(D) range**

\[0.347 \text{ (low D)} < U(D) < 0.371 \text{ (high D)}\]

**Transistor stress**

\[I_{\text{MAX}} = 780 \text{mA}, \quad V_{\text{MAX}} = 595 \text{V}, \quad S = 464 \text{ W}\]

**Diode Stress**

\[I_{\text{MAX}} = 27.1 \text{A}, \quad V_{\text{MAX}} = 87.3 \text{V}, \quad S = 2366 \text{ W}\]

**Required Inductance**

\[8.14 \text{ mH}\]

**Overall max power dissipation**

\[23.8 \text{ W}\]

* Using single diode and capacitor at output high diode stress

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**Diagram:**

- **Pdiss** axis: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
- **M(D) / n** axis: 0, 0.2, 0.5, 1, 1.2, 1.5, 1.7, 2, 2.2, 2.5, 2.7, 3, 3.2, 3.5

- Graph showing relationship between \( P_{\text{diss}} \) and \( M(D) / n \).
Switches on DC side

- Advantages:
  - Smaller diodes required
  - Cheaper
  - Less power lost per diode

- Disadvantages:
  - Multiple diodes and output capacitors
  - Possible problem with unloaded output

Switches on transformer side

- Advantages:
  - Single diode and output capacitor required
  - Output “never” unloaded

- Disadvantages:
  - Large required diode
  - Switches must block AC voltage