

EE 290D: Advanced Topics in Semiconductors

- *3-D Transistor Technologies***

Dr. Nuo Xu
EECS Department, UC Berkeley

Administrative

1. Course Focus

2. Course Webpage

<http://www-inst.eecs.berkeley.edu/~ee290d/fa13/>

3. Office Hours (TBD)

4. Course Prerequisites

EE 130, EE 105

5. References

Primarily based on lecture notes

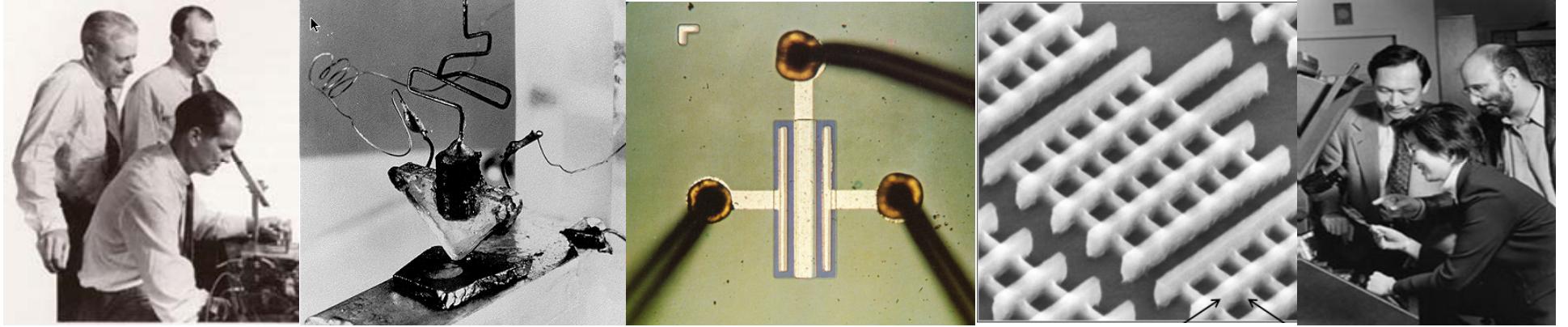
No required texts

6. Grading

HW (30%): 3 assignments

Midterm Exam (40%): Take-home, 48 hrs

Project/Presentation (30%)



Lecture 1

- Course Overview
 - Concepts of Thin-Body MOSFETs
 - History of FinFET Development

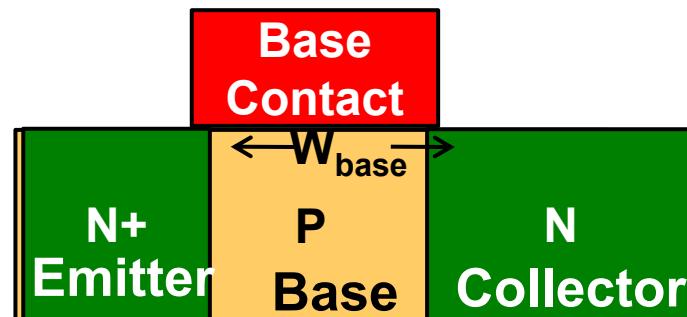
Reading: multiple research articles (reference list at the end of this lecture)

A Journey Back through Time...

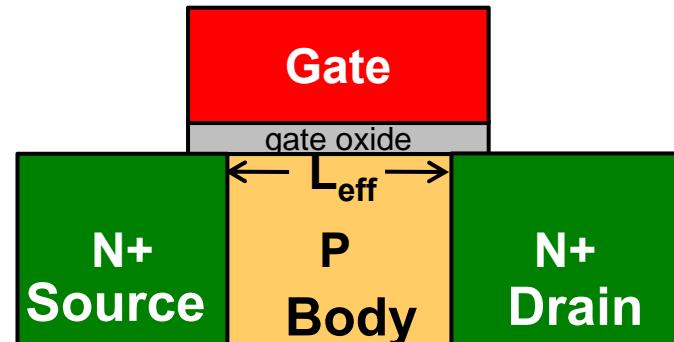
***Notice of Courtesy:
Lots of materials here are from Prof. Tsu-Jae King Liu's
various talks on advanced CMOS devices***

1950s: Diffusive Transistors

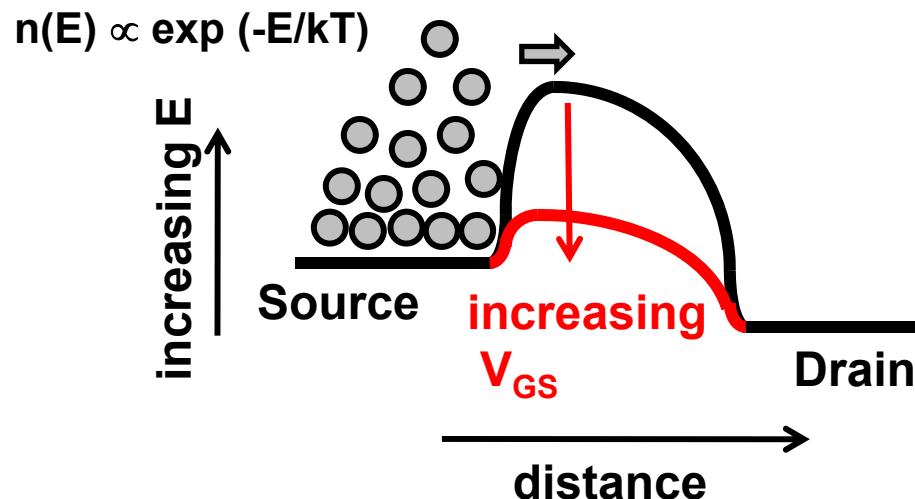
1947: Bipolar Junction Transistor



1959: Metal-Oxide-Semiconductor Field Effect Transistor

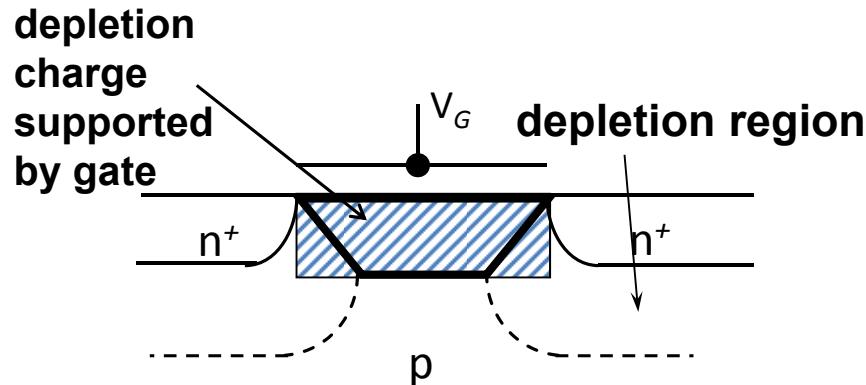


Electron Energy Band Profile

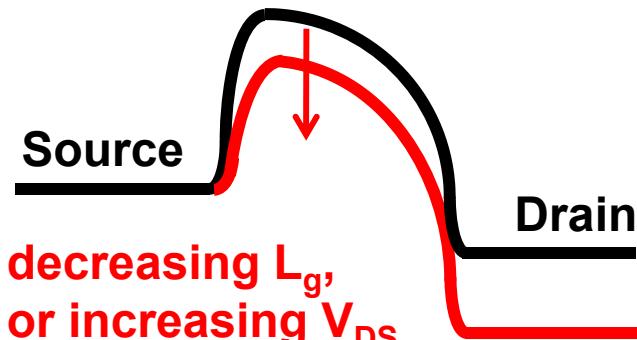


1990s: Short L_g MOSFET Effects

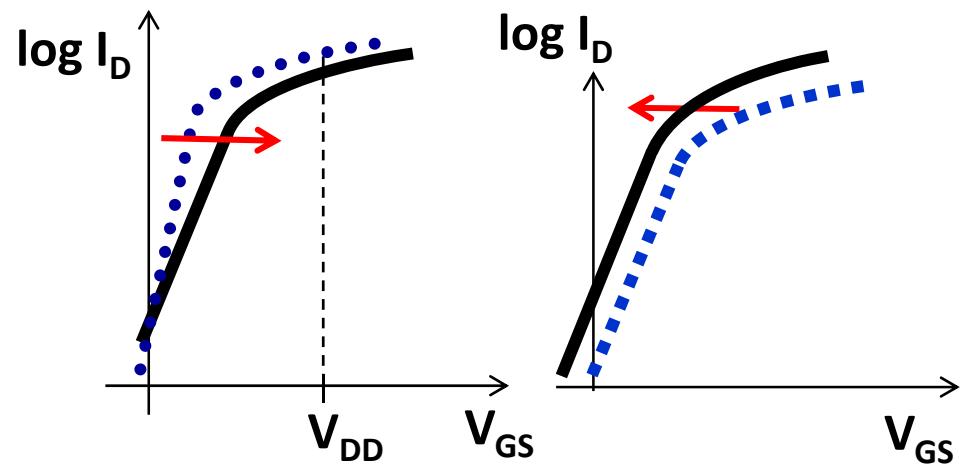
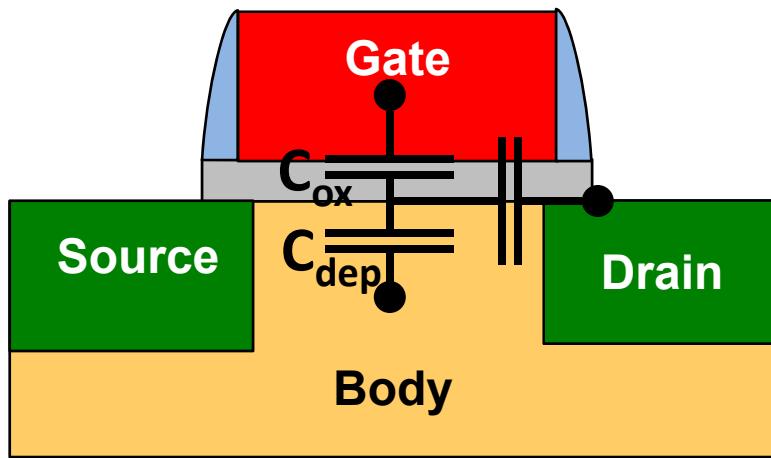
Short Channel Effects



Drain Induced Barrier Lowering

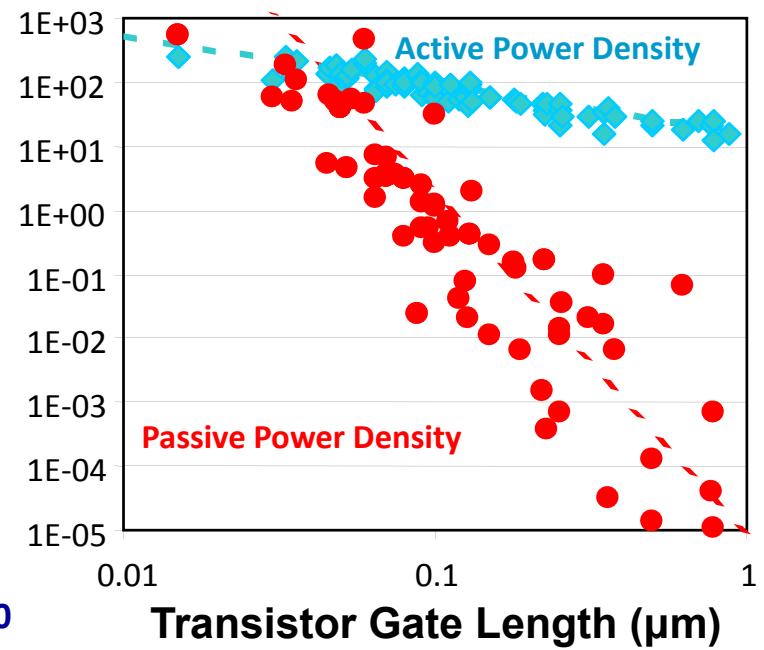
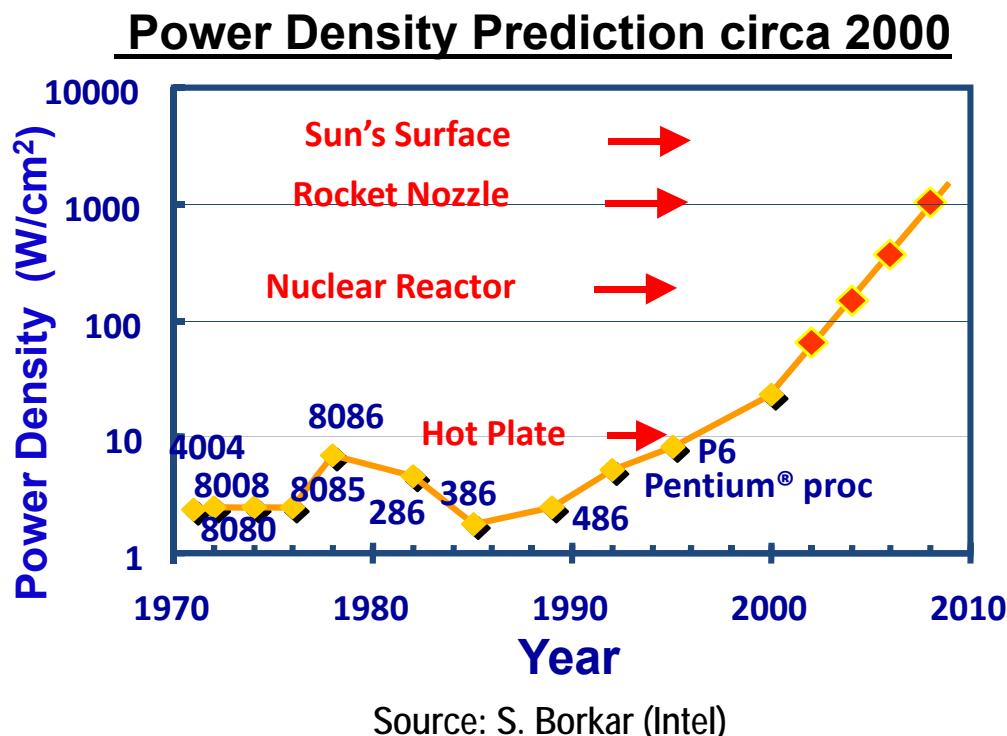


Sub-threshold Swing Degradation



2000s: The IC Power Crisis

- As transistor density has increased, the transistor operating voltage has not decreased proportionately.
→ Power density now constrains chip design!



- Transistor innovations are needed to alleviate this crisis.

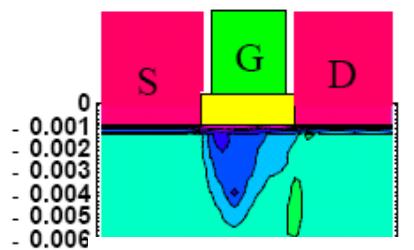
Impact of Body Thickness

- TCAD Simulation results

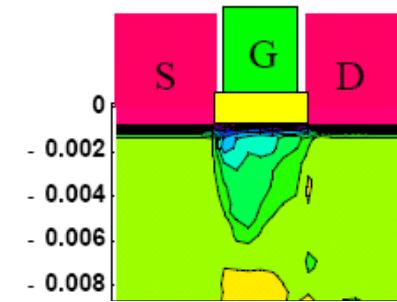
Courtesy of Prof. C. Hu

$V_{gs}=0V$, $V_{ds}=0.7V$
 $L_g=18nm$, $Tox=1.5nm$

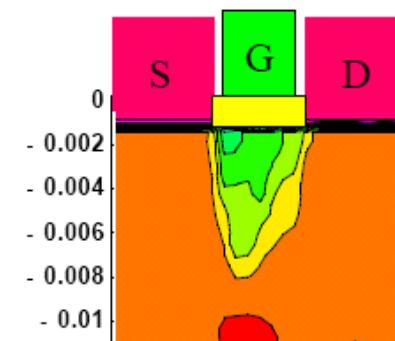
A/cm^2
 10^{-1} 10^2 10^6



$T_{si}=5\text{nm}$



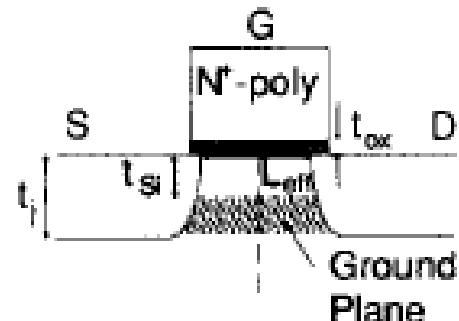
$T_{si}=7.5\text{nm}$



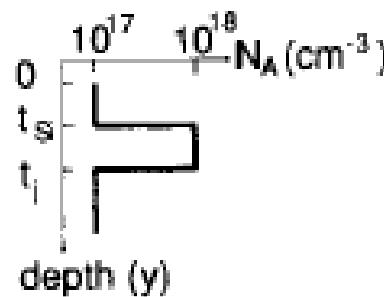
$T_{si}=10\text{nm}$

Thin body – 1000x lower leakage current !!!

Planar MOSFET Scaling Technique: Retrograde Well Doping

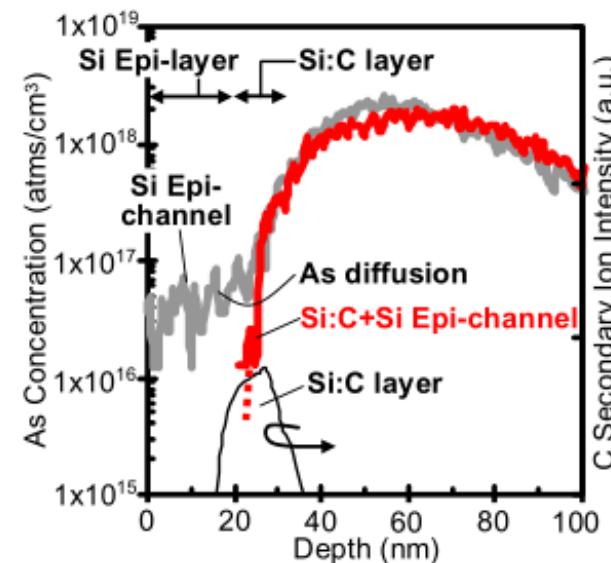


(a)



(b)

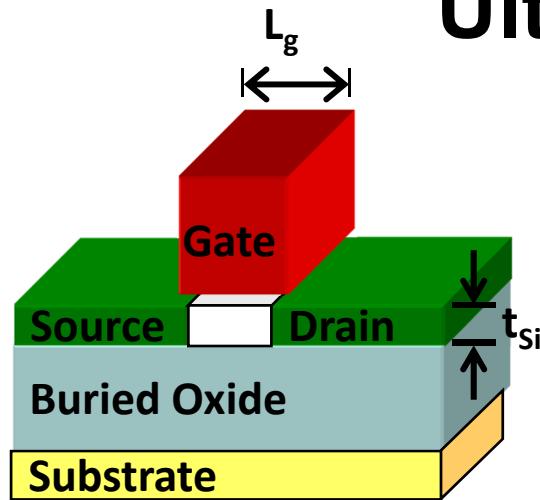
R.-H. Yan, T-ED(1992)



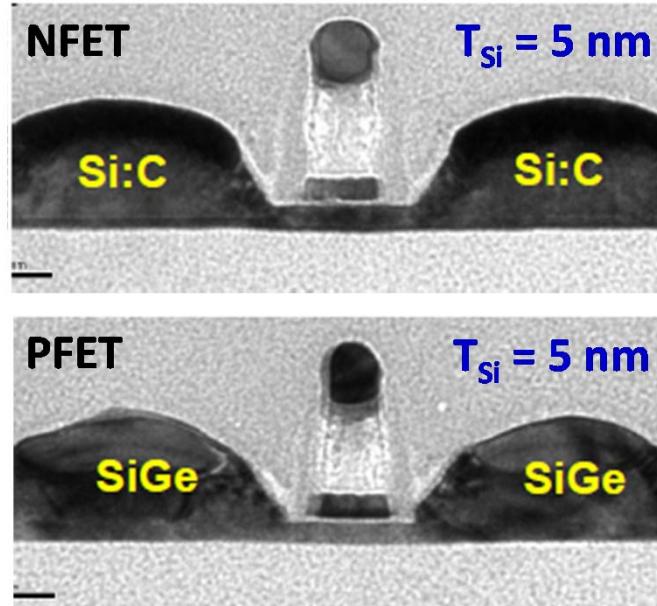
A. Hokazono, VLSI-T(2008) & IEDM(2009)

- Use high doping to “turn off” the sub-channel leakage path.
- Channel is kept undoped, ideally.
- Steep retrograde doping gradient is a limiting factor.
 - Exotic materials have to be used (Si:C, Si:N, etc.) as a screen layer

Planar MOSFET Scaling Technique: Ultra-Thin-Body SOI



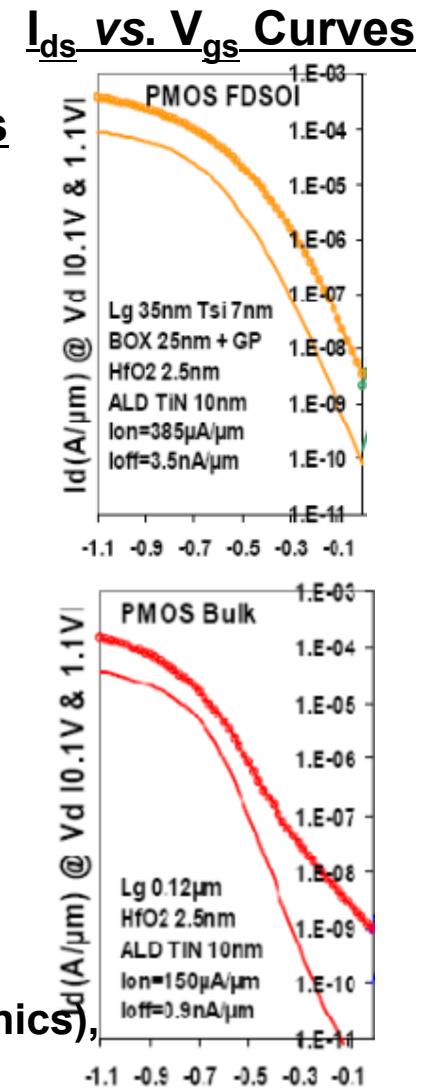
IBM's 20 nm UTB-SOI MOSFETs



- “Remove” the MOSFET substrate by fabricating it on the SOI wafer.
- No channel doping.
- Channel and BOX thicknesses are knobs to tune the device electrostatics.

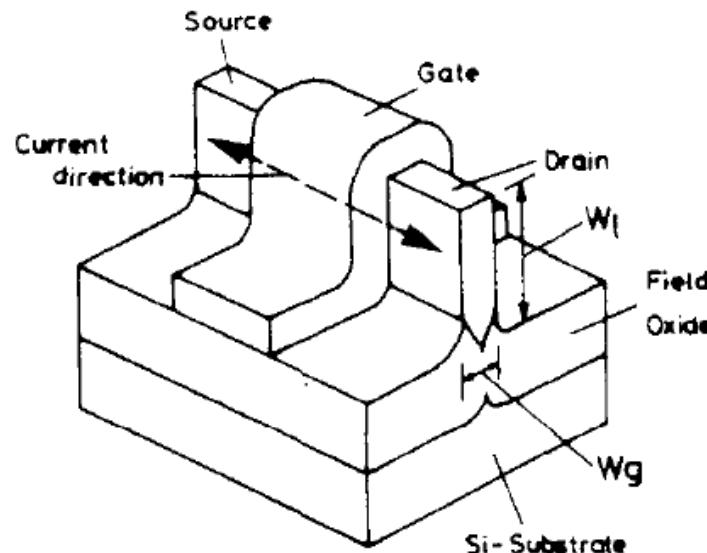
K. Cheng (IBM), IEDM(2009)

C. Fenouillet
(STMicroelectronics),
IEDM(2009)



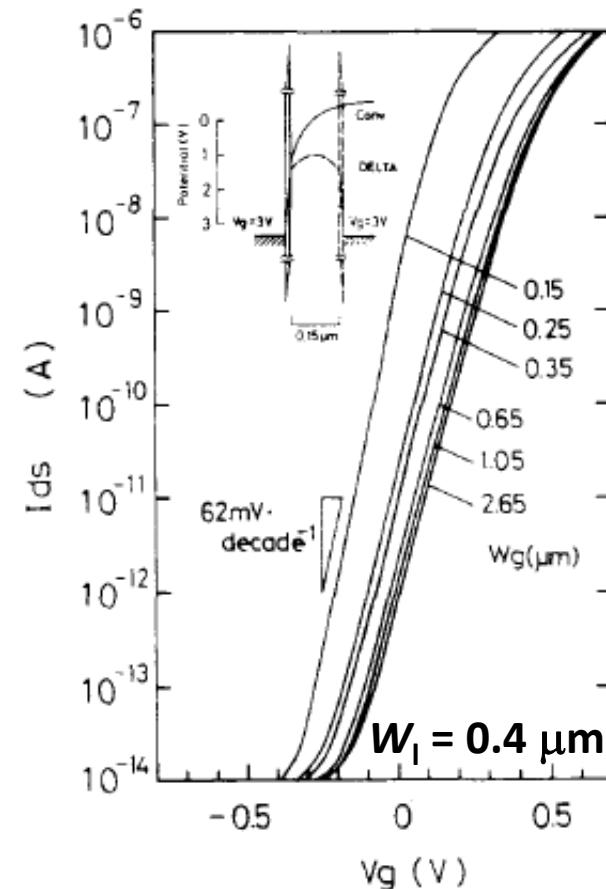
1990: Delta MOSFET

(Hitachi Central Research Laboratory)



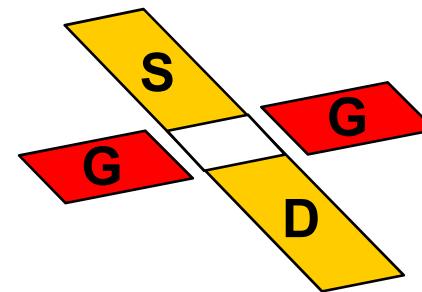
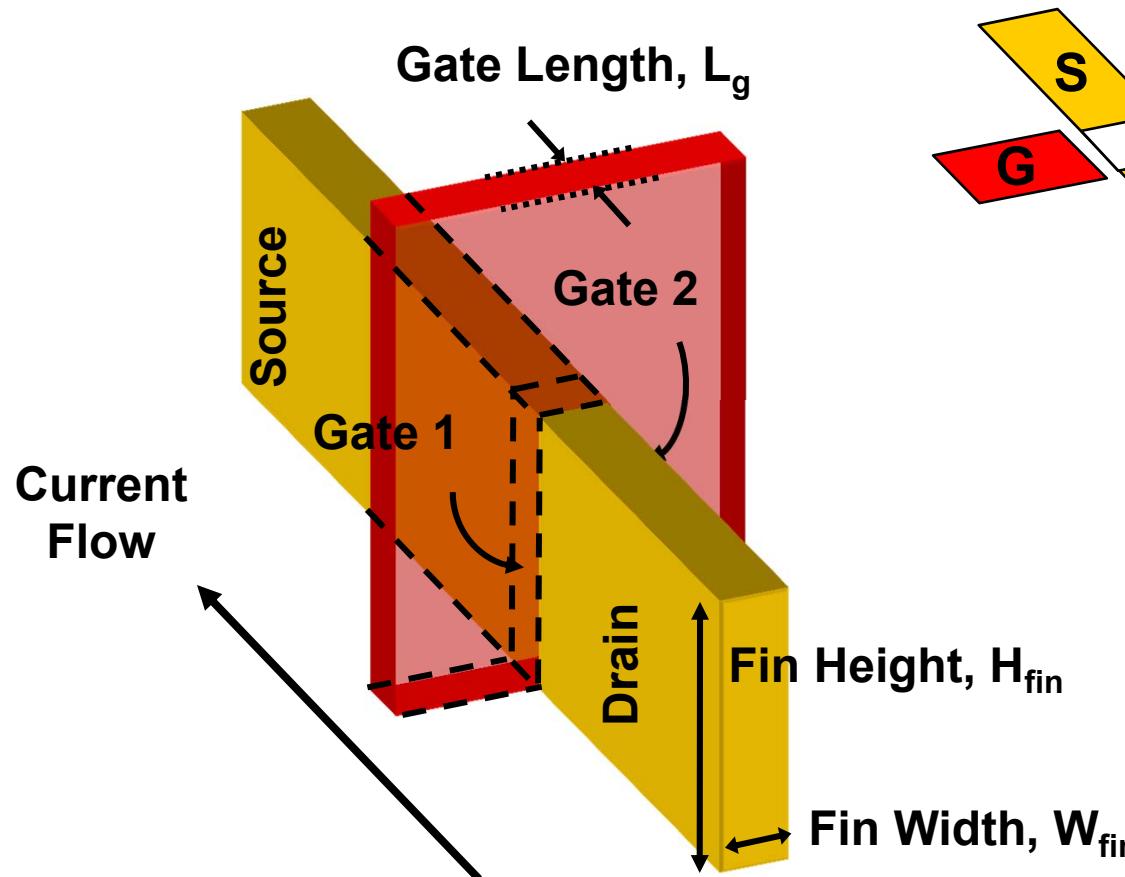
D. Hisamoto, EDL(1990)

- Improved gate control observed for $W_g < 0.3 \mu\text{m}$
 - $L_{\text{eff}} = 0.57 \mu\text{m}$

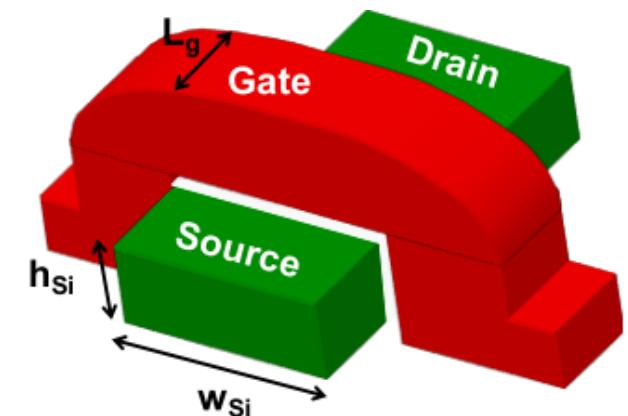


FinFET Concepts

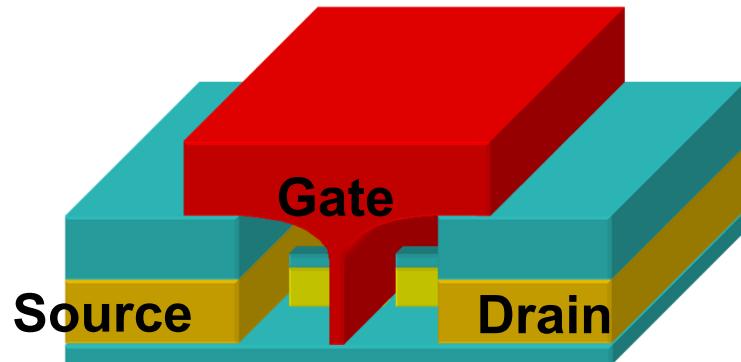
- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface



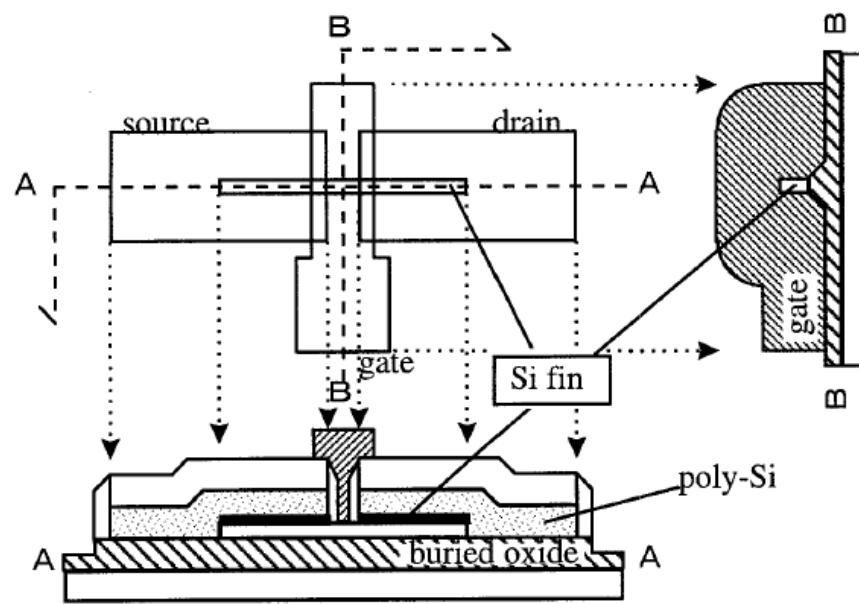
Design Variations



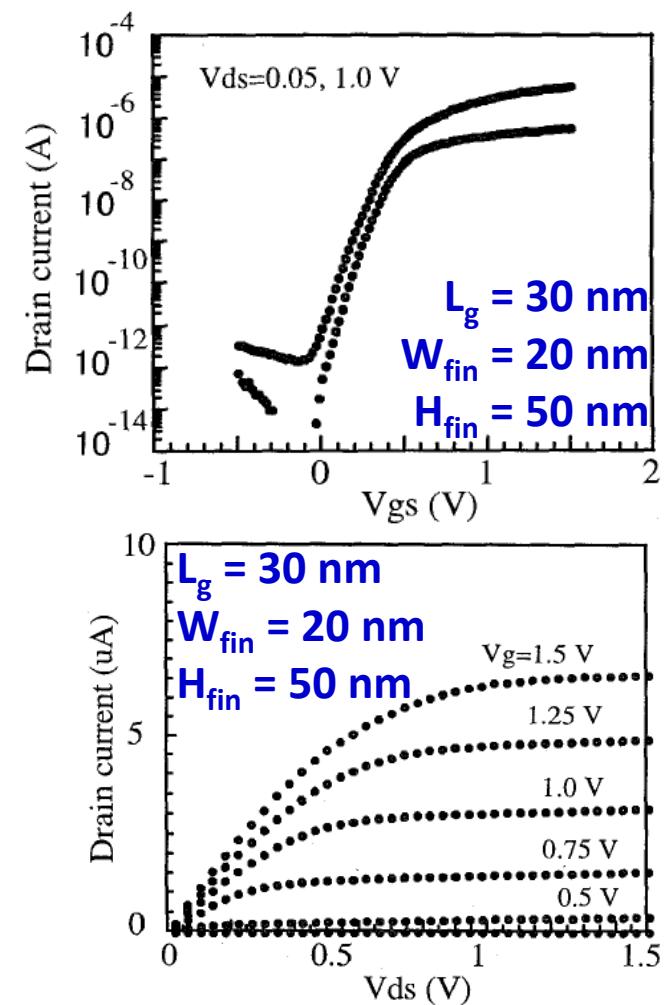
1998: 1st N-Channel FinFET (UC Berkeley)



- Gate-last flow was used originally.



D. Hisamoto, IEDM(1998)



1999: 1st P-Channel FinFET (UC Berkeley)

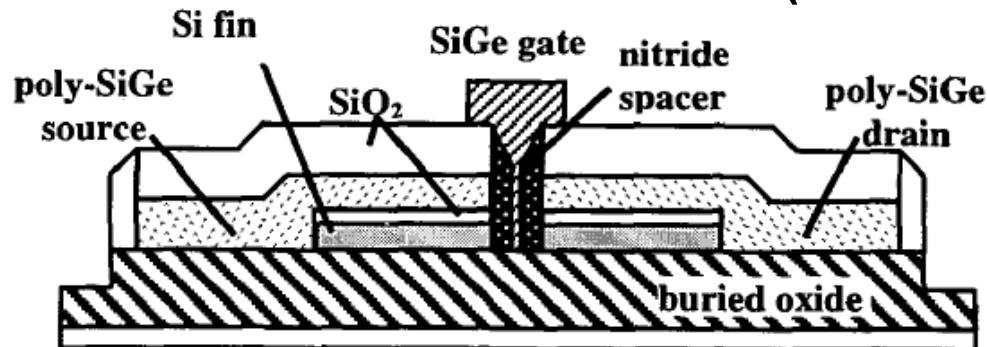
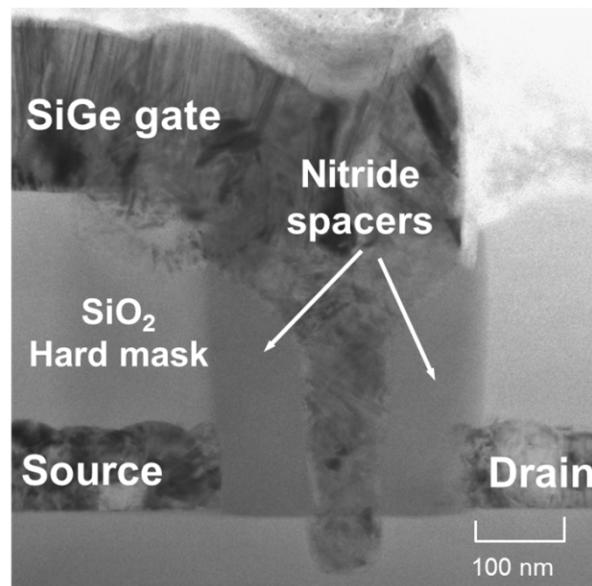
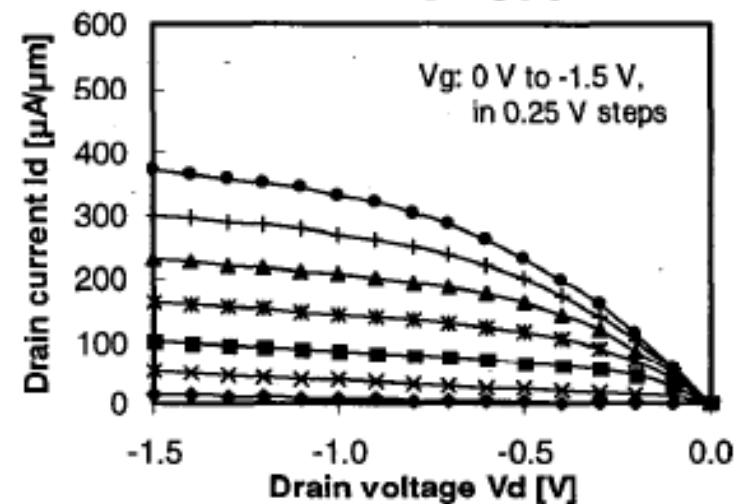
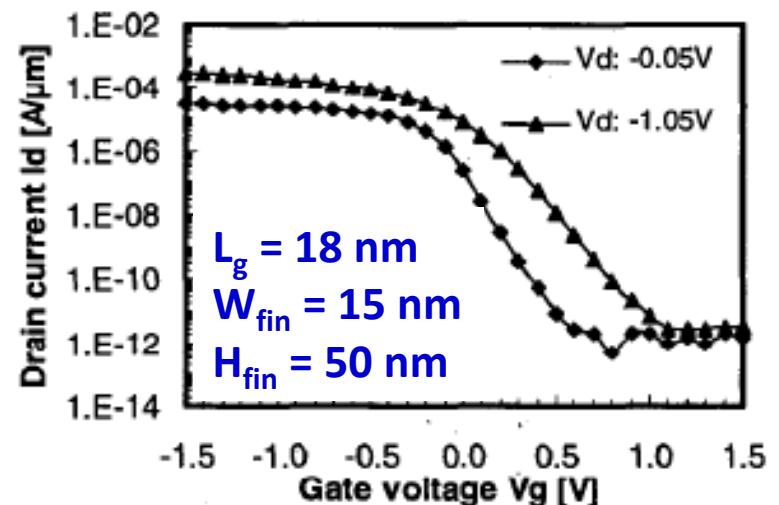


Figure 1: Schematic drawing of FinFET



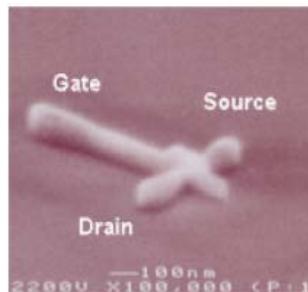
Transmission
Electron
Micrograph

X. Huang, IEDM(1999)

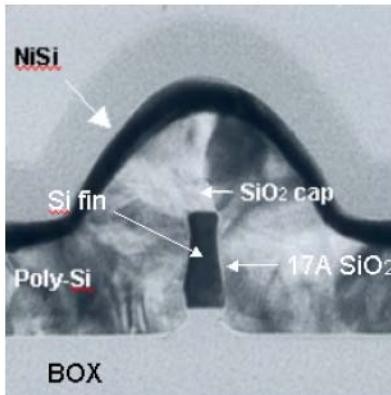
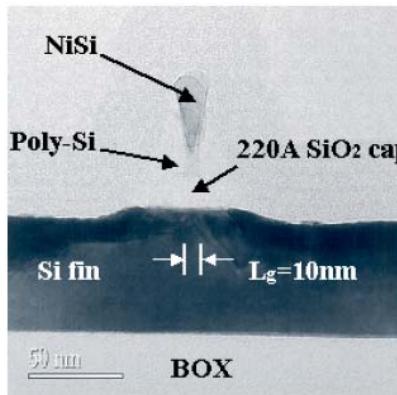


2002: 10 nm L_g FinFETs (AMD & UC Berkeley)

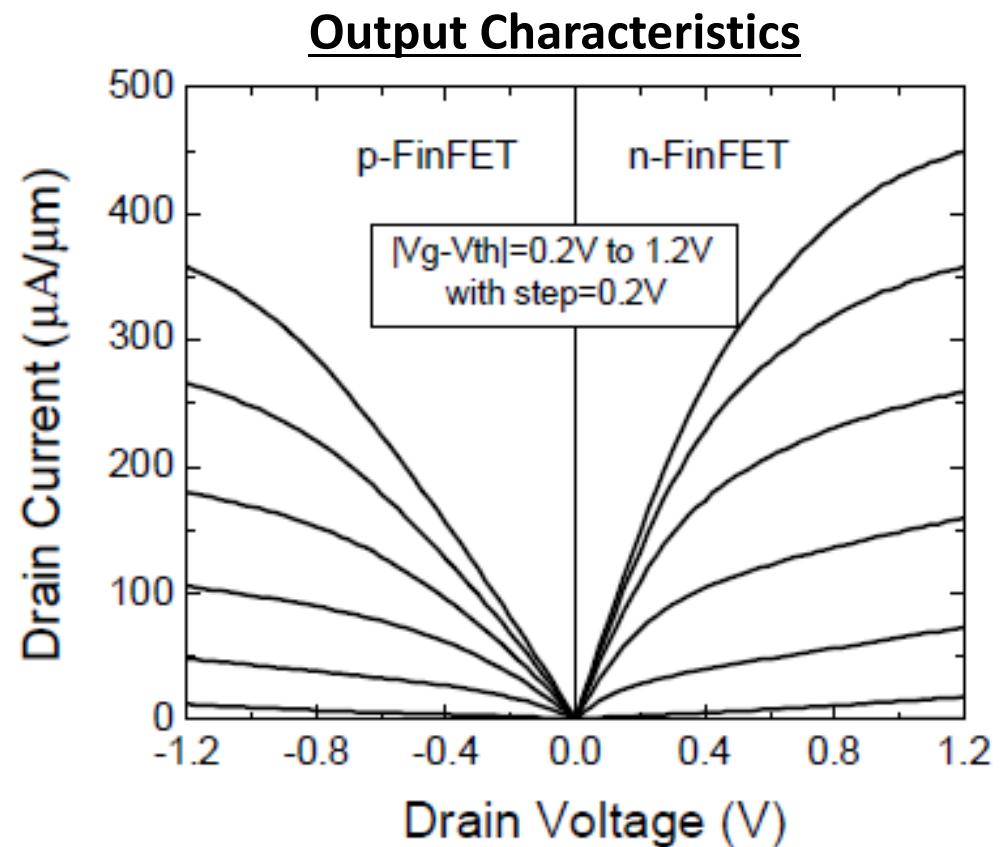
SEM
image:



TEM images

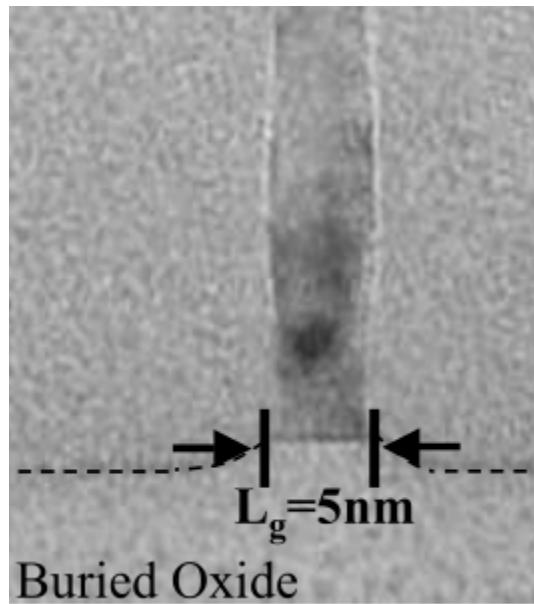
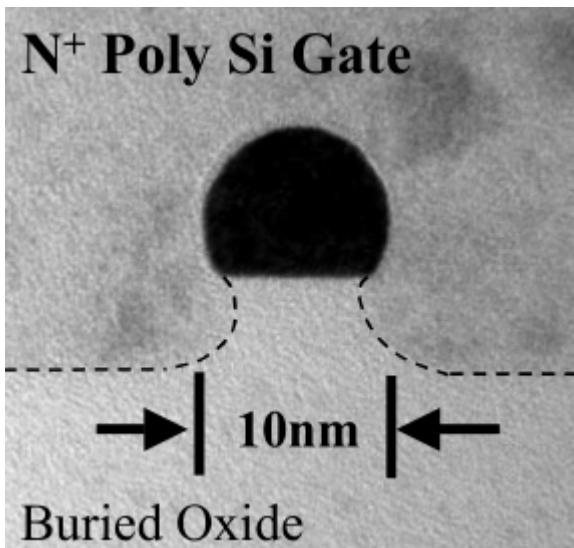


B. Yu, IEDM(2002)

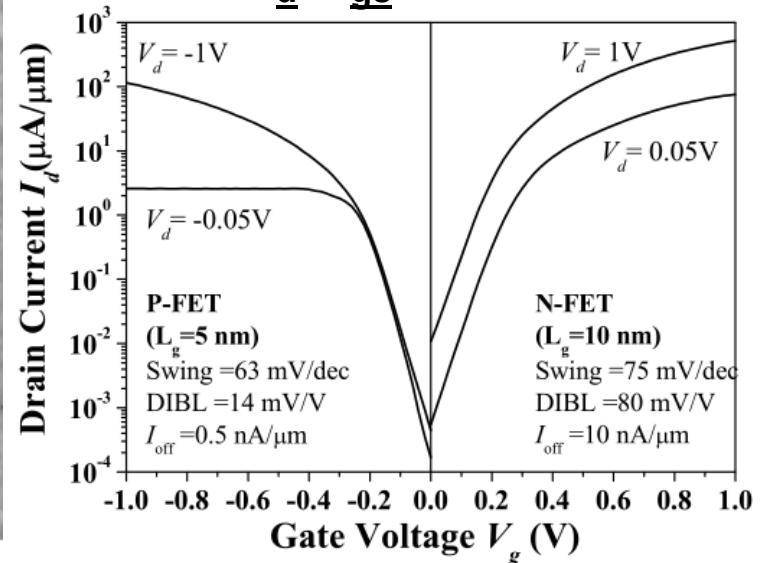


2004: 5 nm L_g FinFETs (TSMC)

TEM images

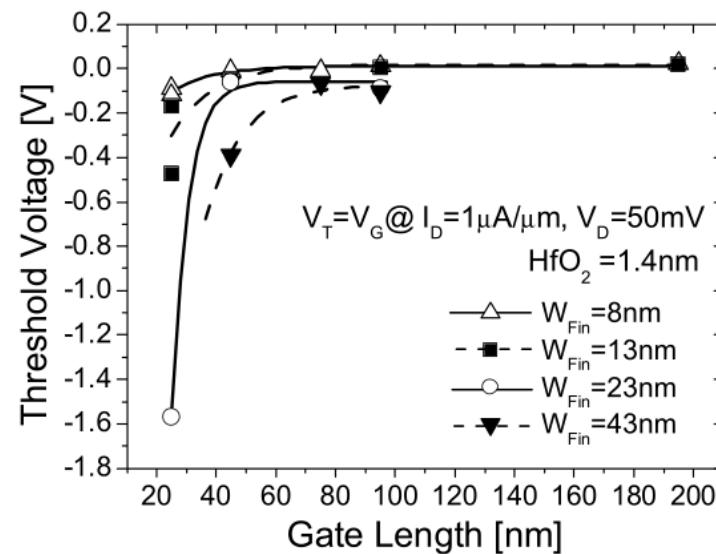
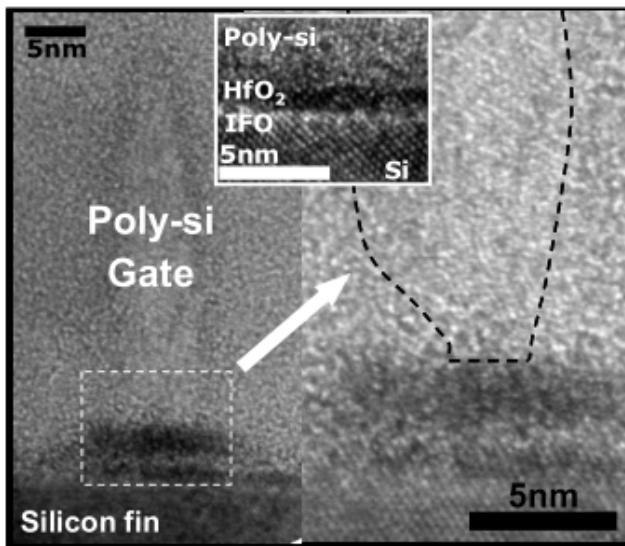
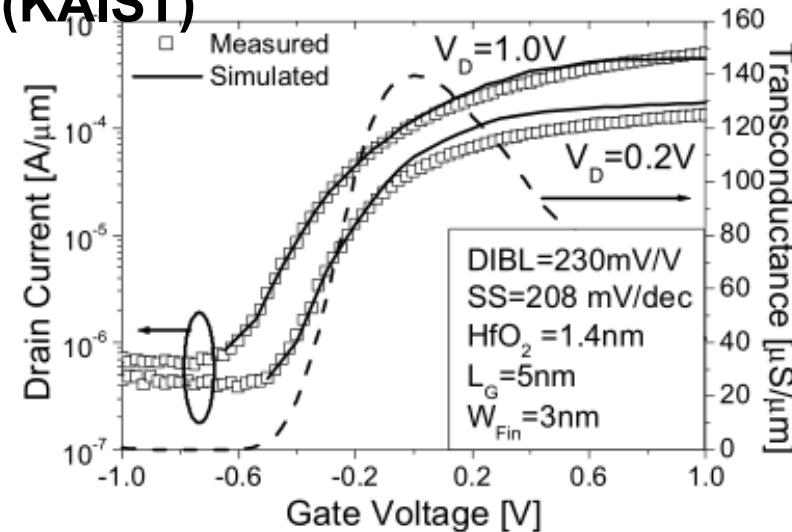
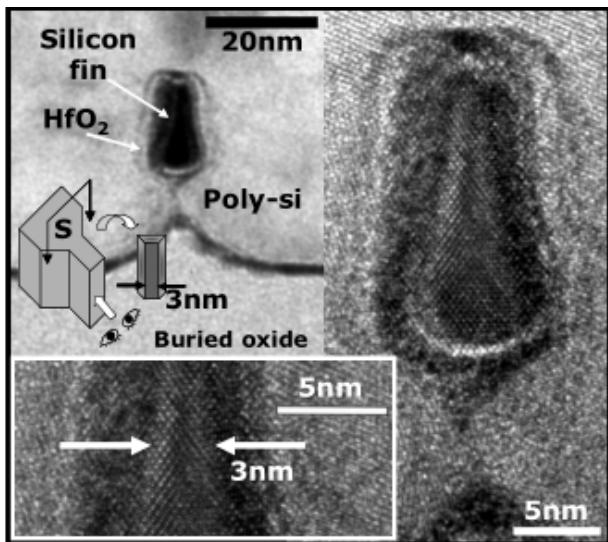


I_d-V_{gs} Curves



2006: 5 nm L_g , 3 nm W_{Fin} FinFETs

(KAIST)



H. Lee, VLSI-T(2006)

2004: 1st Bulk FinFET (Samsung)

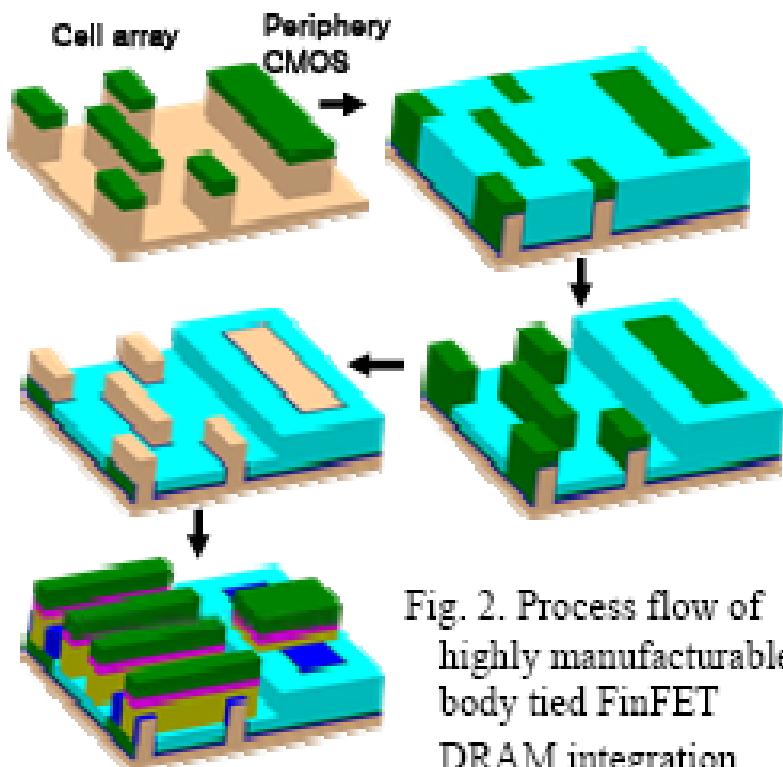
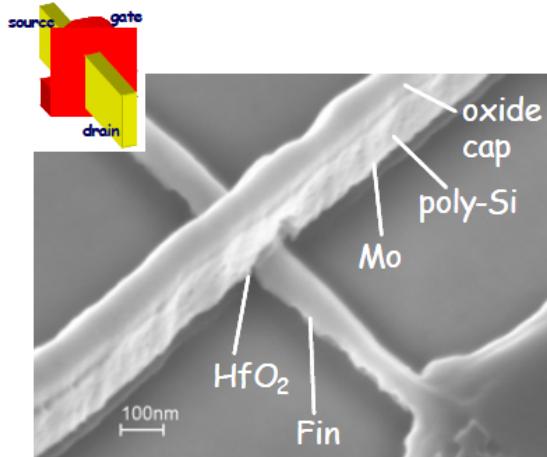


Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

C.-H. Lee, VLSI-T(2004)

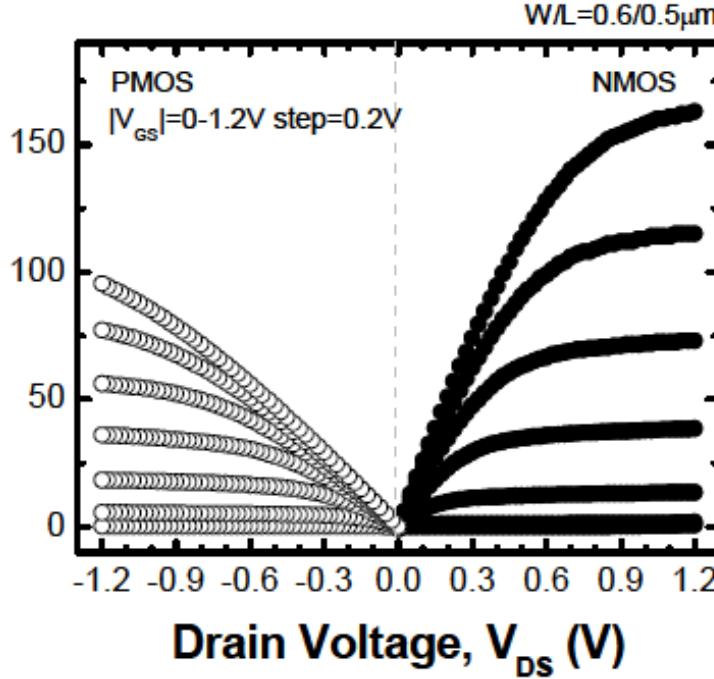
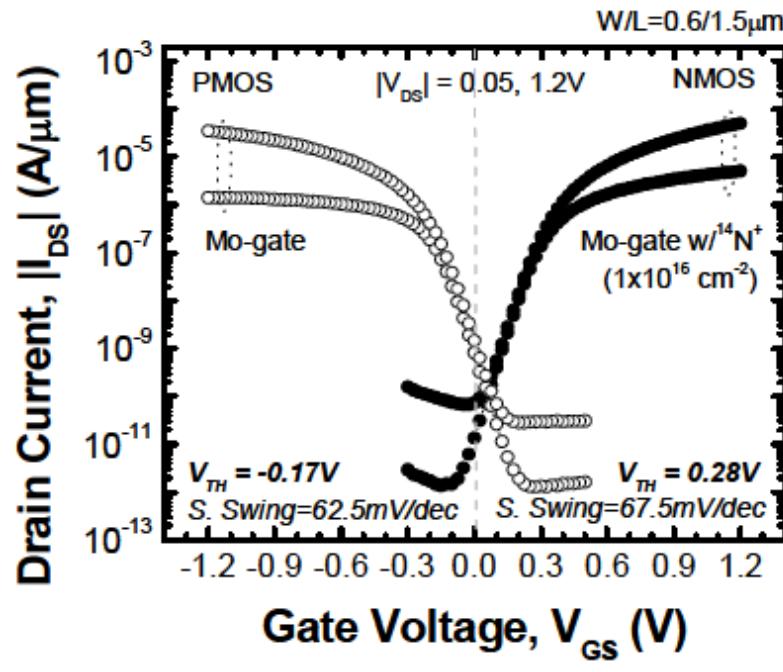
- FinFETs can be made on bulk-Si wafers
 - ✓ lower cost
 - ✓ improved thermal conduction with super-steep retrograde well (SSRW) or “punch-through stopper” at the base of the fins
 - 90 nm L_g FinFETs demonstrated
 - $W_{fin} = 80$ nm
 - $H_{fin} = 100$ nm
- DIBL = 25 mV

2004: High- κ FinFETs (UC Berkeley)



- FinFET Threshold Voltage tuning is flexible by implementing N into Mo metal gate.
- Highly matched N/P-FinFETs

D. Ha, IEDM(2004)



On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years. A new 3-dimensional transistor design will enable the production of integrated-circuit chips that operate faster with less power...

THE WALL STREET JOURNAL. ****

Thursday, May 5, 2011

CORPORATE NEWS

Intel Rethinks Chip's Building Blocks

By DON CLARK

Intel Corp. showed off what it called the most radical shift in semiconductor technology in more than fifty years, a design that could produce more powerful chips for gadgets without taxing their batteries.

The company plans to change a key part of each chip into a vertical, fin-like structure, a similar principle to the way high-rise buildings pack more office space in a city. The parts being changed—transistors—are the building block of nearly all electronic products; today's microchips can contain billions of tiny switching elements.

Intel said its latest technology could bring more computing power to smartphones and tablet computers as well as speed up corporate data centers—all while sharply reducing power consumption.

Though rivals also have been exploring similar technologies, Intel is the first to commit to using the so-called 3-D approach in high-volume production, a gamble that analysts said could help Intel marce the performance advantages of rivals that have largely kept Intel's chips out of the smartphone market.

"We've been talking about these 3-D circuits for more than

10 years, but no one has had the confidence to move them into manufacturing," said Dan Hutcheson, a chip-manufacturing specialist with the firm VLSI Research.

Intel executives demonstrated working chips based on the new approach at a gathering Wednesday in San Francisco. They indicated the first microprocessors would likely be targeted for high-end desktop computers and server systems and arrive in early 2012.

For decades, chip manufacturers have raced to shrink the size of components, which increases the performance of chips while decreasing the cost of each computing function. Competition has spurred companies to introduce ever-smaller processes every couple of years.

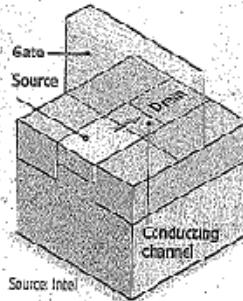
Intel executives say the shift to 3-D transistors brings more benefits than simply moving to a new generation of manufacturing technology. For example, if designers keep performance consumption constant, the new technology consumes half the power as Intel's existing production method.

"That is an unprecedented gain," said Mark Bohr, who holds the title of Intel fellow and leads its development of new manufacturing processes. "We've

Intel's Move Into 3-D

The chip maker breaks from conventional approaches to make transistors.

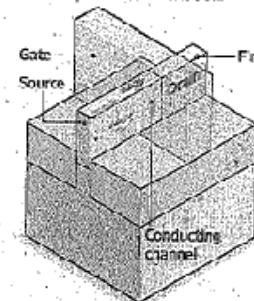
Conventional transistor: Electrons flow between components called a source and a drain, forming a two-dimensional conducting channel. A component called a gate starts and stops the flow, switching a transistor on or off.



never achieved that kind of performance gain at low voltage."

Chip designers have long worked in more than two dimensions, with transistors topped by layers of interconnecting wiring. Intel's shift relates to a part of each transistor that determines how fast electricity flows and how much current may leak out,

Intel's new transistor: A fin-like structure rises above the surface of the transistor with the gate wrapped around it, forming conducting channels on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.



affecting power consumption.

Intel engineers replaced a flat channel for conducting electrons with a fin-shaped structure surrounded on three sides by a device called a gate that turns the flow on and off. The three-dimensional shape, Mr. Bohr said, lets more current flow during the "on" state and less current

to leak when the transistor is switched "off."

Intel disclosed the underlying approach in research papers in 2002, and has spent the intervening years perfecting it. It has opted to shift completely to the new transistors for its next manufacturing process—slated to create chips with circuit dimensions measured at 22 nanometers, or billionths of a meter. Intel's current chips use 32-nanometer technology.

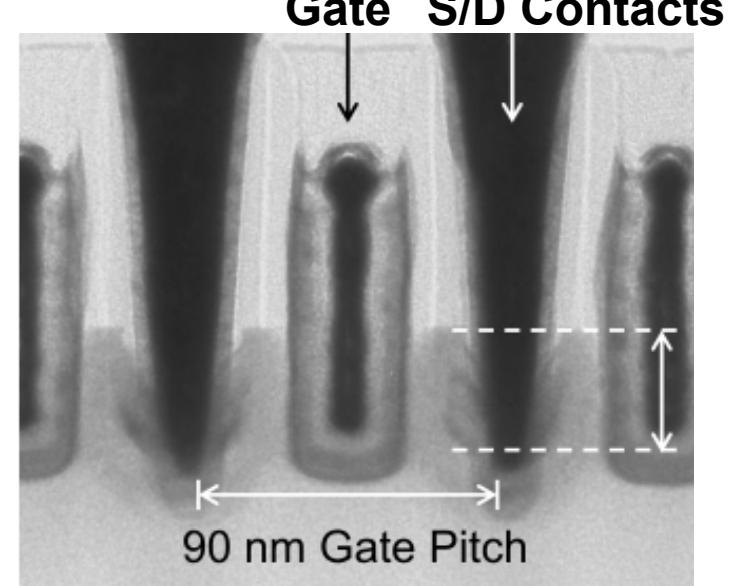
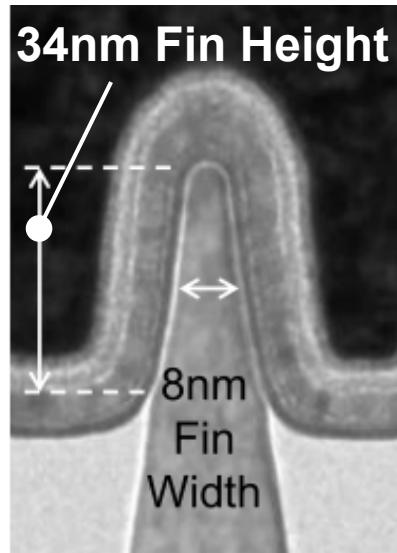
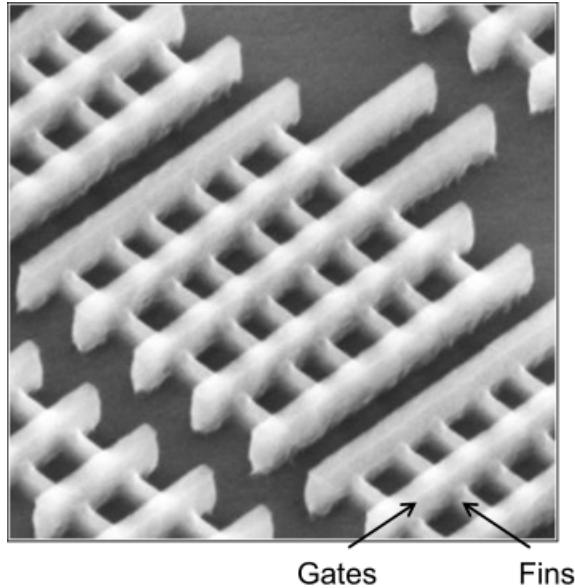
Departures from conventional manufacturing technologies tend to increase costs, and chip companies try to avoid them. Mr. Bohr said Intel concluded it could move to the new technology with a 2% to 3% increase in the cost of a finished silicon wafer, each of which contains hundreds of chips.

Others are expected to use the approach at some point, too, but not until they have shrunk their circuitry beyond 22 nanometers.

Globalfoundries, a production service spun off from Advanced Micro Devices Inc., said Wednesday it will use conventional transistors for its forthcoming 20-nanometer process. "We don't see the need" for technologies like 3-D transistors until subsequent production processes, a spokesman said.

2012: 1st Tri-Gate FETs in Production

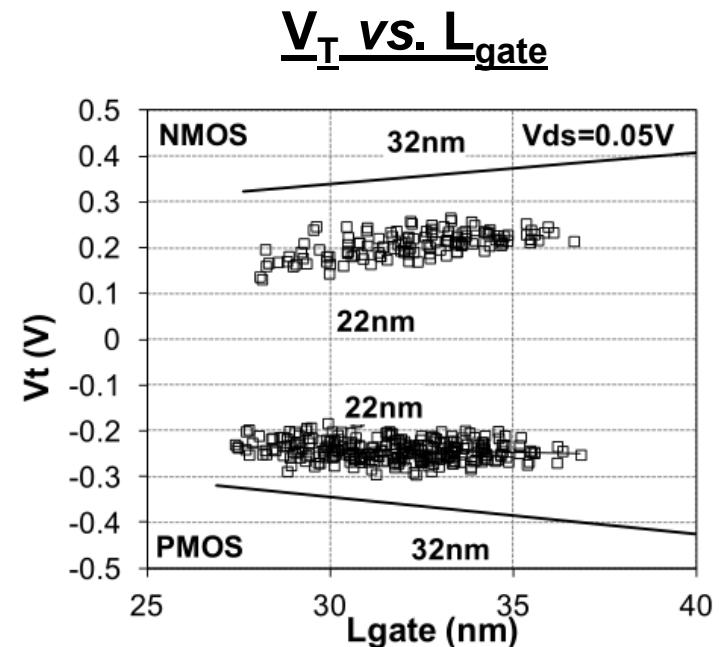
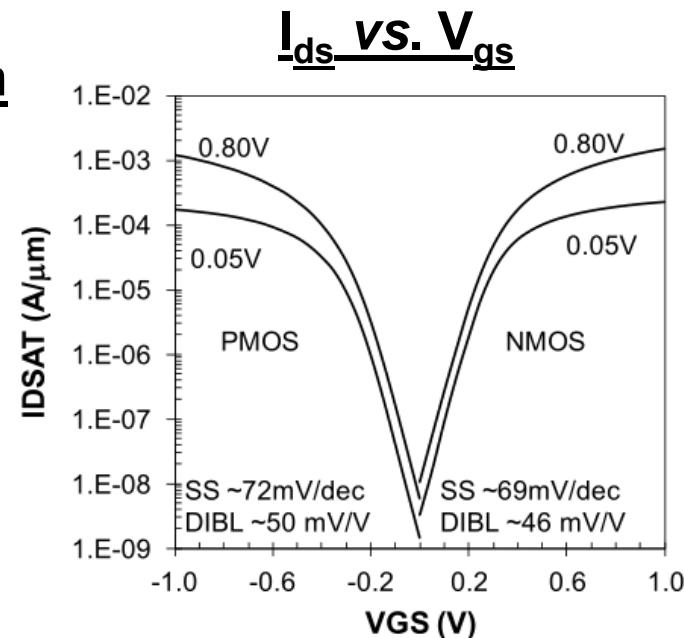
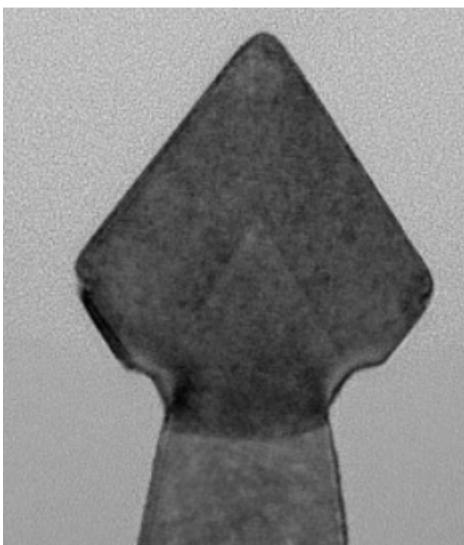
(Intel)



C. Auth, VLSI-T (2012)
M. Bohr, Intel Design Forum (2012)

Intel's Tri-Gate FETs Performance

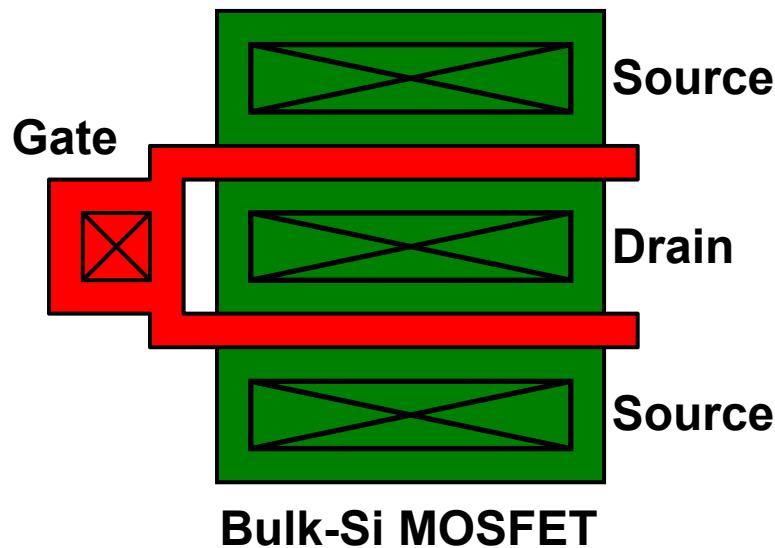
TEM of PMOS epi-SiGe Source/Drain



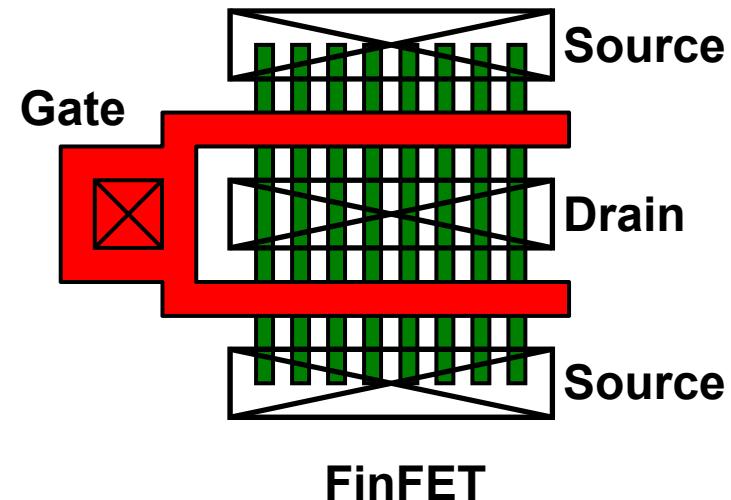
C. Auth, VLSI-T (2012)
M. Bohr, Intel Design Forum (2012)

FinFET Layout

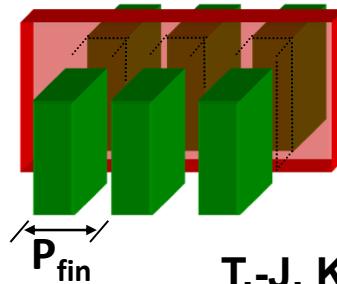
- Layout is similar to that of conventional planar MOSFET, except that the channel width is quantized:



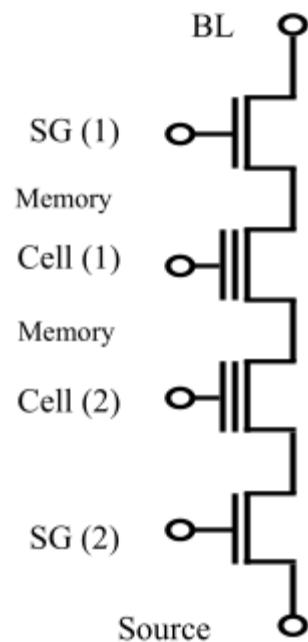
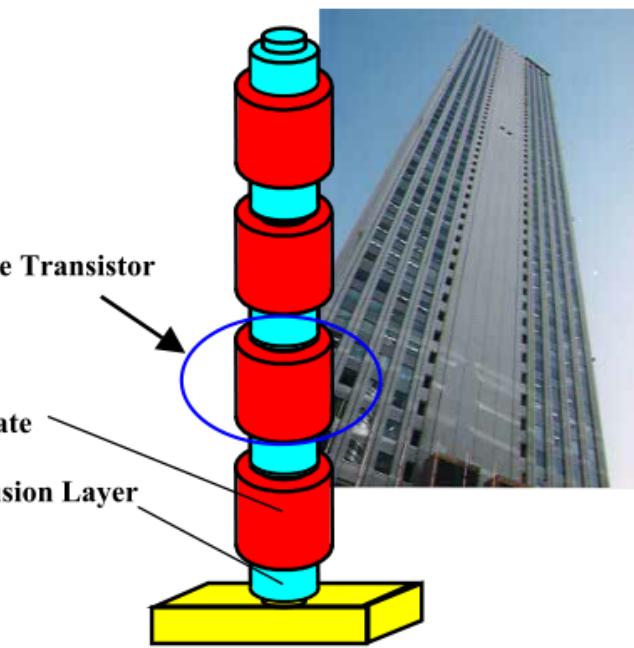
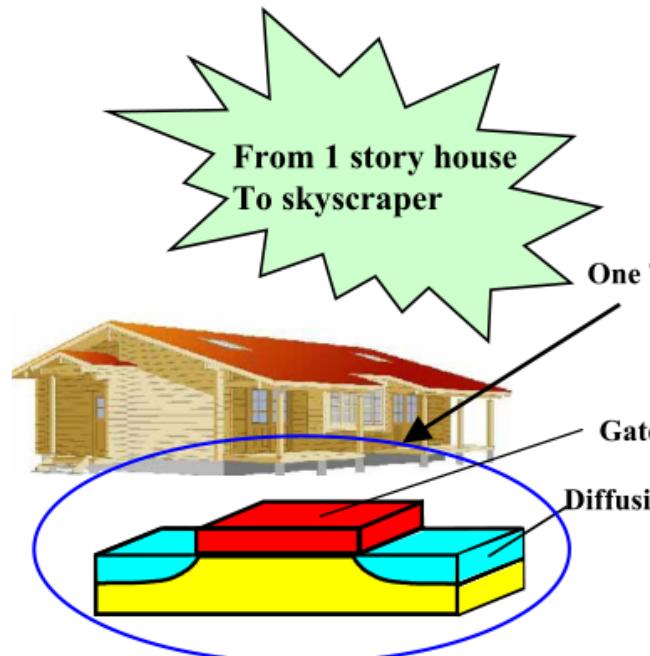
$$W_{\text{eff}} = (2 * H_{\text{fin}}) * N_{\text{Fins}} * N_{\text{Gate-fingers}}$$



- Fin pitch (P_{fin}) is a new key parameter to be optimized for performance and layout efficiency.



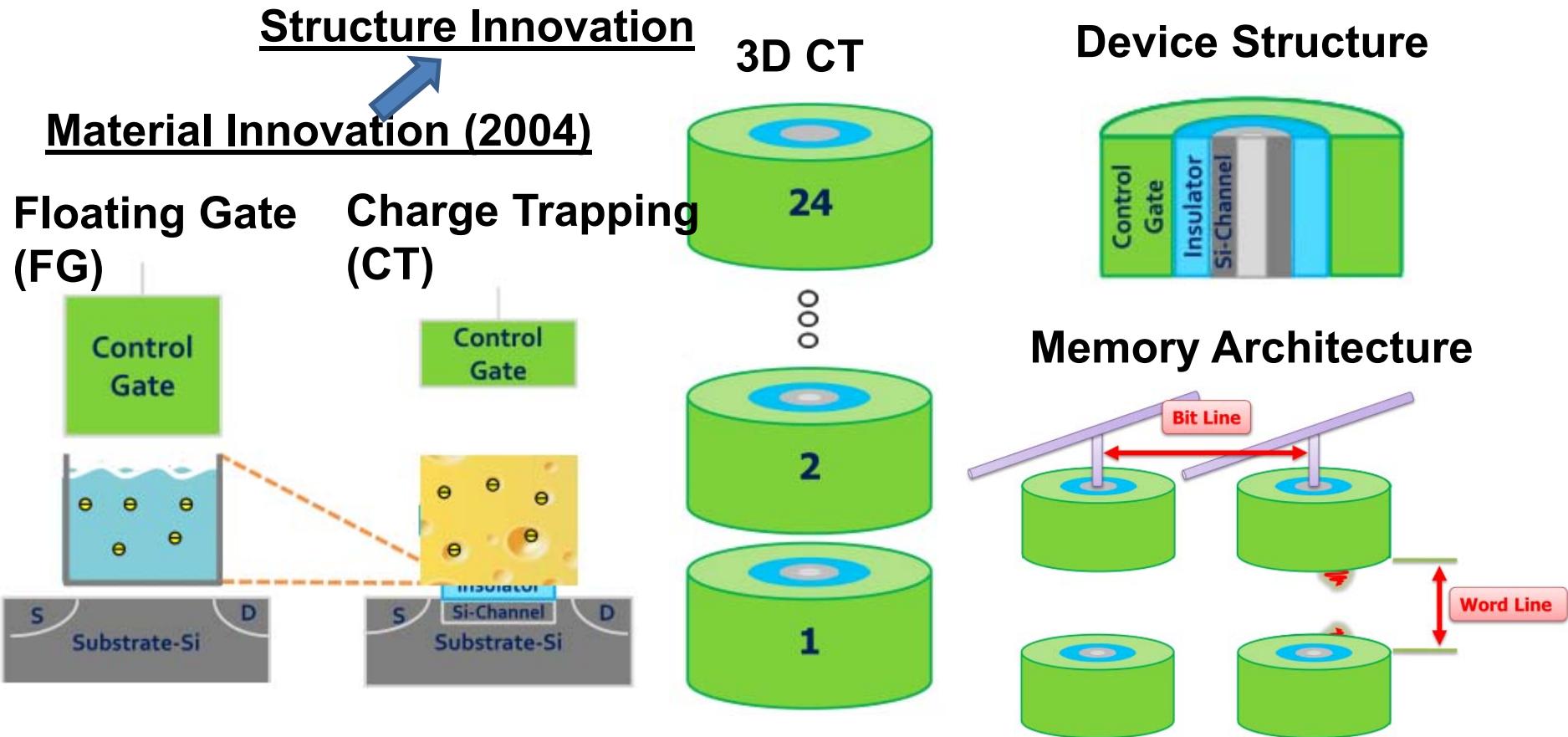
Vertical Stacked MOSFETs – Implication for High Density Memory



Currently used Planar type Transistor

Proposed novel Stacked Vertical Transistor

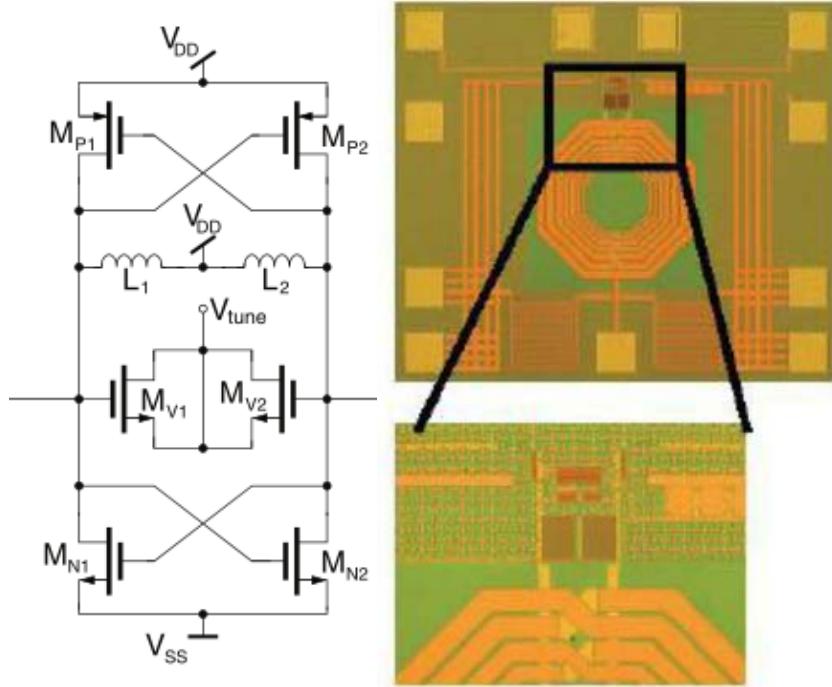
2013: 1st 3-Dimensional NAND (Samsung)



J. Elliott & E.S. Jung, Flash Memory Summit (2013)

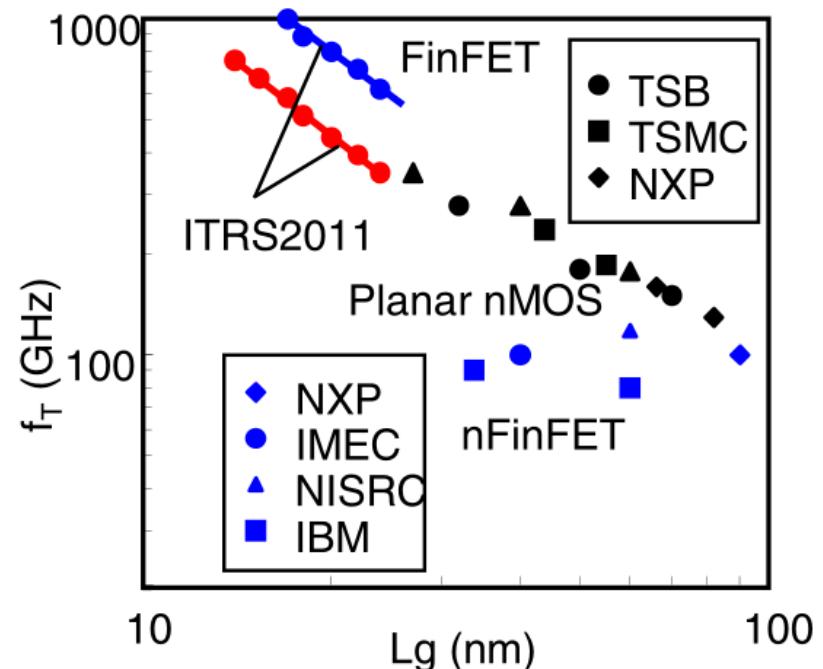
FinFETs in Analog/RF World

FinFET-based VCO



G. Knoblinger, *Int. SOI Conf.* (2007)

Cutoff Frequency (f_T): Bulk vs. FinFET



T. Ohguro, *VLSI-T*(2012)

Summary

- The FinFET was originally developed for manufacture of self-aligned double-gate MOSFETs, to address the need for improved gate control to suppress I_{OFF} , DIBL and process-induced variability for $L_g < 25\text{nm}$.
 - Different variations of the FinFET have been developed to improve performance, manufacturability and cost.
 - It has taken ~10 years to bring “3-D” transistors into volume production.
- Multi-gate MOSFETs provide a pathway to achieving lower power and/or improved performance.
 - Further evolution of the MOSFET to a 3-D stacked-channel structure may occur by the end of the roadmap.
 - Issues needed to address for implementing FinFET into a System-on-Chip (SoC).

Course Modules

1. Device Physics (~5 lectures)

- History and course overview
- Short-channel MOSFET Issues, performance metrics,
- Thin-body transistors design, scale length,
- MOSFET Compact Modeling, Technology CAD

2. Device-Process Interactions (~9 Lectures)

- Advanced MOSFET process flow overview,
- FinFET substrate impacts,
- Advanced gate stack process,
- Source/Drain doping, Threshold Voltage tuning for FinFETs
- Quantum Mechanical effects,
- Carrier mobilities, Strained-Si technology, **high mobility channel materials (guest lecture)**

Course Modules (Cont'd)

3. Device-Circuit Interactions (~9 lectures)

- Performance variability: systematic and random
- Industry's state-of-the-art FinFET platforms
- FinFET-based SRAM design
- FinFET-based analog and RF device/circuit
- 3-D integrations for advanced CMOS technologies
- FinFET reliability issues: Bias-Temperature Instability, noise, ESD and self-heating,...

References

Retrograde Well Doping

1. R.-H. Yan, A. Ourmazd, K.F. Lee, “Scaling the Si MOSFET: from Bulk to SOI to Bulk,” *IEEE Transactions on Electron Devices*, Vol. 39, Issue 7, pp. 1704-1710, 1992.
2. A. Hokazono, H. Itokawa, N. Kusunoki, I. Mizushima, S. Inaba, S. Kawanaka, Y. Toyoshima, “Steep Channel & Halo Profiles utilizing Boron-Diffusion-Barrier Layers (Si:C) for 32 nm and Beyond,” *Symposium on VLSI Technology Digest*, pp. 112-113, 2008.
3. A. Hokazono, H. Itokawa, I. Mizushima, S. Kawanaka, S. Inaba, Y. Toyoshima, “Steep Channel Profiles in n/p MOS Controlled by Boron-doped Si:C Layers for Continued Bulk CMOS Scaling,” *IEEE International Electron Devices Meeting Technical Digest*, pp. 673-676, 2009.

UTB on SOI

4. (IBM) K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss *et al.*, “Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications,” *IEEE International Electron Devices Meeting Technical Digest*, pp. 49-52, 2009.
5. (STMicroelectronics) C. Fenouillet-Beranger, P. Perreau, L. Pham-Nguyen, S. Denorme, F. Andrieu *et al.*, “Hybrid FDSOI/Bulk high-k/Metal Gate platform for Low Power (LP) multimedia technology,” *IEEE International Electron Devices Meeting Technical Digest*, pp. 667-670, 2009.

FinFET

6. (Delta MOSFET) D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, “A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET,” *IEEE Electron Device Letters* Vol. 11, pp. 36-39, 1990.
7. (1st N-FinFET) D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, C. Hu, “A folded-channel MOSFET for deep-sub-tenth micron era,” *IEEE International Electron Devices Meeting Technical Digest*, pp. 1032-1034, 1998.

References (Cont'd)

8. (1st P-FinFET) X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, C. Hu, "[Sub 50-nm FinFET: PMOS](#)," *IEEE International Electron Devices Meeting Technical Digest*, pp. 67-70, 1999.
9. (AMD's 10nm-Lg) B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabcry, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, D. Kyser, "[FinFET scaling to 10nm gate length](#)," *IEEE International Electron Devices Meeting Technical Digest*, pp. 251-254, 2002.
10. (TSMC's 5nm-Lg) F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu *et al.*, "[5nm-Gate Nanowire FinFET](#)," *Symposium on VLSI Technology Digest*, pp. 196-197, 2004.
11. H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon *et al.*, "[Sub-5nm All-Around Gate FinFET for Ultimate Scaling](#)," *Symposium on VLSI Technology Digest*, 2006.
12. (Samsung's Bulk Fin) C.-H. Lee,
13. D. Ha, Y.-K. Choi, T.-J. King, W.-P. Bai, D.-L. Kwong, A. Agarwal, M. Ameen, "[Molybdenum-gate HfO₂ CMOS FinFET technology](#)," *IEEE International Electron Devices Meeting Technical Digest*, pp. 643-646, 2004.
14. (Intel's Tri-Gate) C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, "[A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors](#)," *Symposium on VLSI Technology Digest*, pp. 131-132, 2012.
15. (Intel's Tri-Gate) M. Bohr, "[Silicon Technology Leadership for the Mobility Era](#)," Intel Design Forum, 2012.

References (Cont'd)

3-D NAND & Mixed Signal

16. T. Endoh, “[Impact of 3D Structured Devices – High Performance Logic & High Density Memory](#),” *Stanford and Tohoku Open Workshop*, 2007.
17. (Samsung’s V-NAND) J. Elliott, E.S. Jung, “[Ushering in the 3D Memory Era with V-NAND](#),” *Flash Memory Summit*, 2013.
18. T.-J. King Liu, N. Xu, “[FinFET versus UTBB SOI for Analog/RF Applications](#),” *International Solid-State Circuit Conference, Forum 6: Mixed-Signal RF Design and Modeling in Next-Generation CMOS*, 2013.
19. (VCO) G. Knoblinger, M. Fude, D. Siprak, U. Hodel, K. Von Arnim, Th. Schulz, C. Pacha, U. Baumann, A. Marshall, W. Xiong, C.R. Cleavelin, P. Patruno, K. Schruefer, “[Evaluation of FinFET RF Building Blocks](#),” *IEEE International SOI Conference Digest*, 2007.
20. (f_T) T. Ohguro, Y. Higashi, K. Okano, S. Inaba, Y. Toyoshima, “[The Optimum Device Parameters for High RF and Analog/MS Performance in Planar MOSFET and FinFET](#),” *Symposium on VLSI Technology Digest*, pp. 149-150, 2012.