

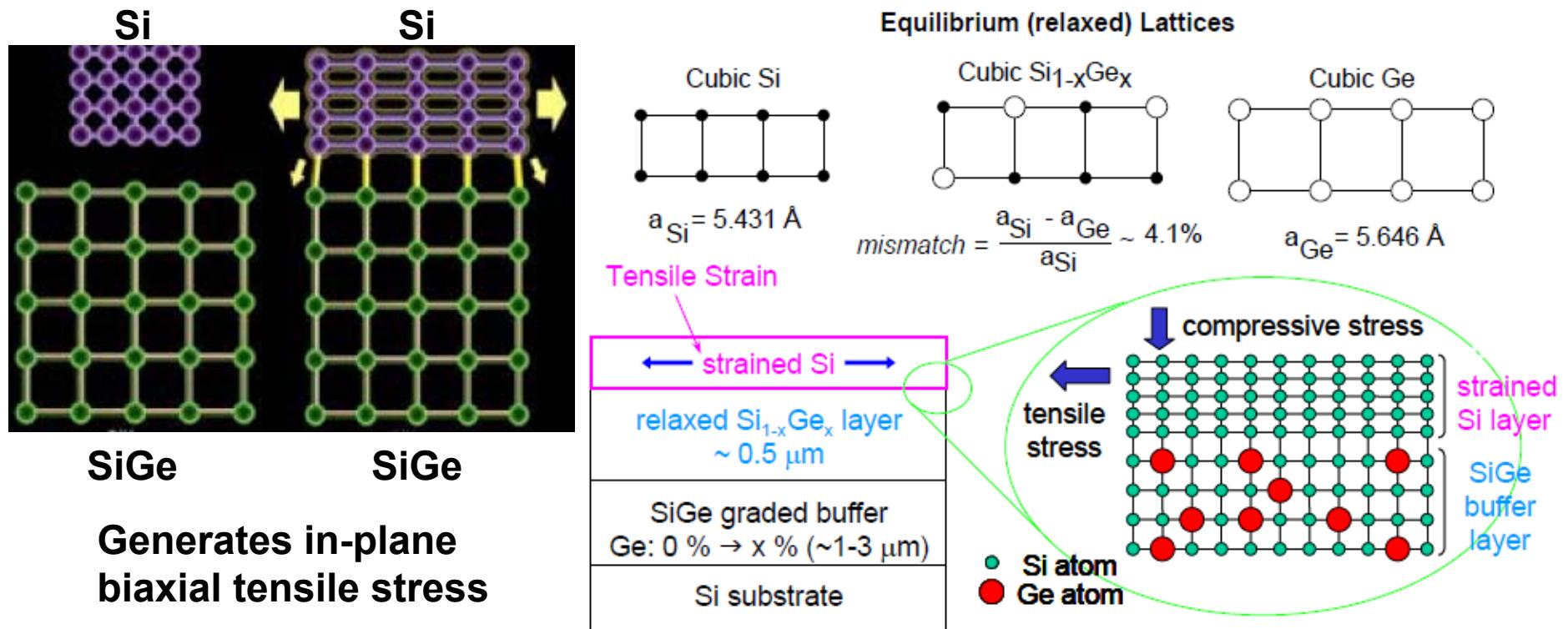
Strain mapping from a 32nm node PMOS. Courtesy of B. Özsdöl (LBNL)

Lecture 10

- **Strained-Si Technology II: Process Implementation**
 - Stressors in Si CMOSFETs
 - Effectiveness of Stressors on Thin-Body MOSFETs

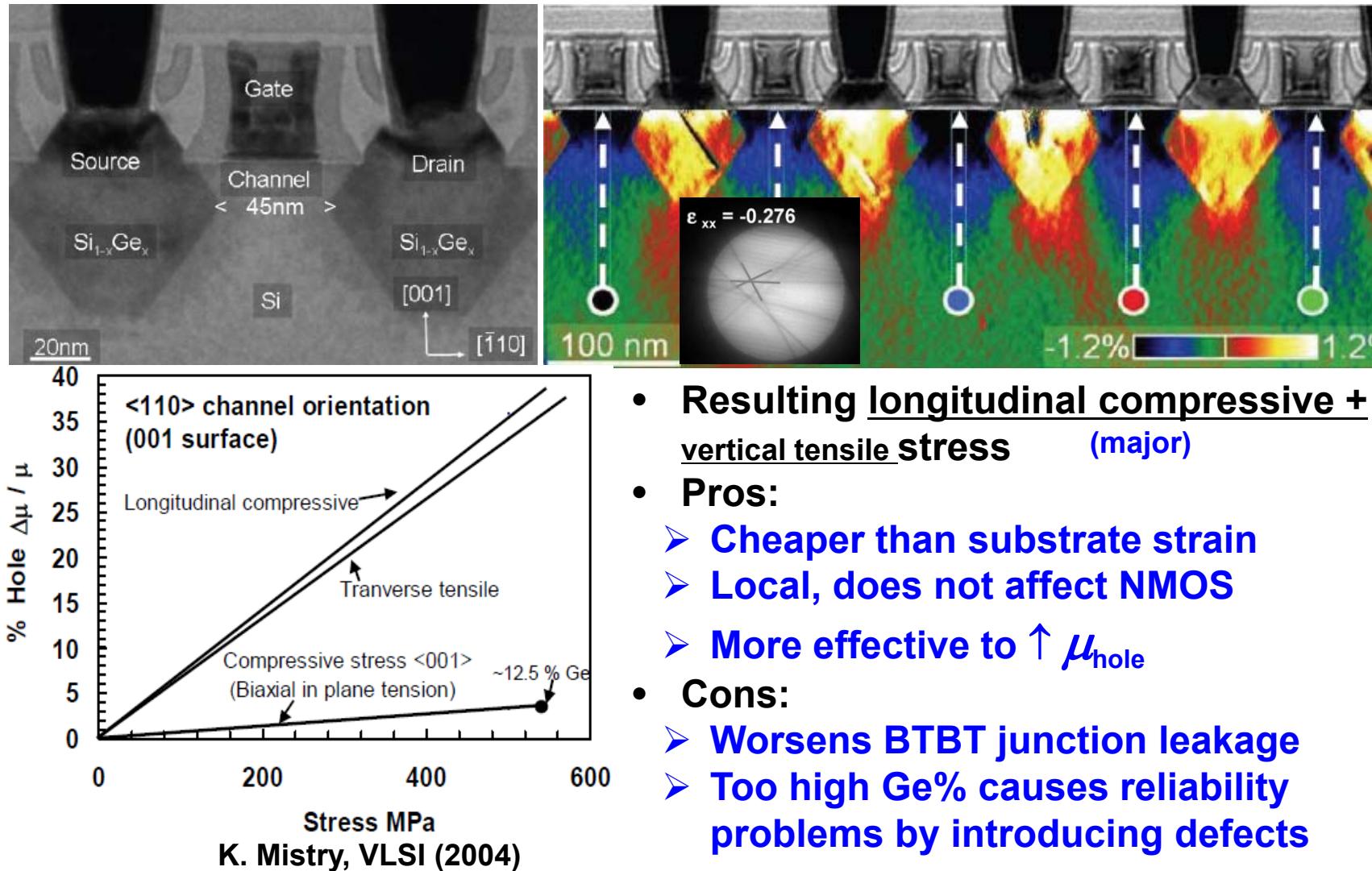
Reading: multiple research articles (reference list at the end of this lecture)

Substrate-induced Strain: SiGe/Si



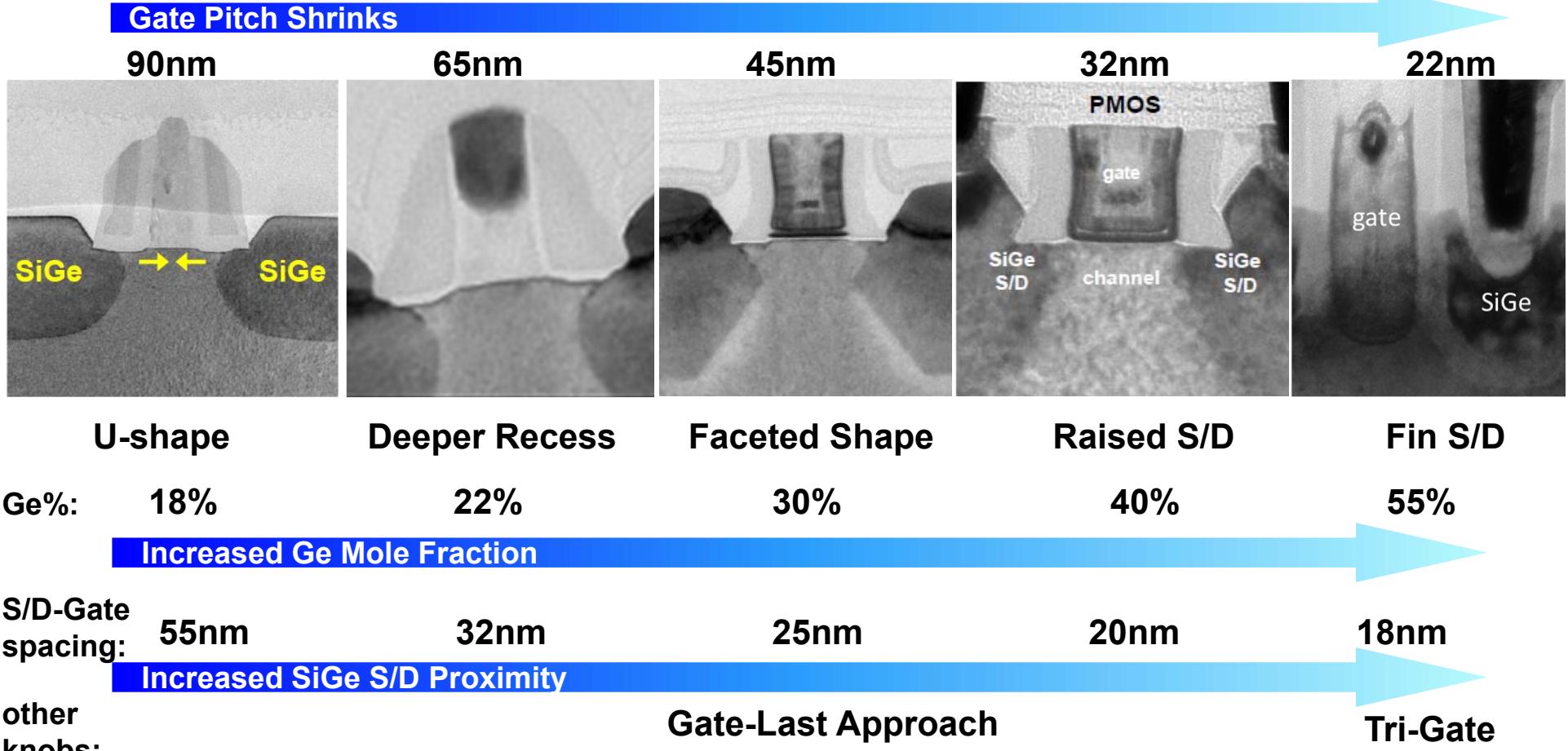
- In old generations of technology, strain is always introduced by growing Si thin channel on top of a relaxed SiGe layer.
- Drawbacks:
 - Enhanced substrate cost
 - Strain is global: for both P- and N- MOS
 - Thermal budget

Embedded Source/Drain Stressor: SiGe for PMOS



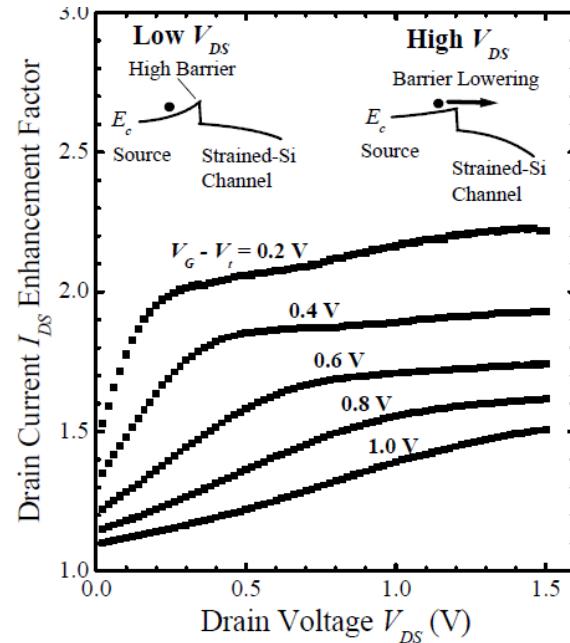
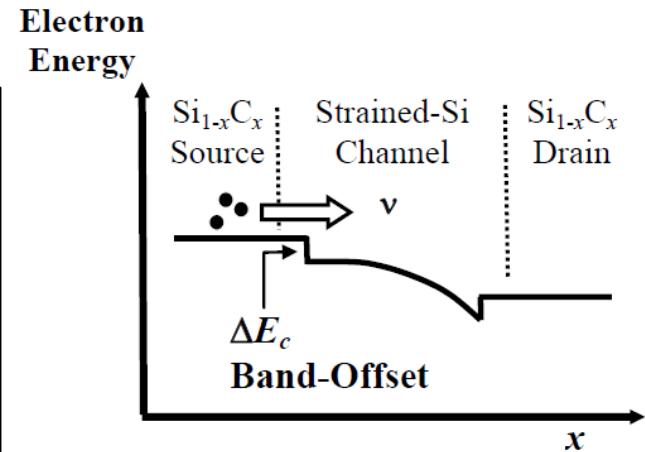
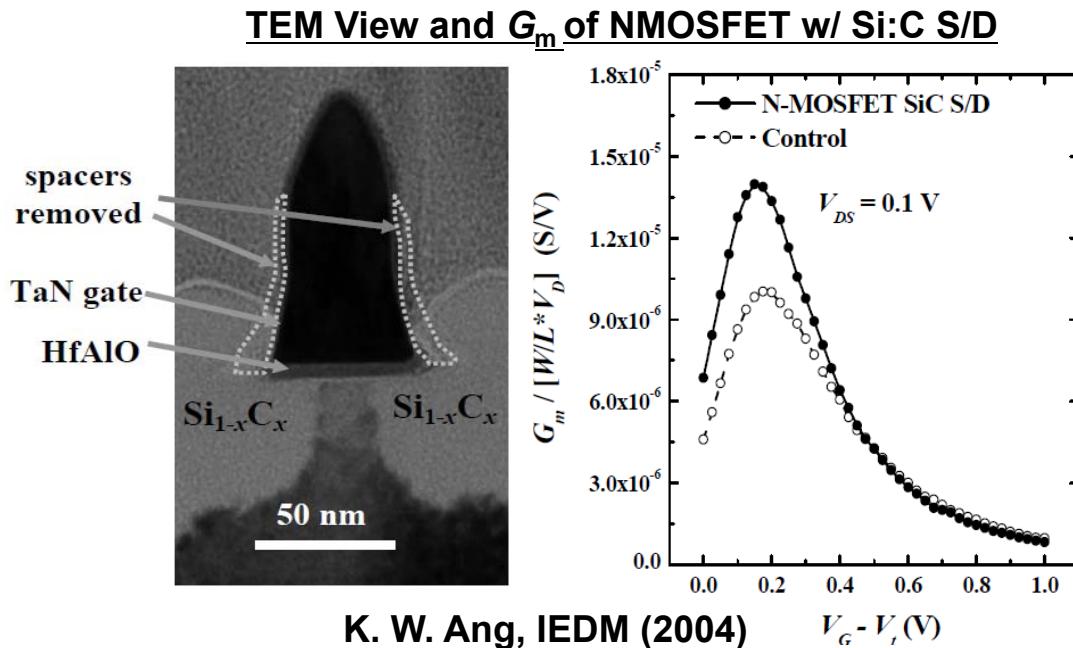
Evolution of eSiGe S/D Technology

Intel's eSiGe S/D Technology



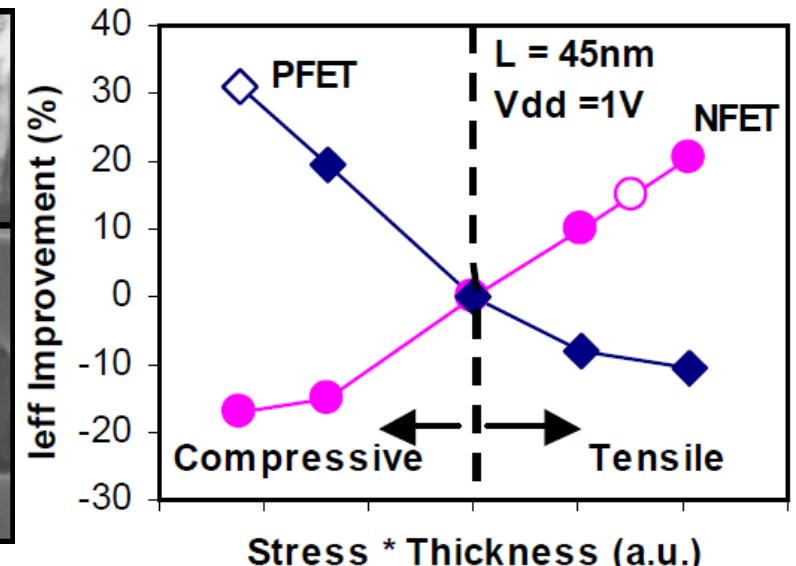
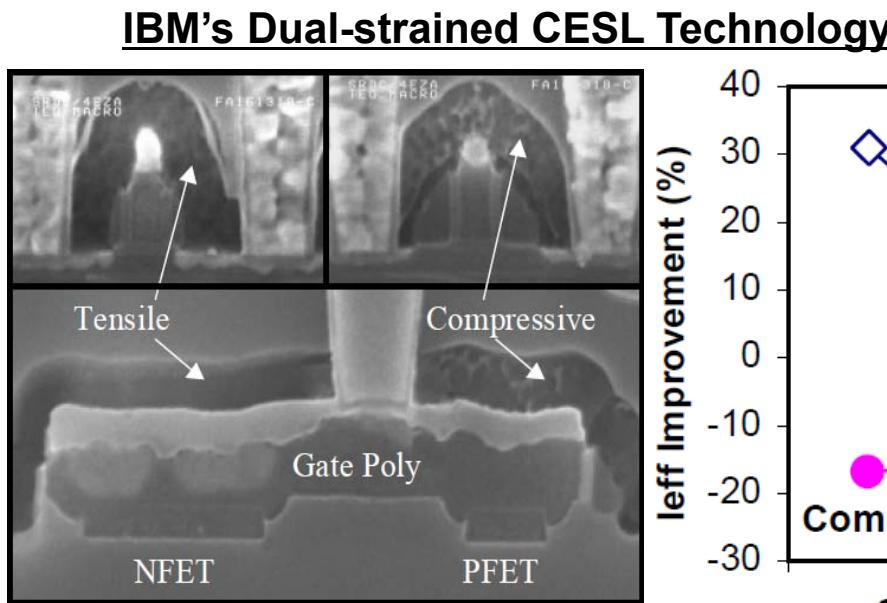
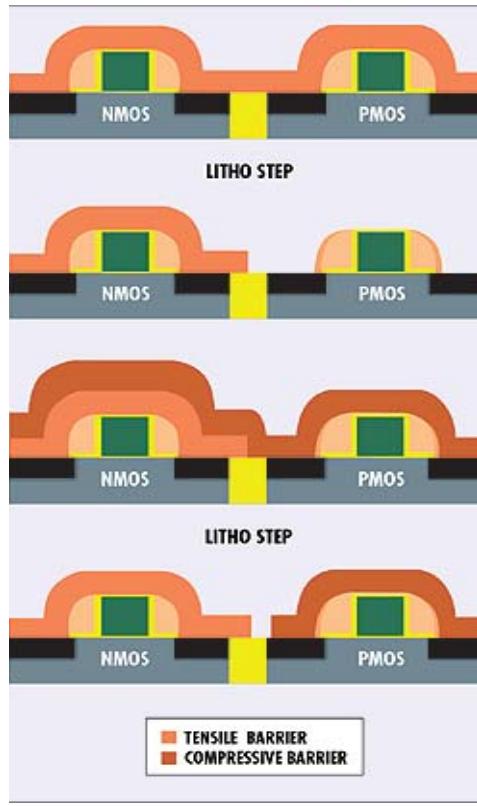
K. Mistry, VLSI (2004) C. Auth, VLSI (2008) P. Packan, IEDM (2009) C. Auth, VLSI (2012)

Embedded Source/Drain Stressor: Si:C for NMOS



- Resulting longitudinal tensile + vertical compressive stress
→ Good for NMOS mobility
- A barrier forms at Source/channel interface for electrons
→ Reduced drain current at low V_{DS}

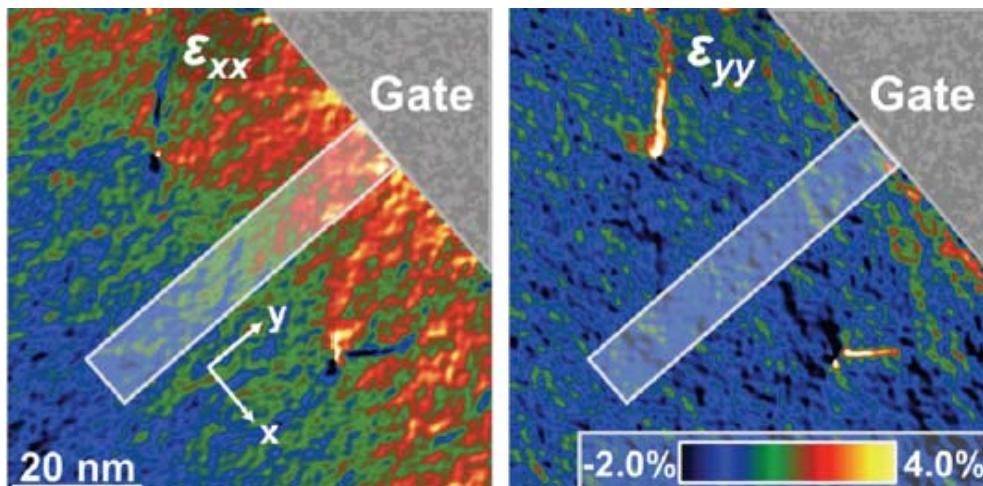
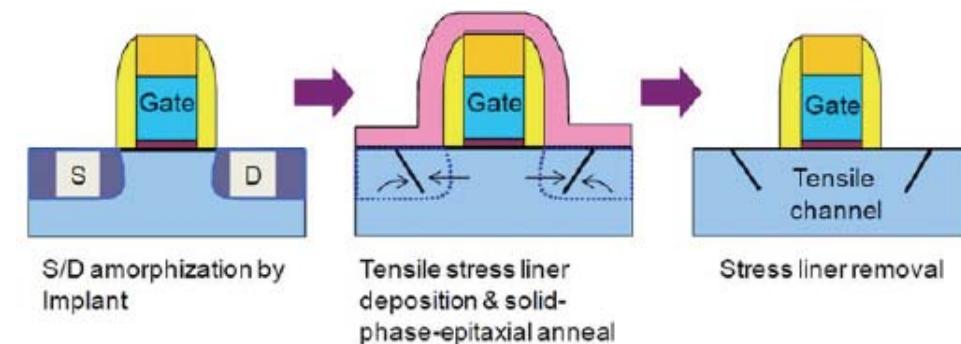
Strained Contact-Etch-Stop-Liner (CESL) Technology



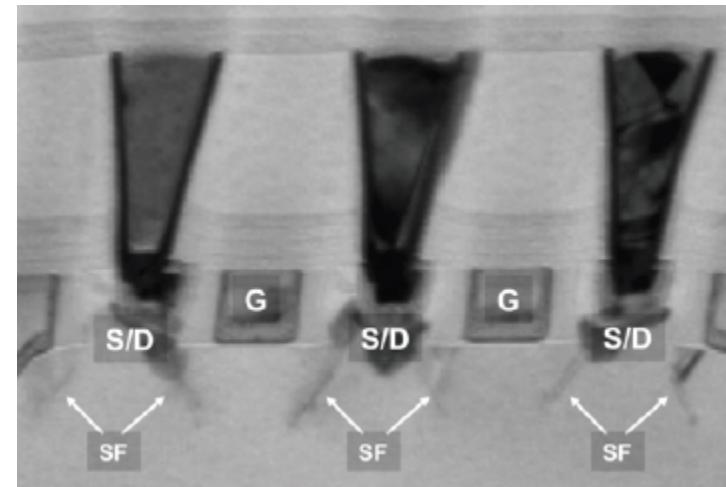
H.-S. Yang, IEDM (2004)

- Pros:
 - Easy to integrate (low thermal budget)
 - No reliability or performance degradation issues
- Cons:
 - Low stress transfer efficiency

Stress Memorization Technology (SMT): Source/Drain

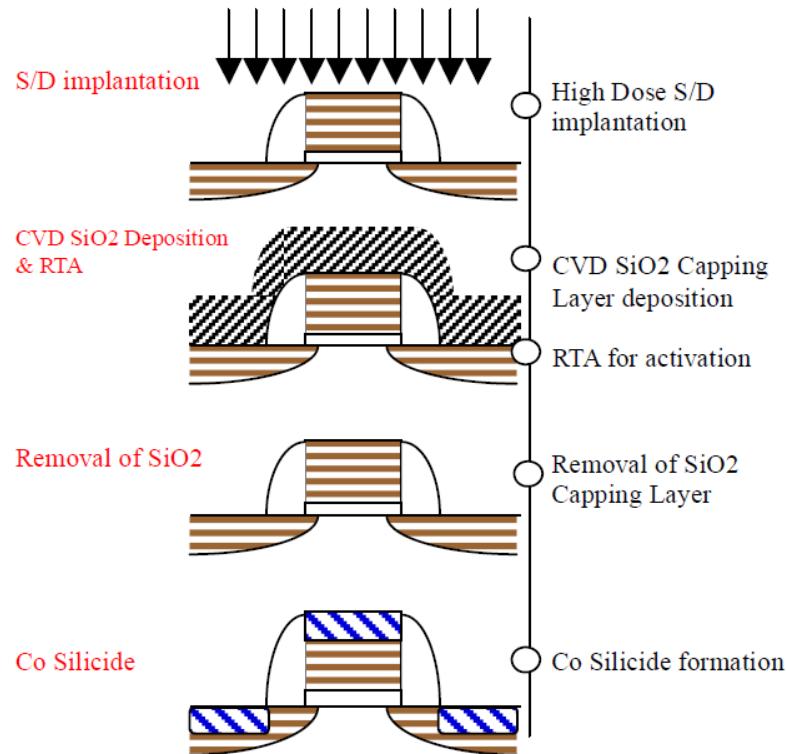


K. Y. Lim, IEDM (2009)

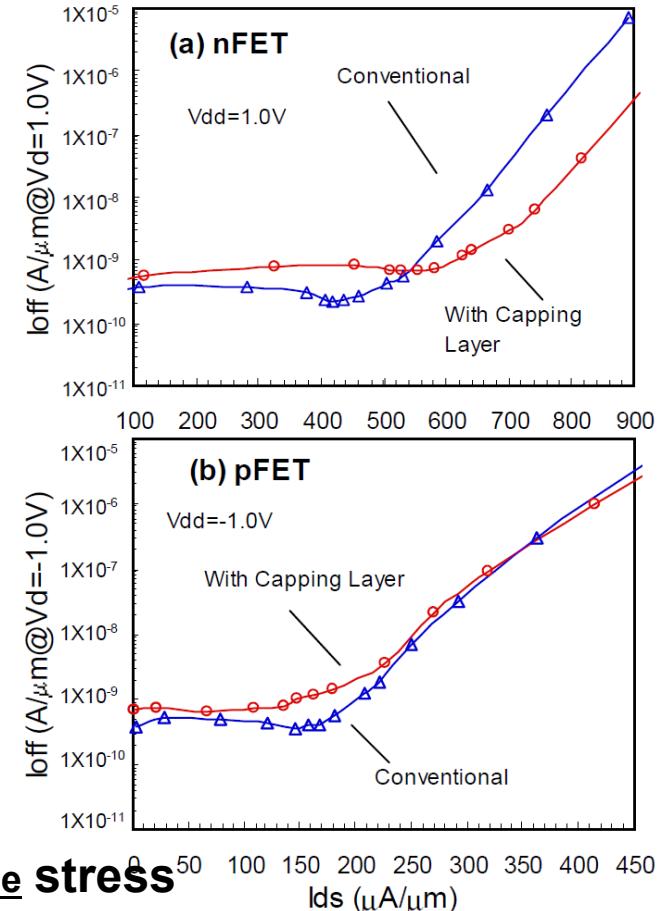
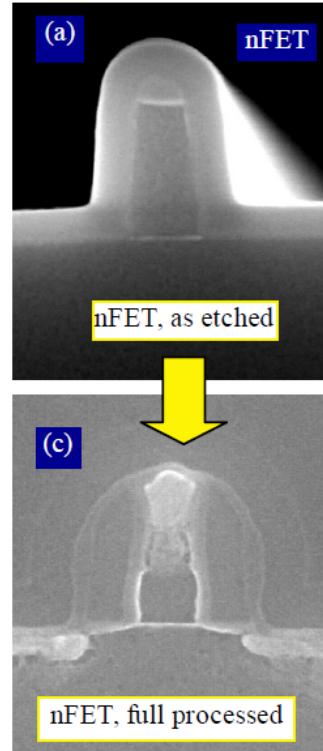


- Resulting longitudinal tensile + Vertical Compressive stress → Good for NMOS mobility
- Amorphized S/D will not be fully recovered when Si volume is shrunk. → Not applicable to thin-body MOSFETs

Stress Memorization Technology (SMT): Poly-Si Gate

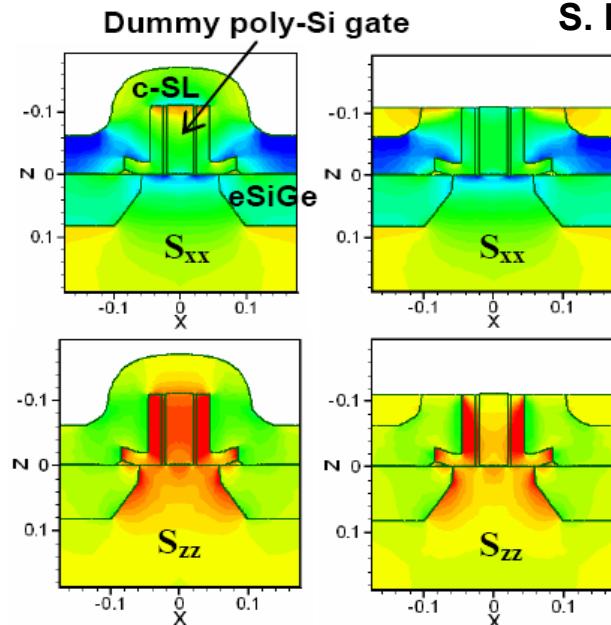


K. Ota, IEDM (2002)
(major)



- Resulting vertical compressive + longitudinal tensile stress for As-doped poly-Si
→ NMOS (electron) mobility enhanced; PMOS unaffected
- Not applicable to metal gate MOSFETs.

Impact of Metal-Gate-Last Process on Channel Strain



1. Deposition of CESL

2. CMP

3. Dummy Gate Removal

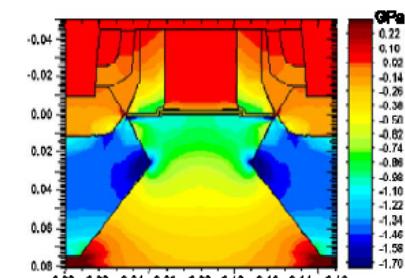
4. Metal Gate Refill

- After poly-Si (dummy) gate removal, longitudinal stress (S_{xx}) is enhanced due to free boundary conditions to the S/D stressors; vertical stress (S_{zz}) is reduced due to the loss of contacted surface from the gate.
 - A trade-off between S_{xx} and S_{zz}

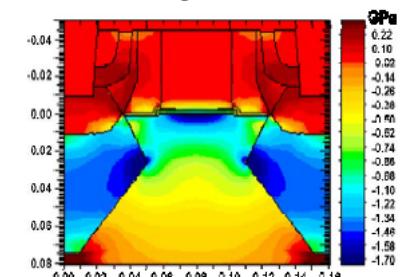
Intel's 45nm PMOS

C. Auth, VLSI (2008)

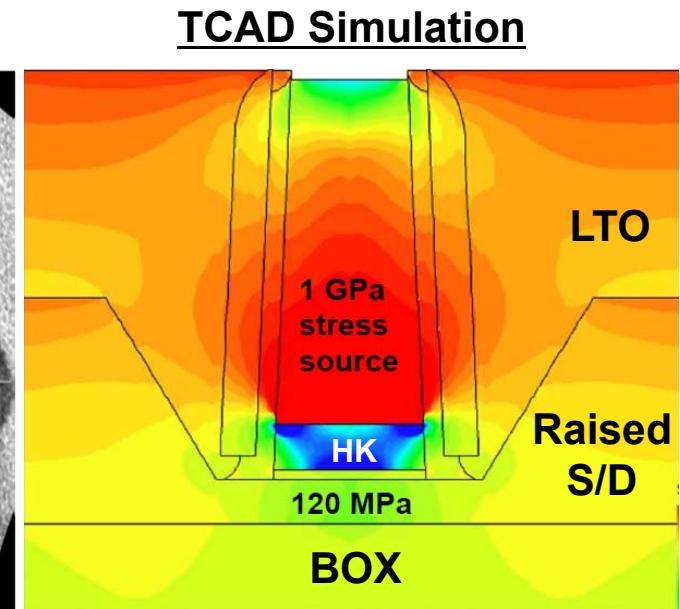
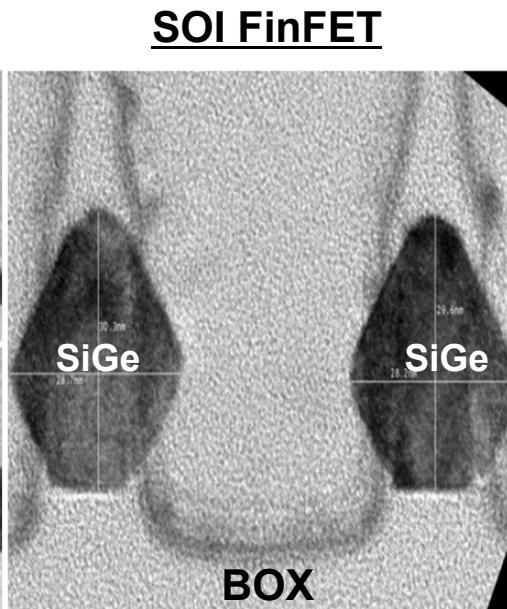
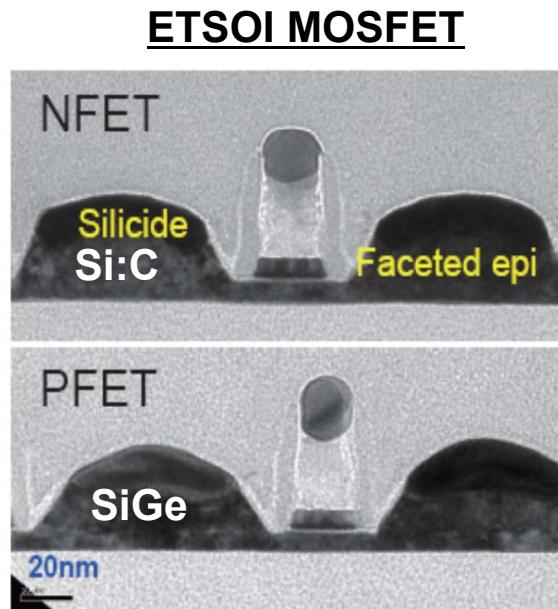
Before gate removal



After gate removal



Impact of Substrate on Channel Strain



K. Cheng, IEDM (2009)

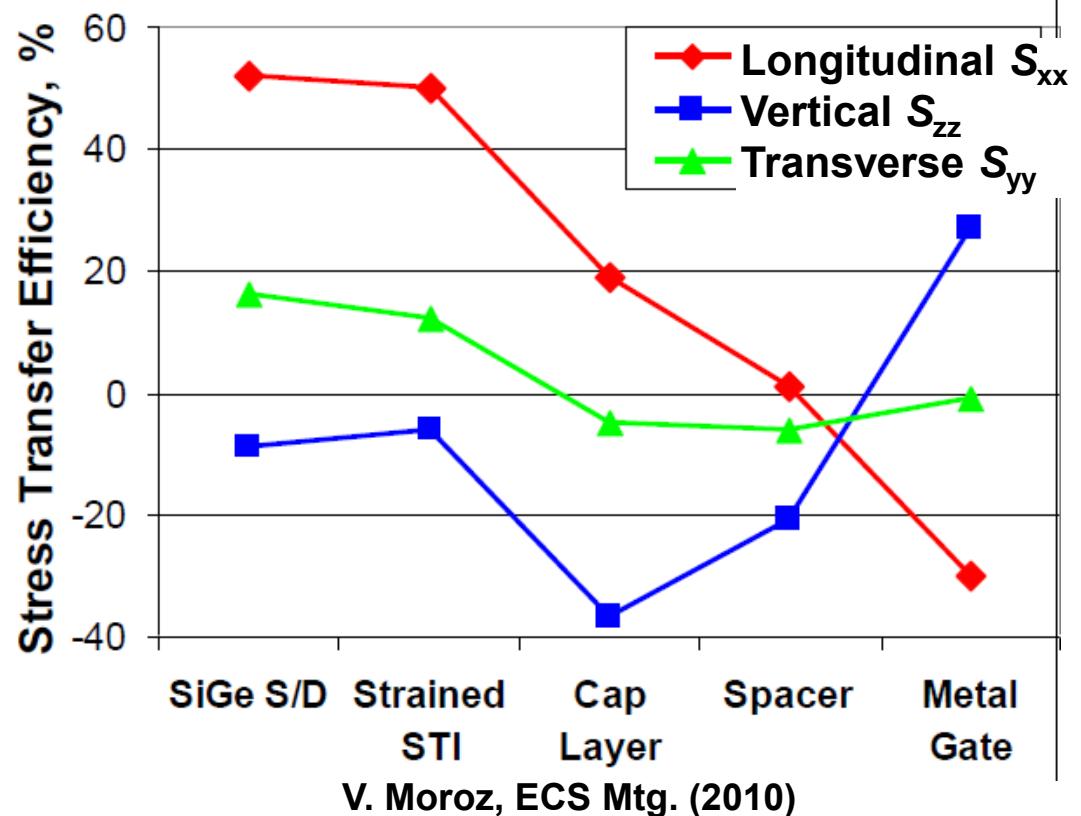
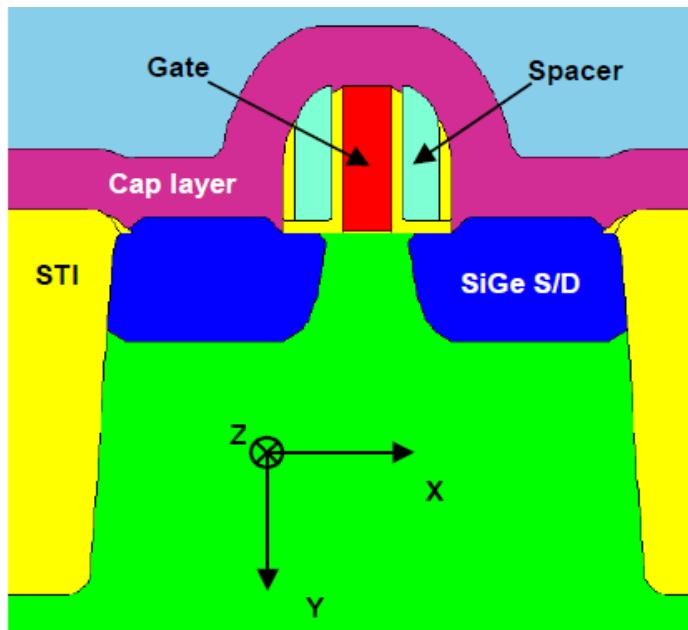
V.S. Basker, VLSI (2010)

V. Moroz, ECS Mtg. (2010)

- SOI MOSFET (planar or Fin-shape) cannot take advantage of the large stressor volume of the embedded Source/Drain.
- BOX region has larger stiffness than Si channel, which lowers the stress transfer efficiency.

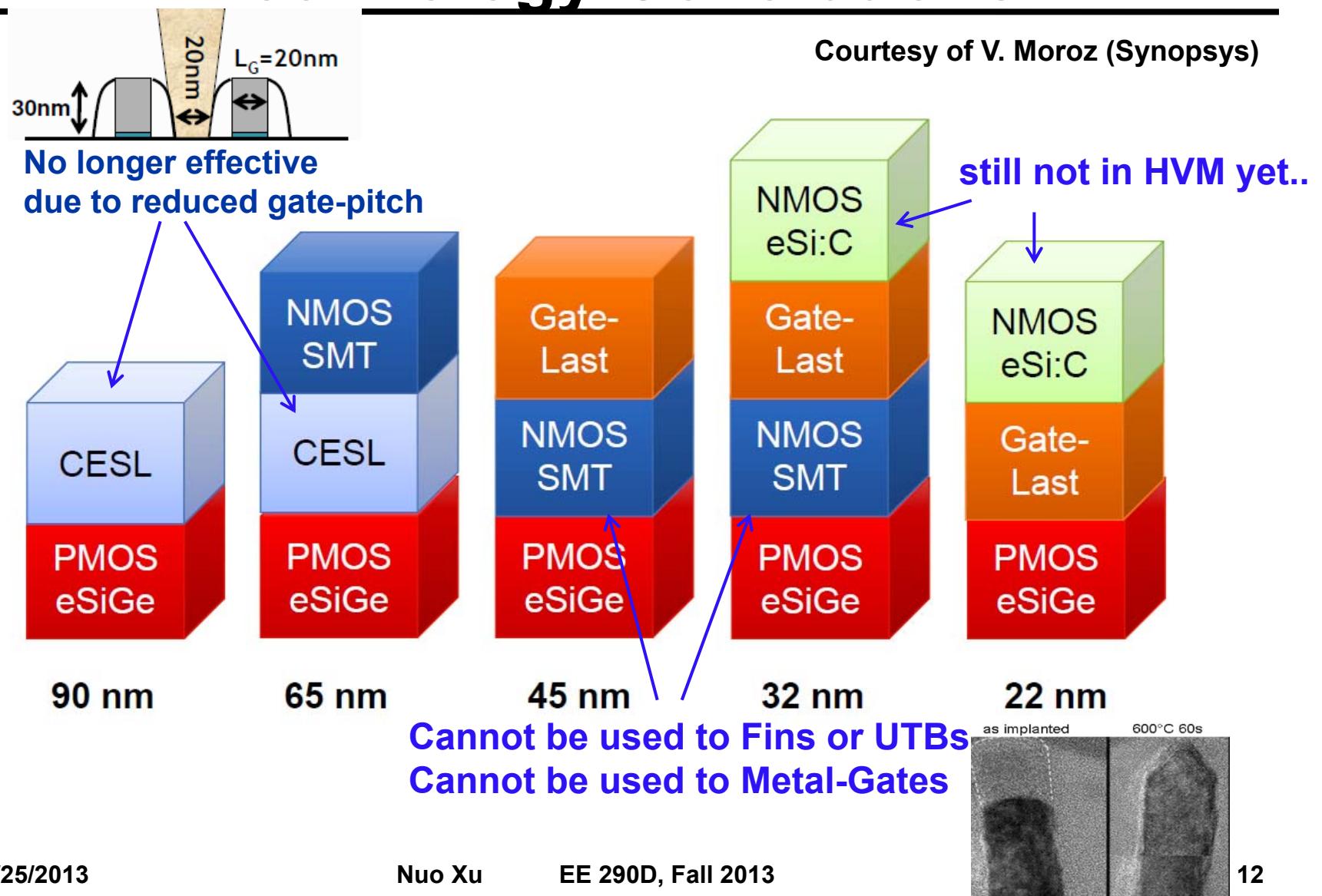
Comparison of Stress Transfer Efficiency (STE)

$$STE \equiv \frac{\text{Final Stress in Channel}}{\text{Initial Stress in Stressor}}$$



- Embedded S/D (S/D SMT or eSiGe) stressor is most effective in longitudinal (x) direction.
- CESL stressor is most effective in vertical (z) direction.
- Transverse stress (S_{yy}) is always very small.

Strained-Silicon Technologies vs. Technology Generations

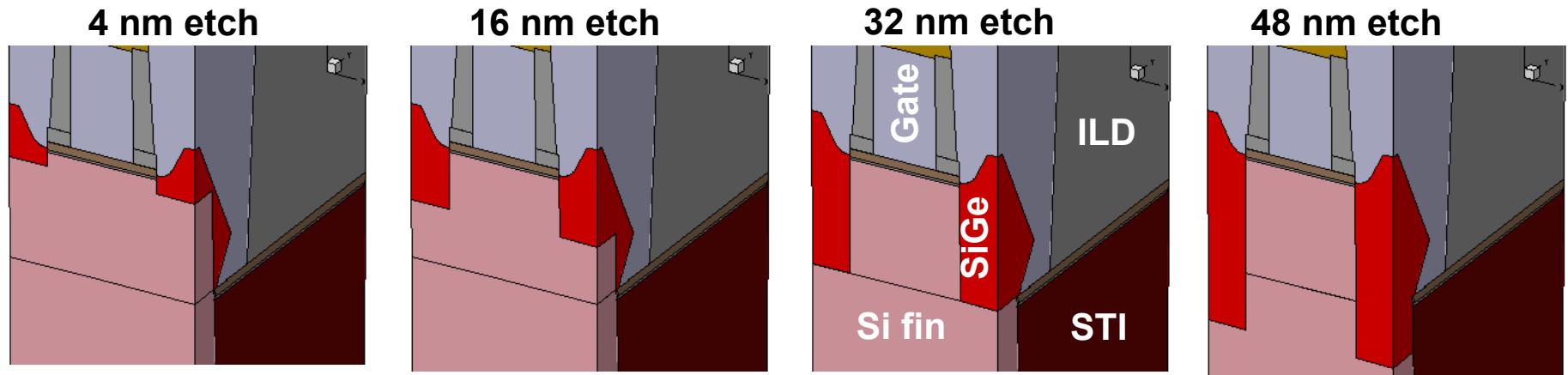


Simulation of Epi-S/D Regrowth with Different Fin Etch

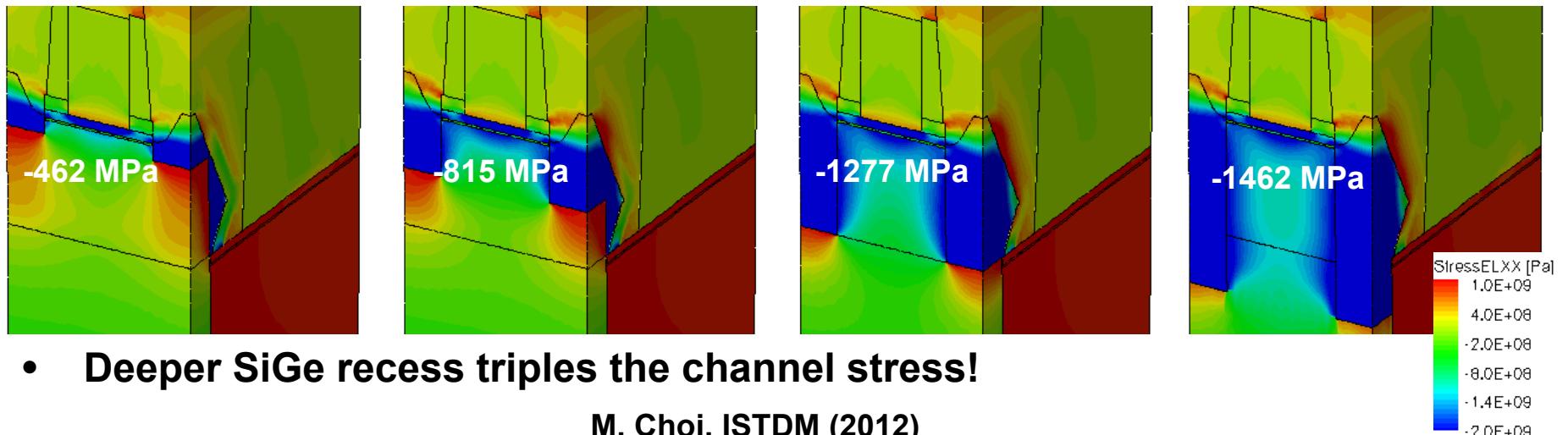
Options \ Time	No fin etch	Half fin etch	Full fin etch	Fin over-etch	Comments
Time 1					Very different shapes at the beginning of epitaxy
Time 2					Still different
Time 3					Now getting similar
Time 4					Now almost identical – the slow growing {111} facets define the shape!

Impact of SiGe-S/D Strain on Fin Etch

$\text{Si}_{0.5}\text{Ge}_{0.5}$ Source/Drain (Intel's 5th-gen strain Si tech.)



Longitudinal Stress (S_{xx})



- Deeper SiGe recess triples the channel stress!

M. Choi, ISTM (2012)

10/25/2013

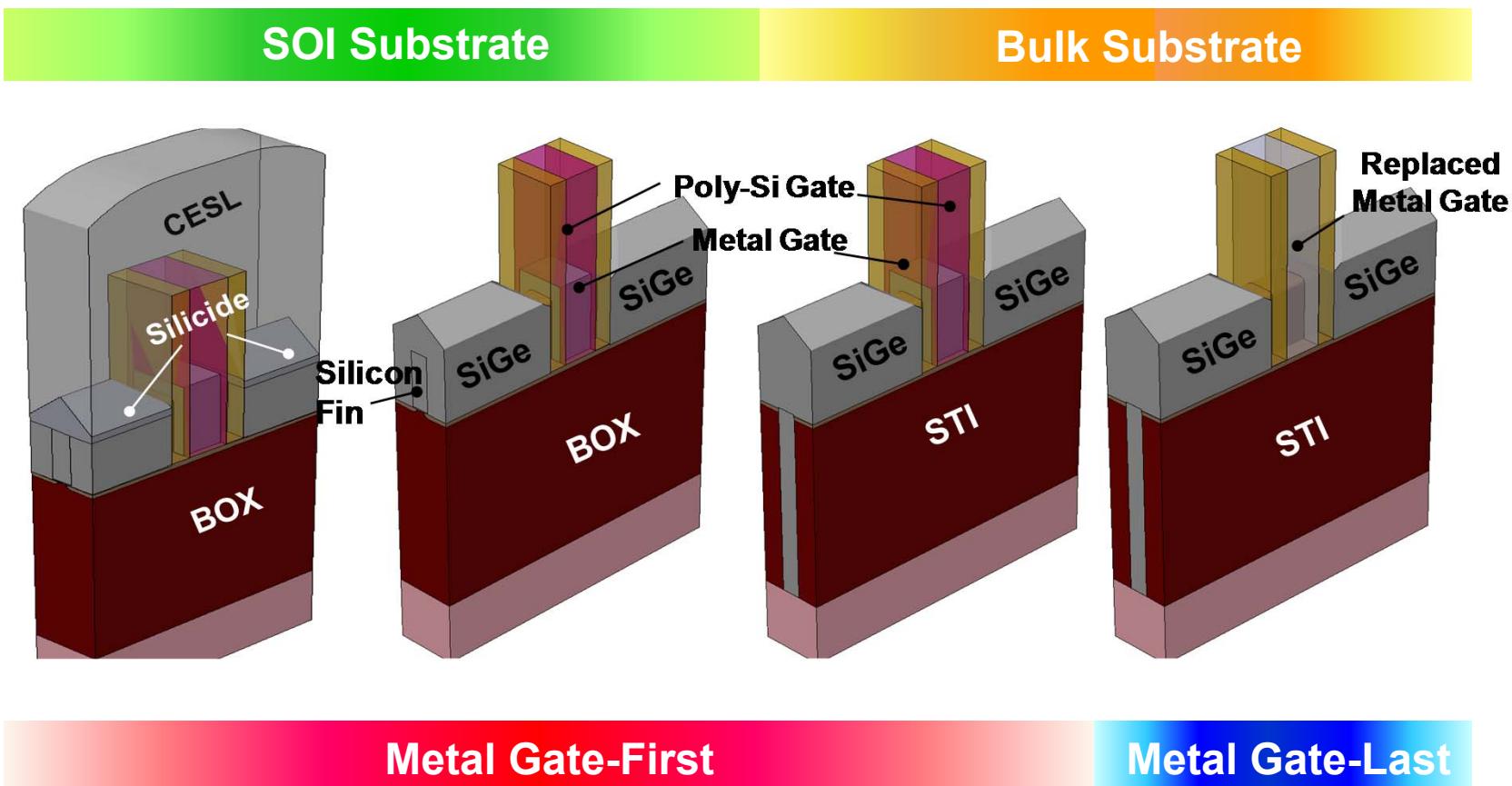
Nuo Xu

EE 290D, Fall 2013

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Strained FinFETs Design Variations

- Various ways to introduce local uniaxial strain in advanced FinFET's process.



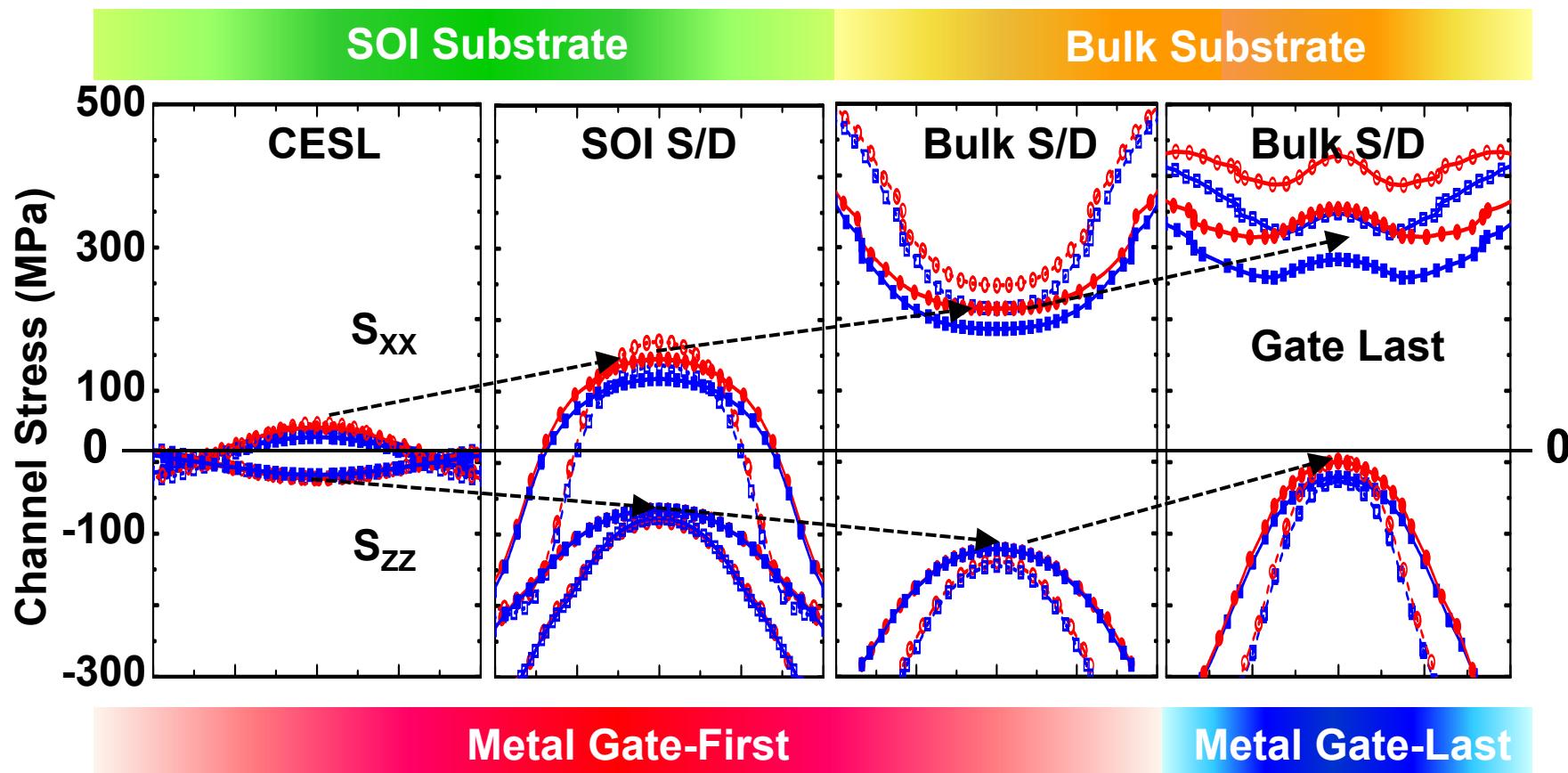
Metal Gate-First

Metal Gate-Last

N. Xu, TED (2012)

Stress in Aggressively scaled FinFETs

- Longitudinal (S_{xx}) and Vertical (S_{zz}) stress profiles along FinFET's channel in 17/12nm node.

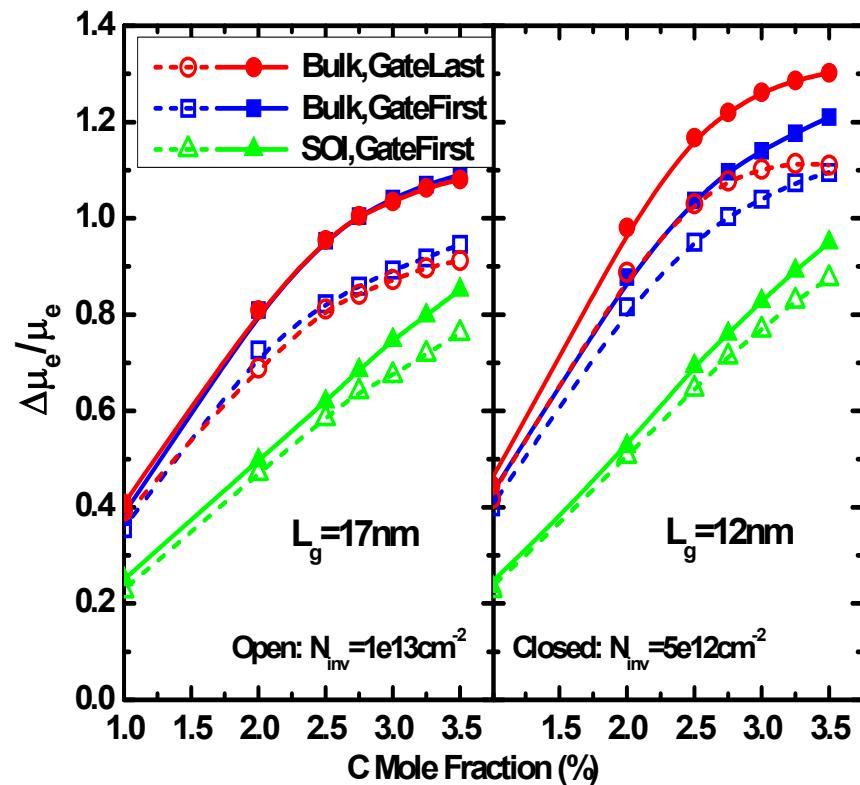


N. Xu, TED (2012)

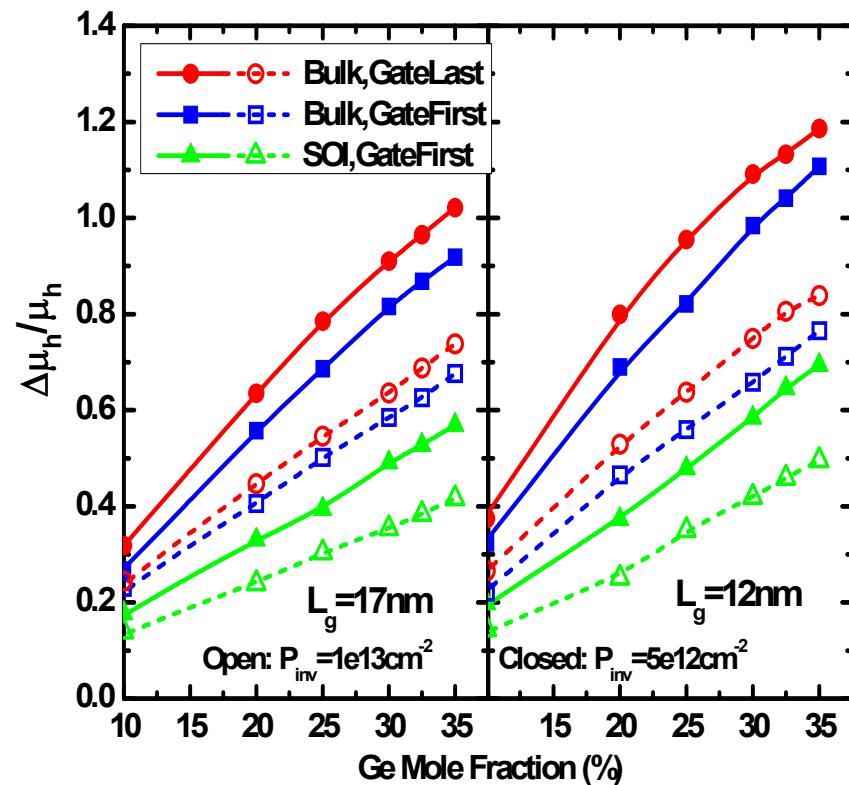
FinFET Carrier Mobility Enhancement with S/D Stressors

- Local uniaxial stress induced by faceted Si:C and SiGe S/D.

N-Channel (Electron)



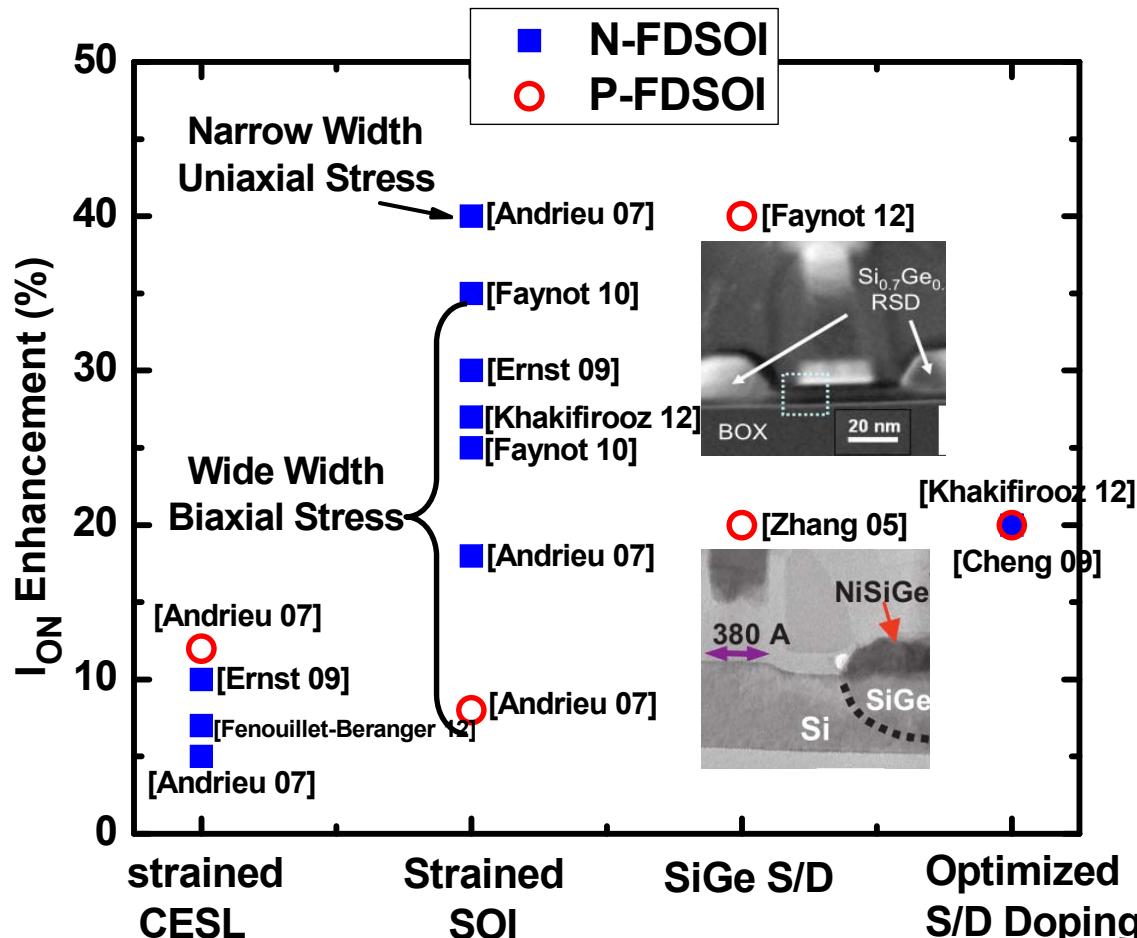
P-Channel (Hole)



N. Xu, TED (2012)

Stress-Induced I_{ON} Enhancement

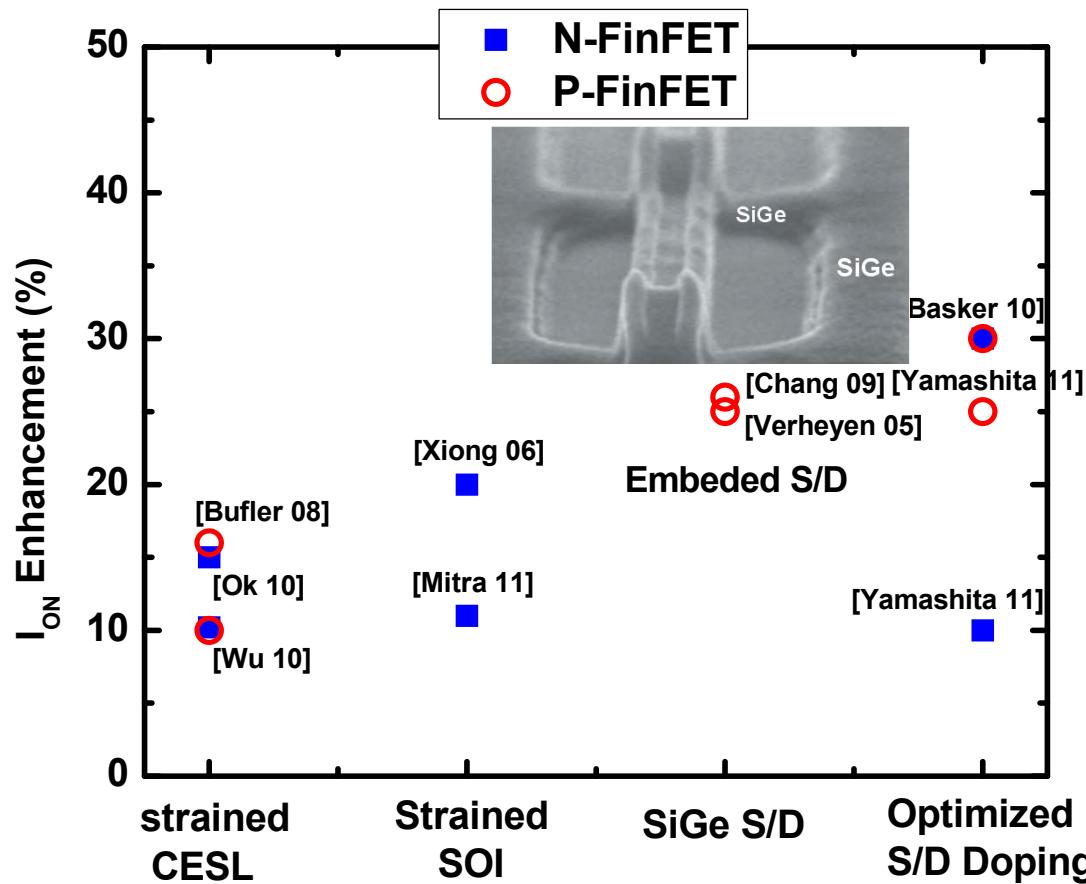
FD-SOI MOSFETs



- sCESL-induced enhancement is small.
- sSOI-induced enhancement is large for narrow-width nMOSFETs.
 - Strain becomes uniaxial after SOI etching
- Embedded-SiGe S/D is not effective unless raised-SiGe S/D is used.

N. Xu, Int. SOI Conf. (2012)

Stress-Induced I_{ON} Enhancement FinFETs

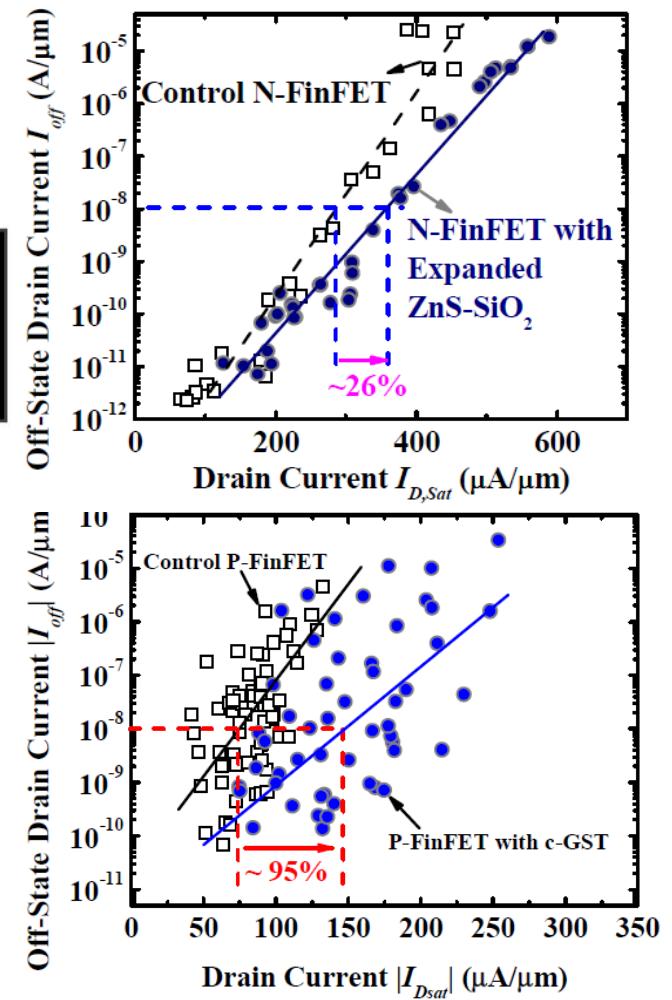
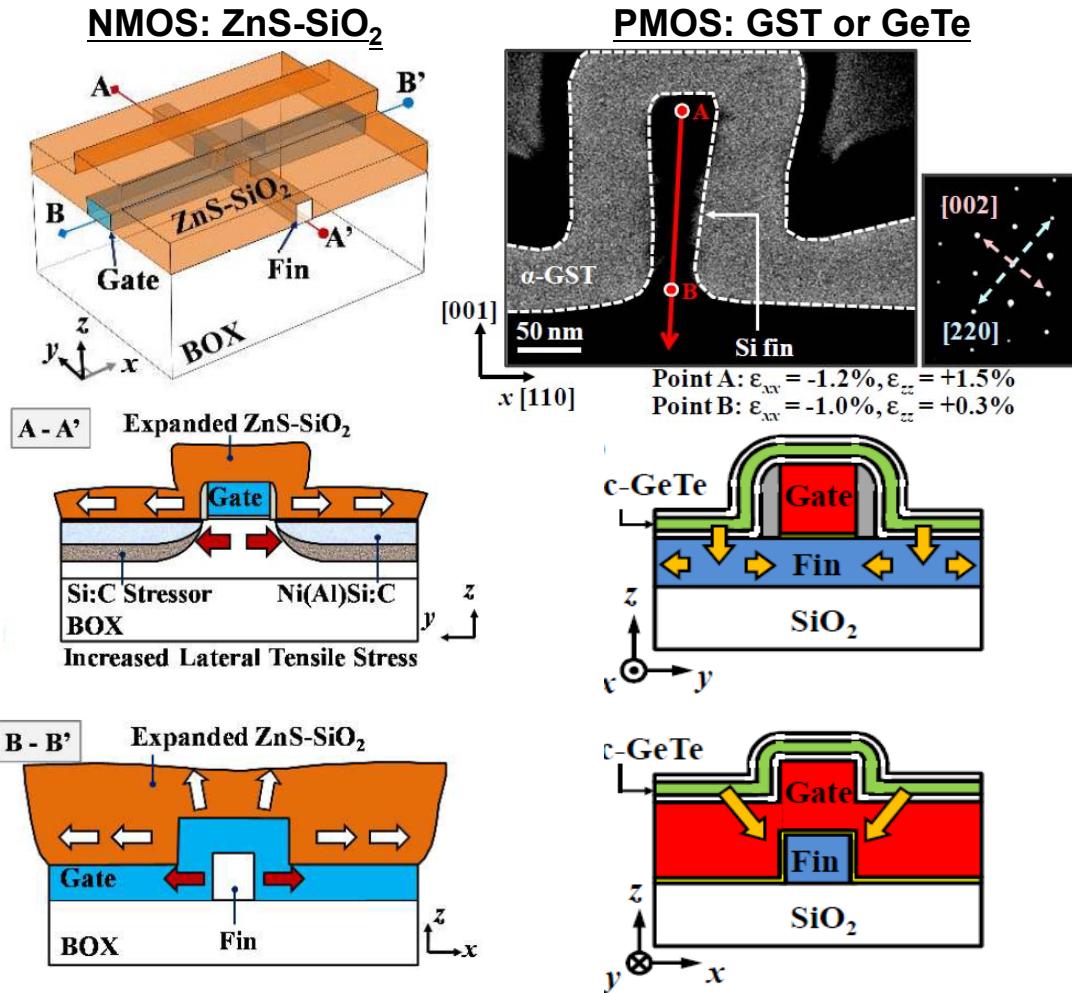


- sCESL and sSOI can provide for significant enhancements.
- Embedded-SiGe S/D is the most effective for p-FinFETs.
- S/D doping must be optimized for maximum strain-enhancement.

N. Xu, Int. SOI Conf. (2012)

Volume-Change Stress Liners - A Way to Extend Strained-Si ?

by Prof. Y.-C. Yeo's group (NUS)



Y. Ding, IEDM (2011) & VLSI-T (2013)
R. Cheng, VLSI-T (2012)

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Planar MOSFET Stressors

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FinFET Stressors

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