

45nm Bulk CMOS Within-Die Variations. Courtesy of C. Spanos (UC Berkeley)

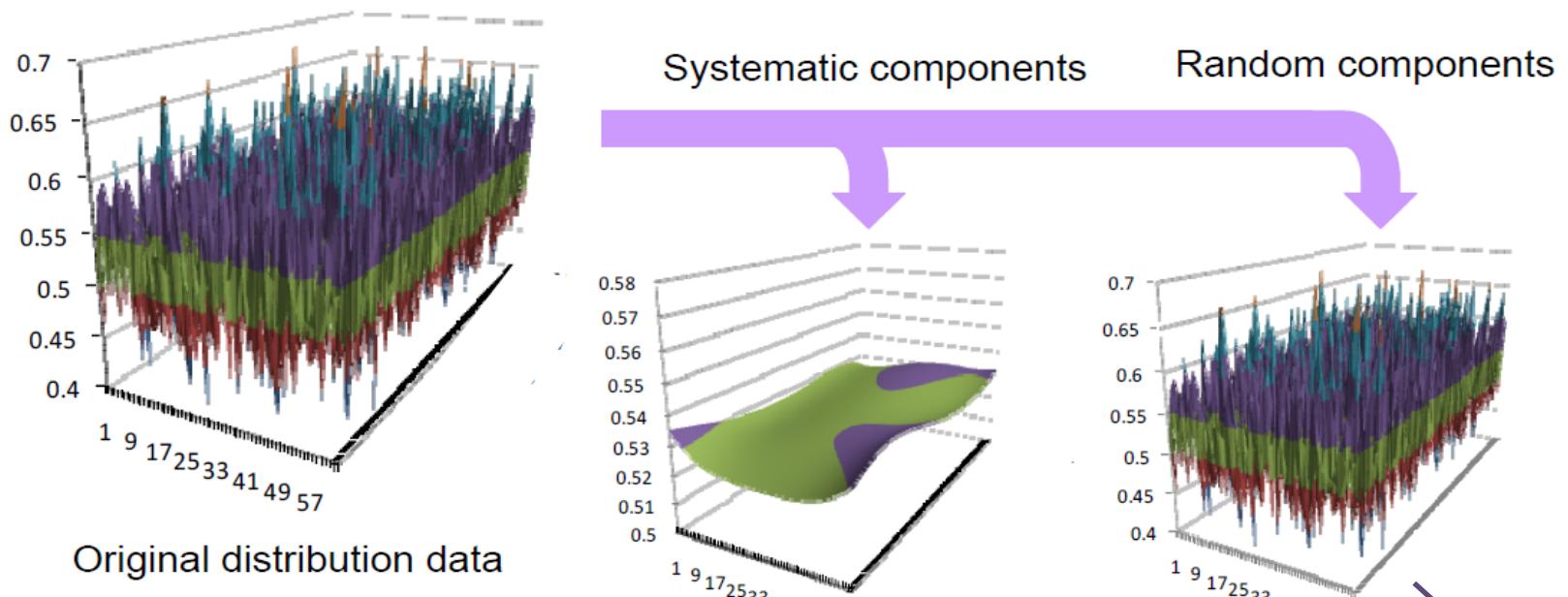
Lecture 11

- **Process-induced Variability I: Random**
 - Random Variability Sources and Characterization
 - Comparisons of Different MOSFET Structures

Reading: multiple research articles (reference list at the end of this lecture)

Device Performance Variability

- An issue for small channel or active region area MOSFETs

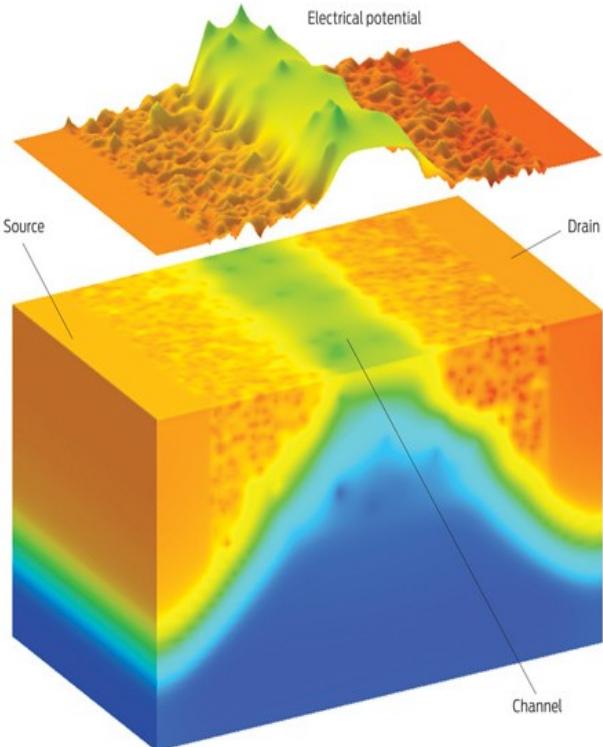


- Layout dependent
- Performance can be predicted

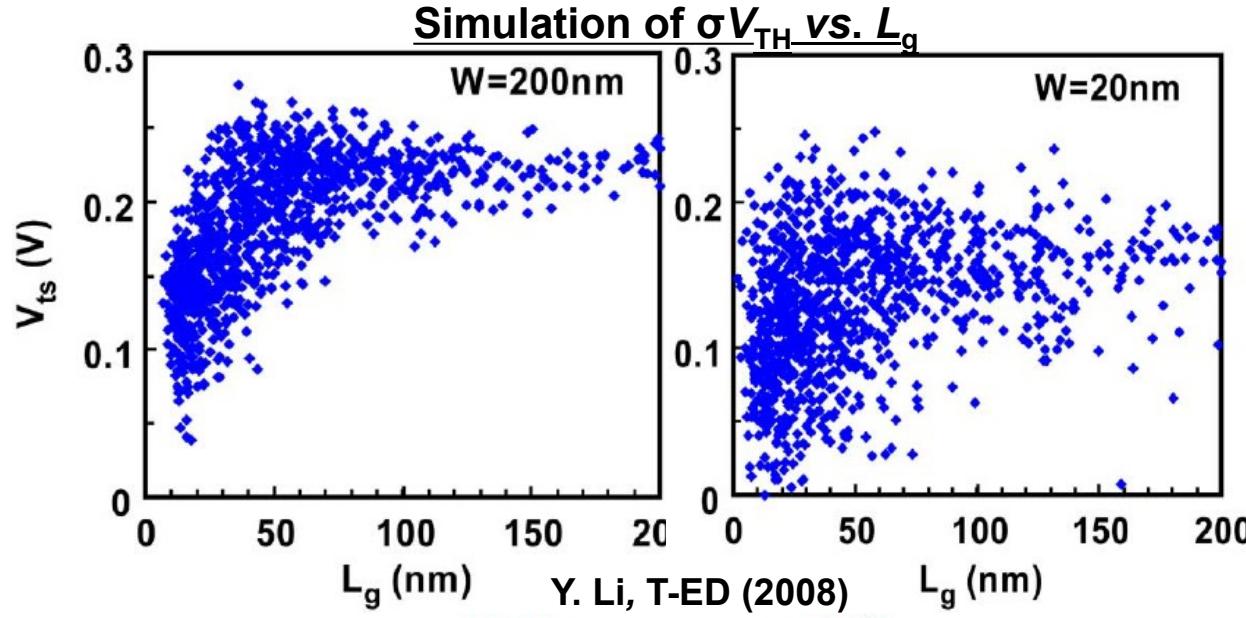
- Less layout dependent
- Only standard deviation can be predicted
- Dominant factor

T. Hiramoto, FD-SOI Workshop (2011)

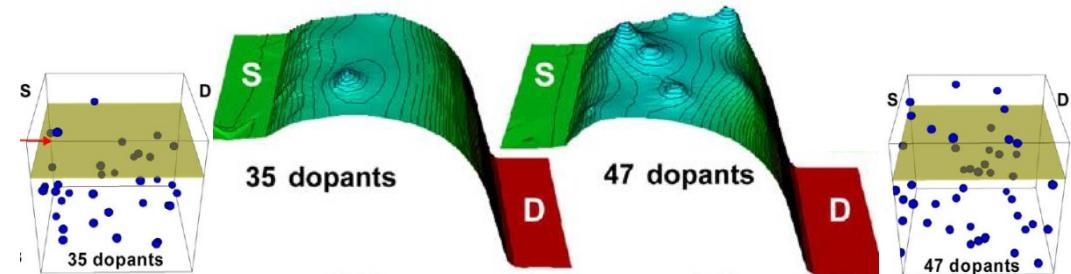
Random Dopant Fluctuations (RDF)



A. Arsenov, T-ED (1998)

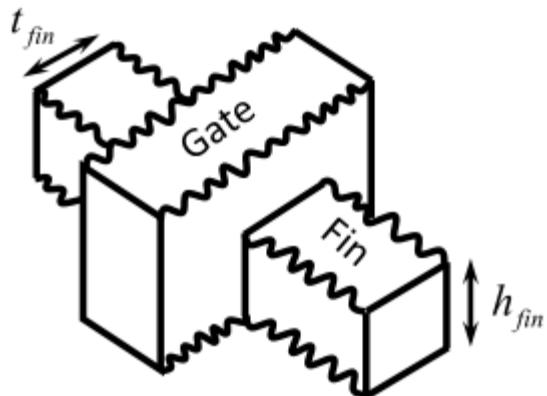
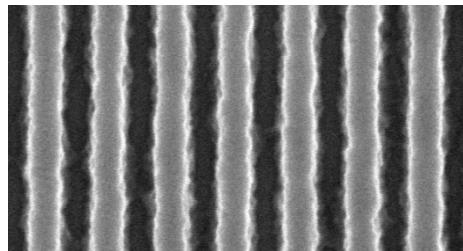


Y. Li, T-ED (2008)

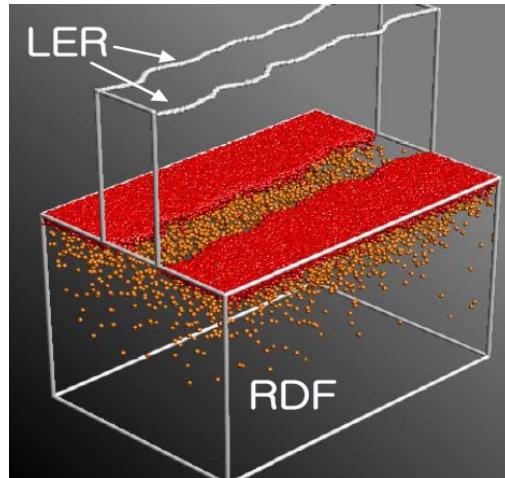


- arises from variations in ion implantation and thermal diffusion
- becomes the dominant factor due to fewer dopants are used in scaled MOSFETs
- causes V_{TH} (lowering) and electrostatics variations

Line Edge Roughness (LER)

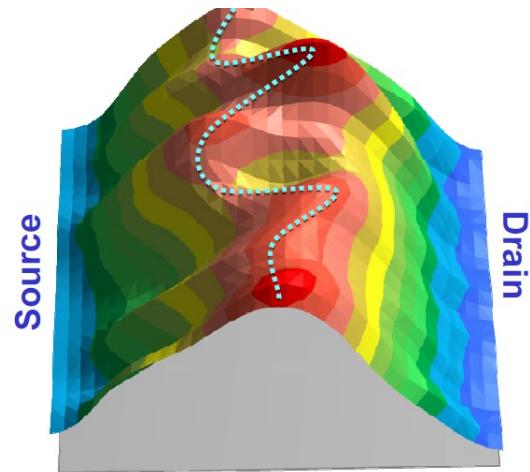


Correlation between
LER and RDF



M. Hane, SISPAD (2003)

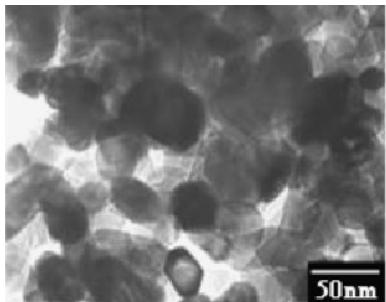
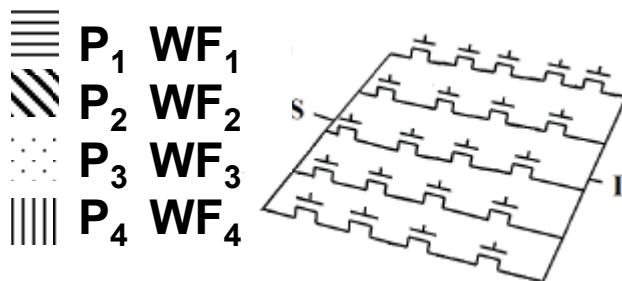
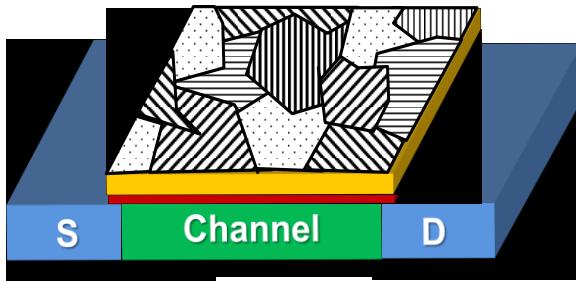
Potential Profiles of a
Narrow Width MOSFET



T. Hiramoto, FD-SOI
Workshop (2011)

- arises from variations in lithography (photons absorption, molecular structure of photoresist) and etching (chemical reactivity of materials)
- causes channel width and gate length variations
- can correlate with RDF to induce more severe L_{eff} and electrostatics variations

Metal Grain Granularity (MGG)

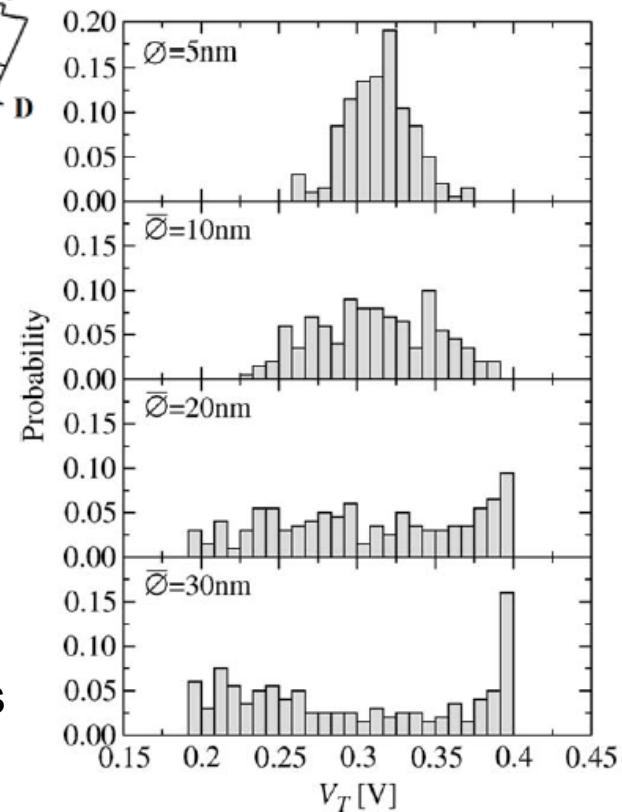


Example: TiN Metal Gate

Orientation	Probability	Work Function
$\langle 200 \rangle$	60%	4.6 eV
$\langle 111 \rangle$	40%	4.4 eV

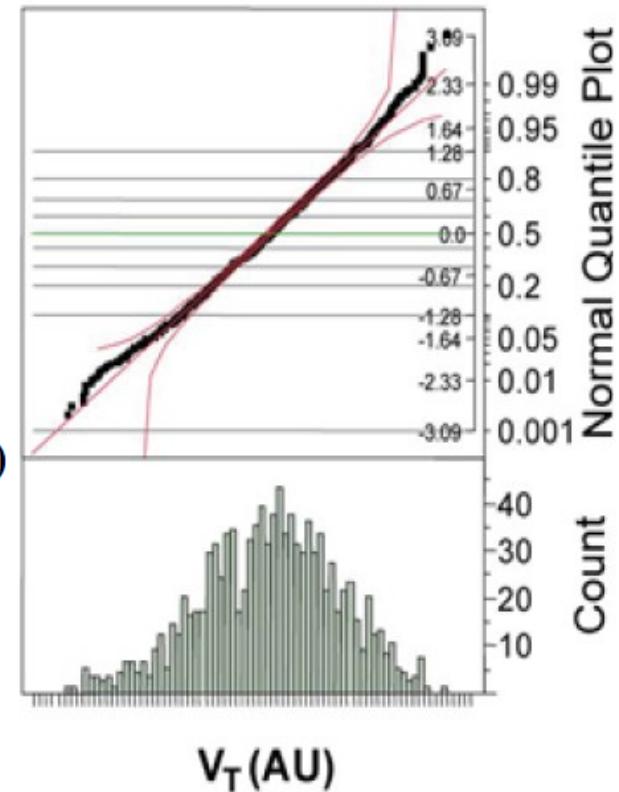
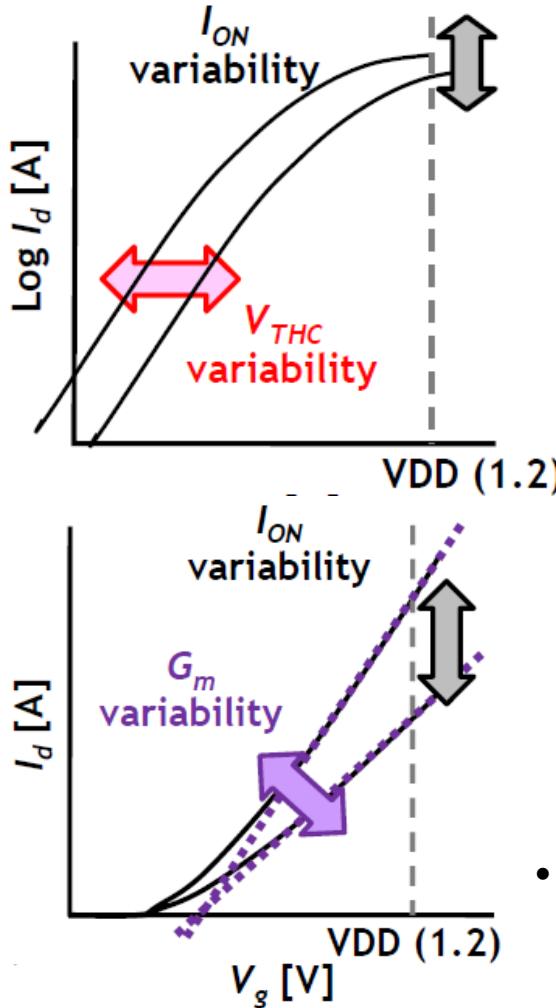
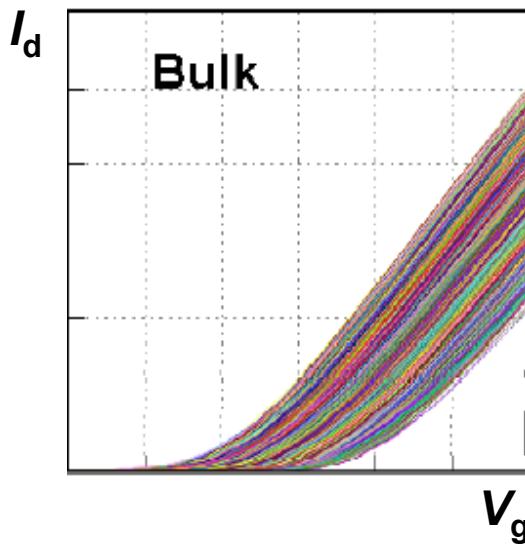
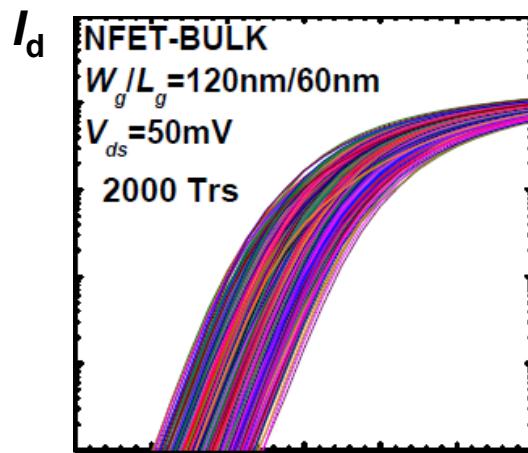
- arises from variations in metal crystallographic orientations during deposition and thermal process
- causes different workfunction values, mainly affects σV_{TH}
- efforts needed for the metal gate engineering

Impact of grain diameter on σV_{TH}



A.R. Brown, EDL (2010)

Performance Variability Analysis

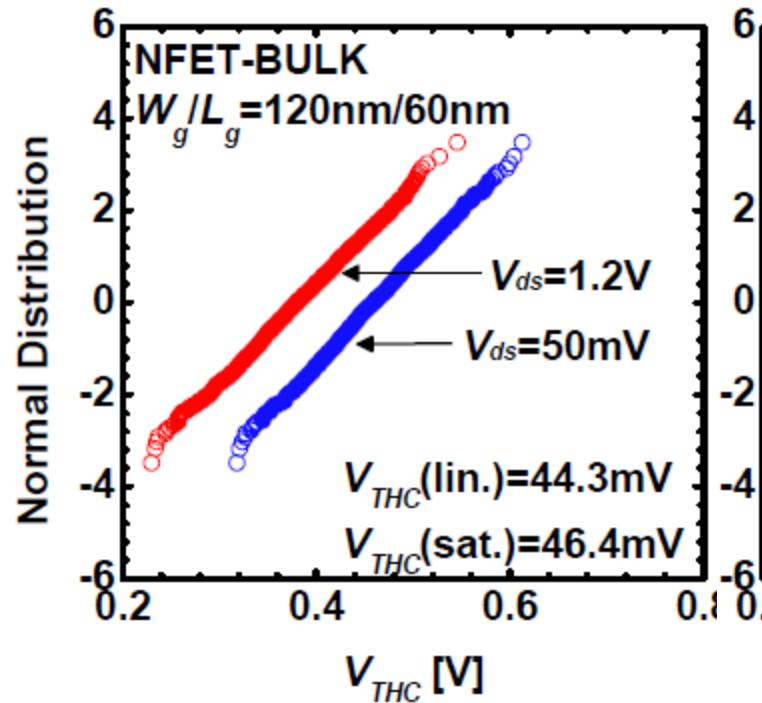


- Performance statistics should show a Gaussian distribution.

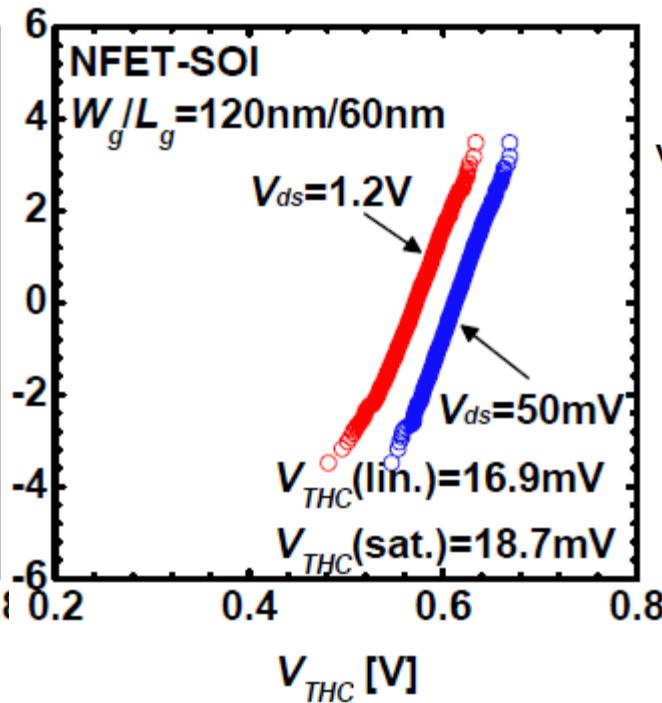
T. Hiramoto, Int. SOI Conf. (2010)

V_{TH} Variability Characterization

Bulk



SOI



MOSFET V_{TH}

$$V_t = V_{FB} + \phi_s + \frac{qN_{sub}W_{DEP}}{C_{inv}}$$

MOSFET σV_{TH}

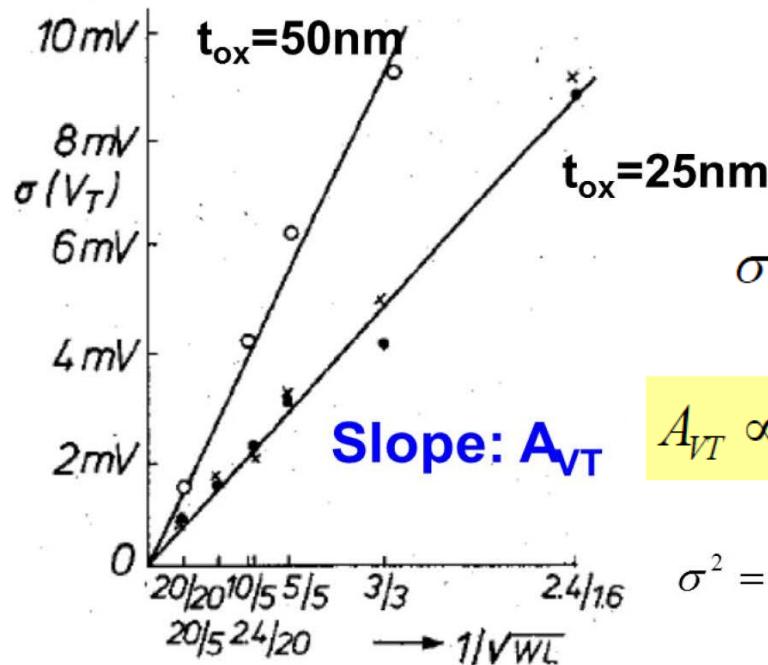
$$\sigma V_t = \frac{q}{C_{inv}} \sqrt{\frac{N_{sub}W_{dep}}{3LW}}$$

$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

- cumulative probability curves
- standard deviation (STD, or σ) and mean value

T. Hiramoto, Int. SOI Conf. (2010)

Pelgrom Plot



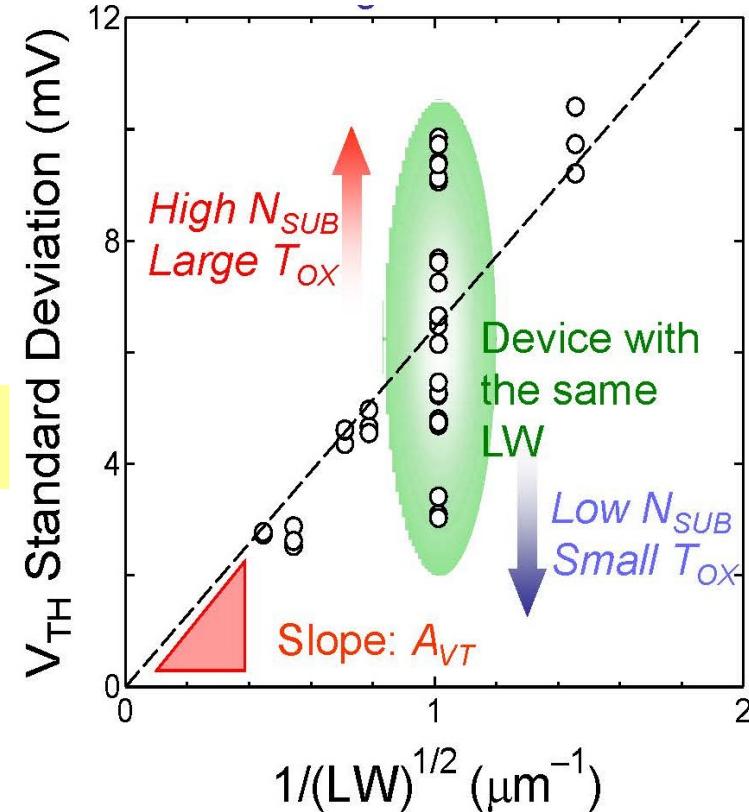
$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

$$A_{VT} \propto t_{INV} \sqrt{N_{SUB} W_{DEP}}$$

$$\sigma^2 = V \left(\frac{x+y}{2} \right)$$

parameter	n-channel s.d.	p-channel s.d.	unit
A_{VT0}	30	35	$\text{mV}\mu\text{m}$
A_β	2.3	3.2	$\%\mu\text{m}$
A_K	16×10^{-3}	12×10^{-3}	$\text{V}^{0.5}\mu\text{m}$
S_{VT0}	4	4	$\mu\text{V}/\mu\text{m}$
S_β	2	2	$10^{-6}/\mu\text{m}$
S_K	4	4	$10^{-6}\text{V}^{0.5}/\mu\text{m}$

M. J. Pelgrom, JSSC (1989)



- Pelgrom plot cannot unify the MOSFET σV_{TH} with different N_{sub} and t_{ox}
- needs a better, universal model!

Takeuchi Plot

$$\sigma_{VTH} = \frac{q}{C_{INV}} \sqrt{\frac{N_{SUB}W_{DEP}}{3LW}}$$



$$= \sqrt{\frac{q}{3\epsilon_{OX}}} \sqrt{\frac{T_{INV}(V_{TH} - V_{FB} - 2\phi_F)}{LW}}$$



$$\sigma_{VTH} = B_{VT} \times \sqrt{\frac{T_{INV}(V_{TH} - V_{FB} - 2\phi_F)}{LW}}$$

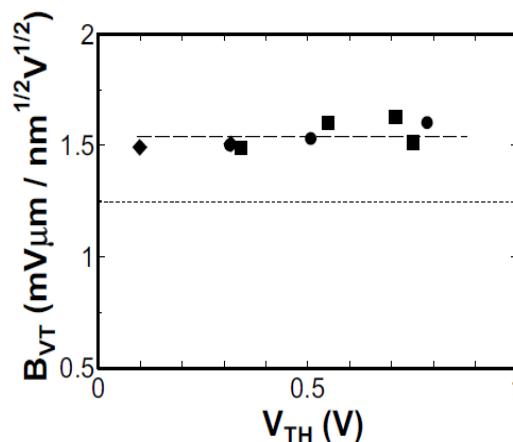
Where, $B_{VT} = \sqrt{\frac{q}{3\epsilon_{OX}}}$

$$V_{TH} = V_{FB} + 2\phi_F + \frac{qN_{SUB}W_{DEP}}{C_{INV}}$$

$$\frac{qN_{SUB}W_{DEP}}{C_{INV}} = V_{TH} - (V_{FB} + 2\phi_F) = V_{TH} + 0.1$$

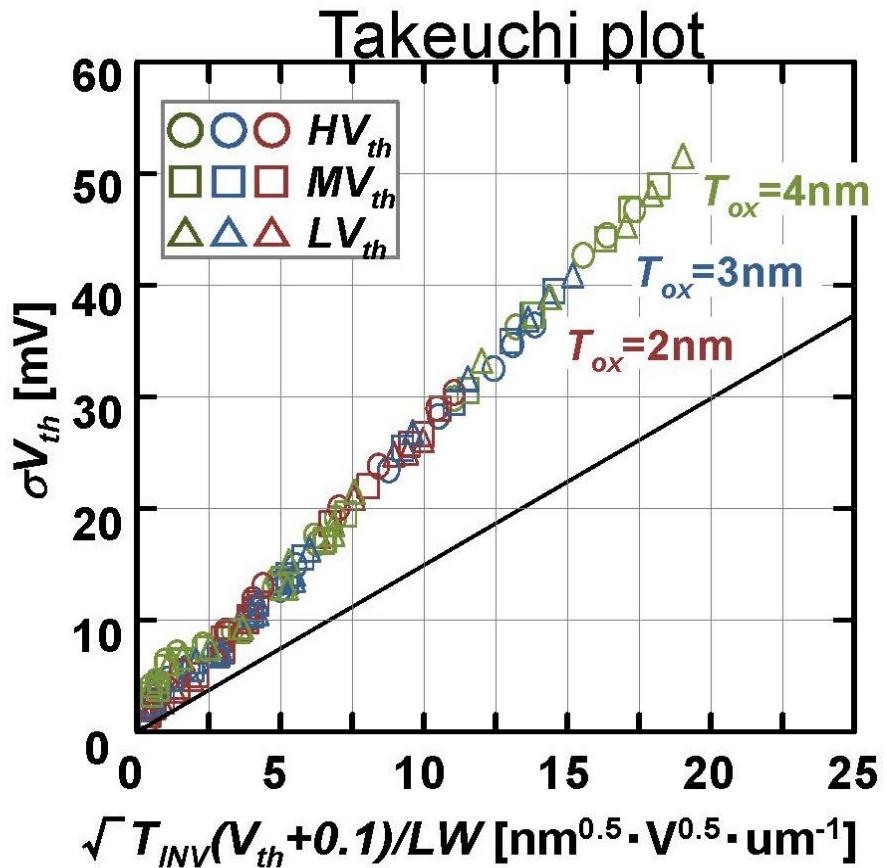
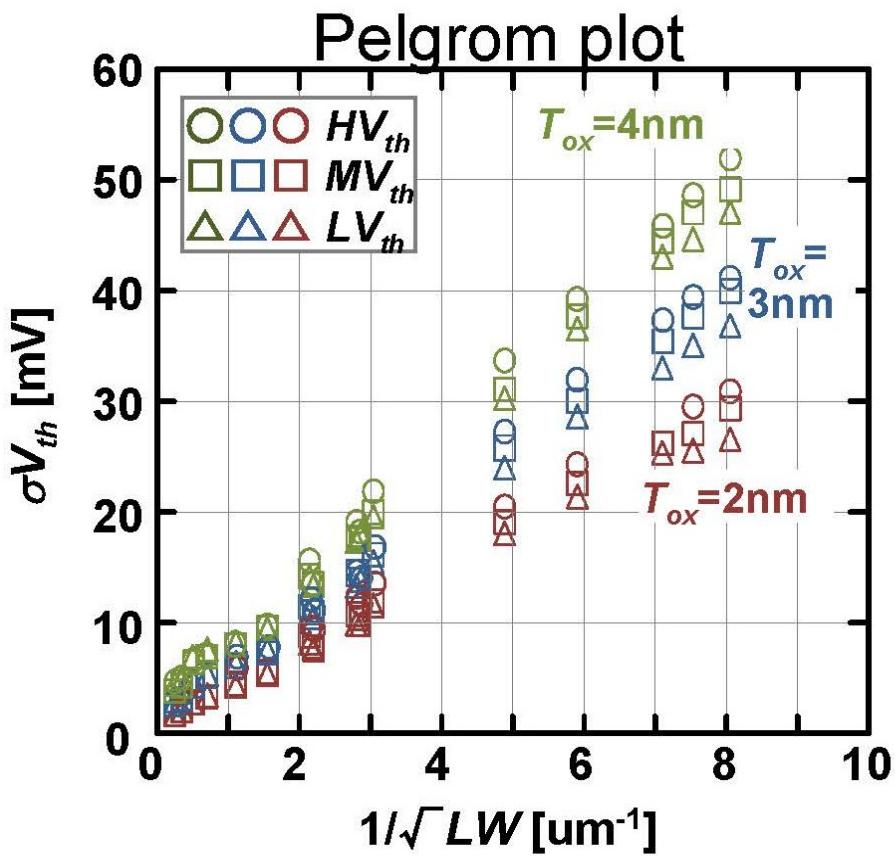
Determined by
Impurities

-0.1V for poly-Si gate.
It varies in metal gate



K. Takeuchi,
IEDM (2007)
& SISPAD
(2009)

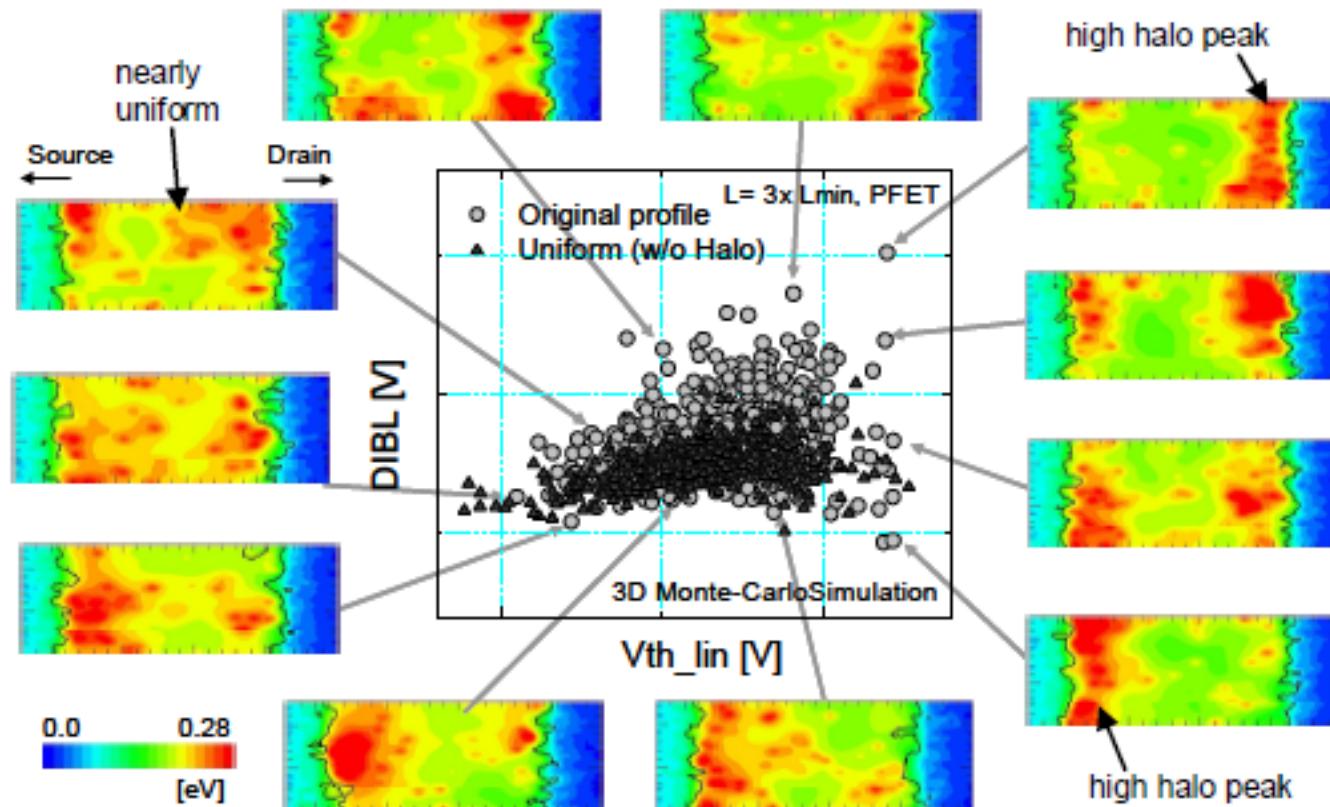
Pelgrom Plot vs. Takeuchi Plot



- Takeuchi plot shows more physical insight on the variability “magnitude”, by decoupling the impact of V_{TH} .

T. Tsunomura, VLSI-T (2008)

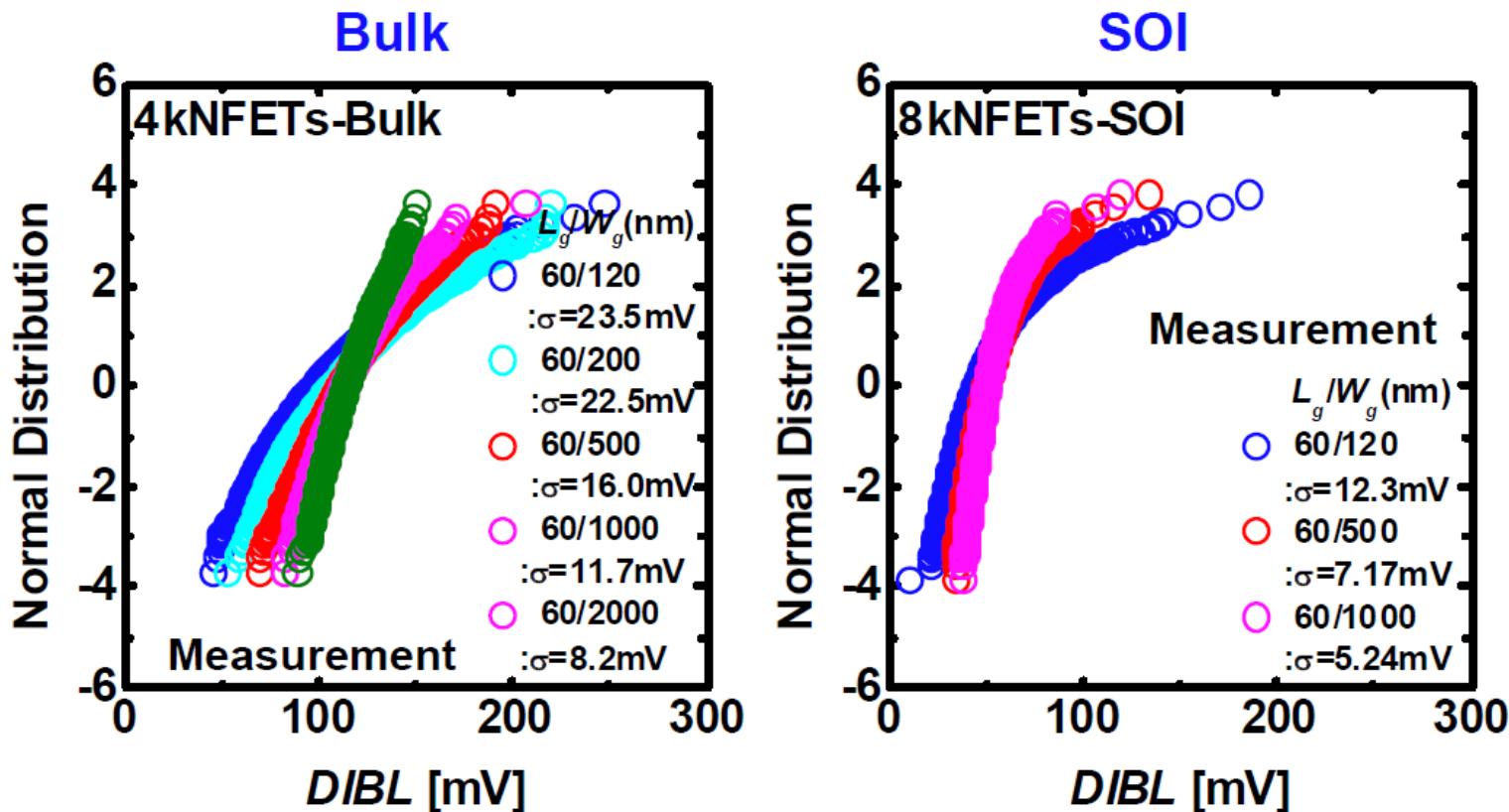
DIBL Variability Origins



- Due to the asymmetric potential (E -field) distributions in a MOSFET channel, any changes on S/D doping will induce DIBL variations.

M. Miyamura, IEDM (2008)

DIBL Variability Characterization

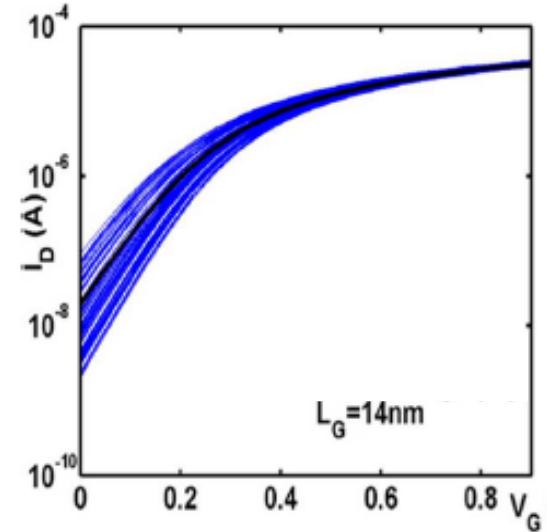


- Mean value of DIBL is determined by MOSFET's electrostatic integrity.
- Standard deviation of DIBL is determined by RDF+LER variations.

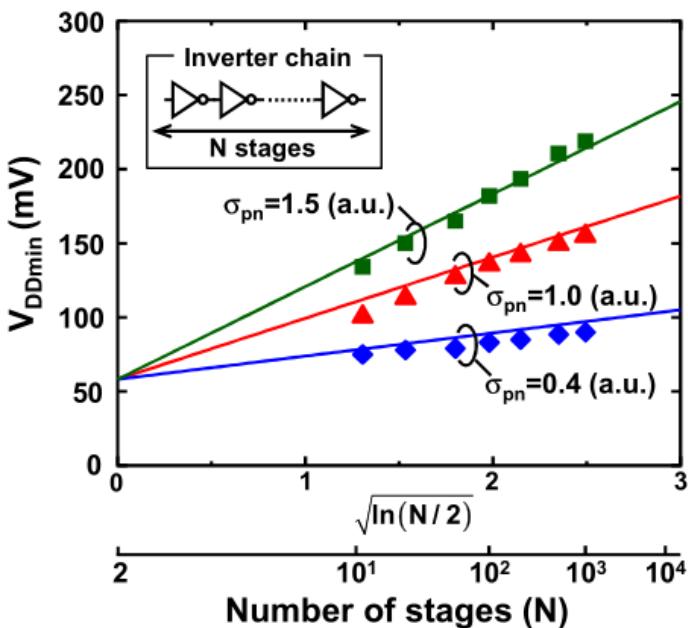
T. Hiramoto, Int. SOI Conf. (2010)

Impact of Random Variability on Circuit Performance

N-MOSFETs

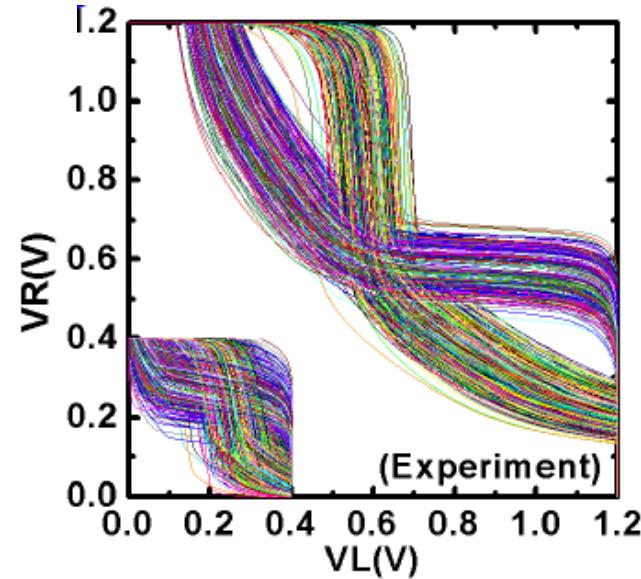


Deep Logic Circuits



H. Fuketa, IEDM (2011)

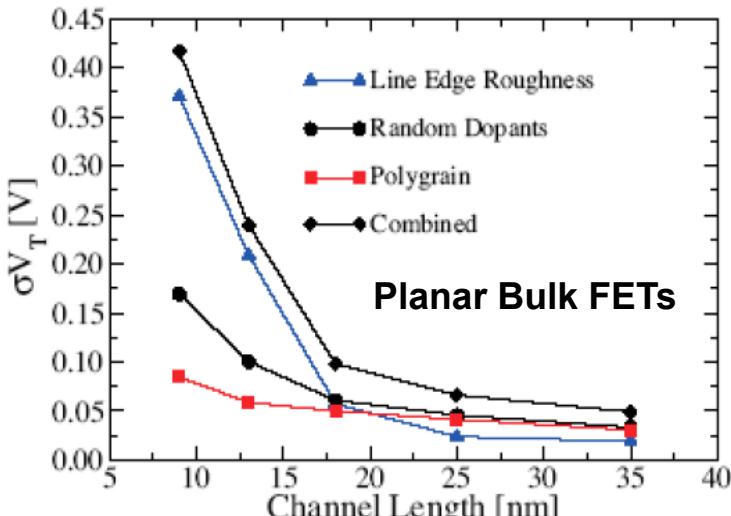
6T SRAMs



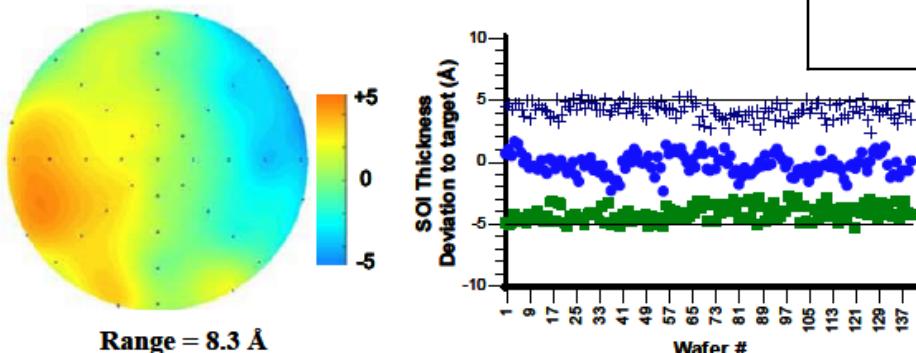
T. Hiramoto, FD-SOI
Workshop (2011)

- Performance variations (dominated by σV_{TH}) cause devices and circuits leakage power increase and limit the V_{DD} scaling.

Planar MOSFETs Random Variability



A. Arsenov, VLSI-T (2007)

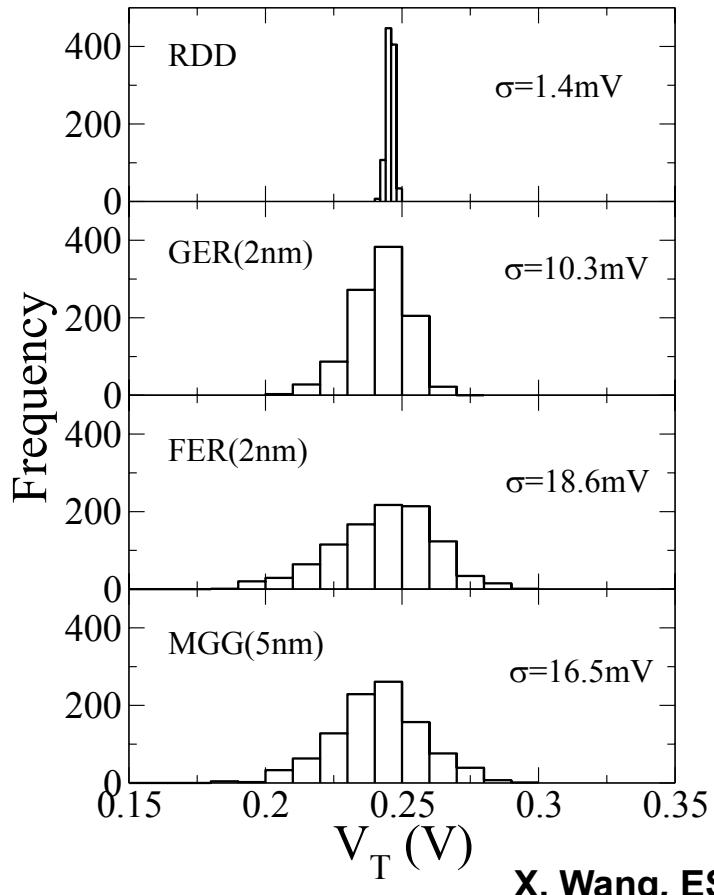
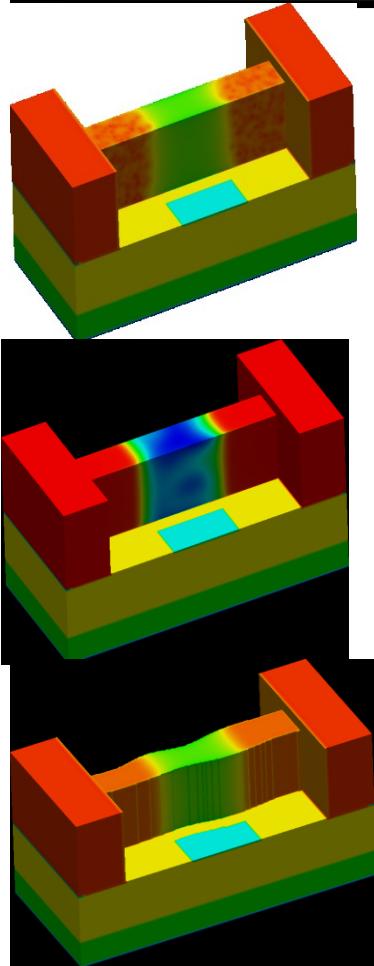


Source: Soitec inc.

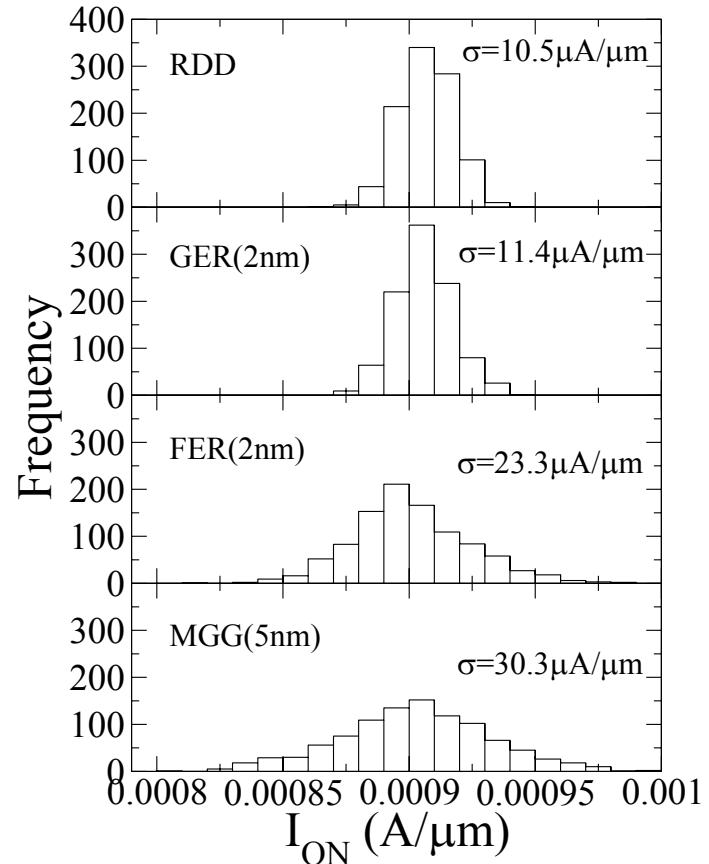
Sources	Technology Solutions
RDF	<ul style="list-style-type: none"> • Retrograde-Well Doping • Co-implantation to mitigate Transient Enhanced Diffusion
LER	<ul style="list-style-type: none"> • Double Patterning Approach (Spacer Lithography)
MGG	<ul style="list-style-type: none"> • Gate Last Process • Metal Material Engineering
All	<p style="color: blue;">Use thin-body MOSFETs to improve electrostatics!</p>

- State-of-the-art UTB FD-SOI MOSFET can achieve very uniform Si film thickness
 - excellent variability behaviors

FinFET's Random Variability



X. Wang, ESSDERC (2012)

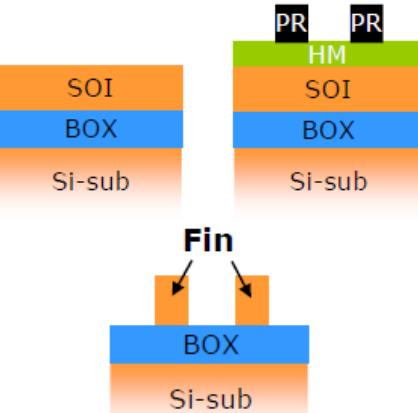


- LER (GateER and FinER) and MGG dominate the variability.
- RDF induced larger I_{on} variation than the proportion in V_{TH} fluctuation.

Bulk vs. SOI FinFETs' Variability: Geometry Fluctuations

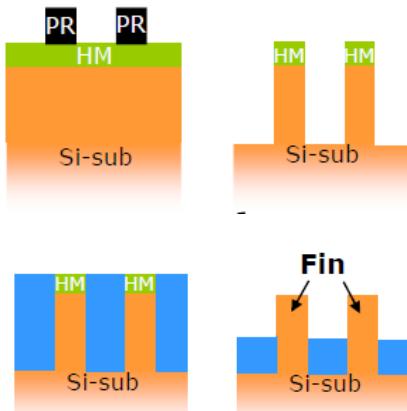
Source: SOI Consortium

SOI FinFET



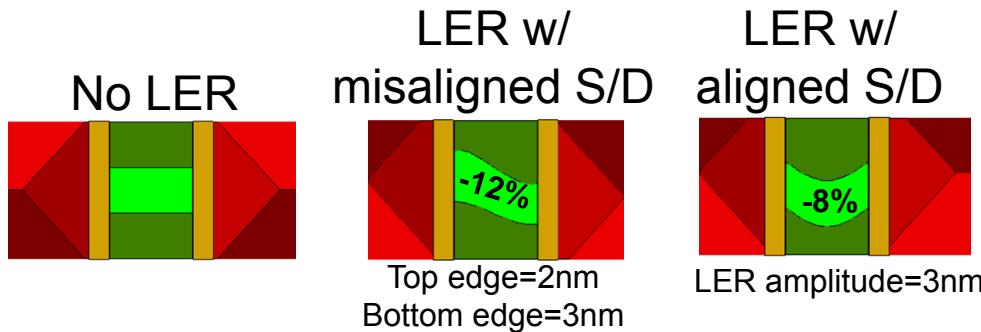
Sources of Variability	Unit	Nominal	3-sigma Tolerance (current)	3-sigma Tolerance (future)	
SOI Layer	nm	70	2	1	5% 3sigma SOI thickness variability with future improvements in high volume manufacturing
Hardmask dep	nm	10	1	0.5	10% cross-wafer 3sigma
Fin Etch	nm	70	4.2	2.1	5% cross wafer + 1% overetch
Corner rounding	nm	2	0.1	0.05	
Total fin height variability (nm)		4.8	2.4		Root sum-square of all sources of variability
Total fin width variability (nm)		1.0	0.5	In 32nm technology, active area CD variability is 15nm across iso-dense patterns, multiple pitches and RIE overetch from variability in vertical layers. For FinFETs, most of the CD variability is expected to come from the overetch to account for thickness variability in Fin definition since the pitch will be fixed. Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability.	

Bulk FinFET



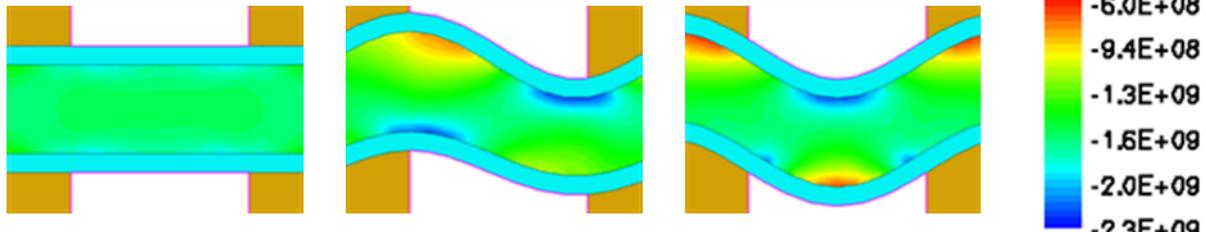
Sources of Variability	Unit	Nominal	3-sigma Tolerance (current)	3-sigma Tolerance (future)	
HM oxide	nm	8	0.4	0.2	5% 3sigma variation for oxide
HM nitride	nm	70	7	3.5	10% 3sigma variation for deposited nitride
Trench etch	nm	170	8.5	4.25	5% 3sigma from trench etch based on 32nm data
Oxide recess	nm	100	5	2.5	Oxide dry/wet etch with no etch stop. 100nm oxide etchback for 70nm fin height assumed.
Pad oxide	nm	2	0.1	0.05	
Well anneal	nm	0	3	1.5	3sigma variability in junction depth from angled implants
Total fin height variability (nm)		12.5	6.2		Root sum-square of all sources of variability
Total fin width variability (nm)		2.5	1.2	Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability. See previous slide for more details on fin width variability.	

Fin LER-induced Strain Variability



- Average channel stress degrades with fin curvature

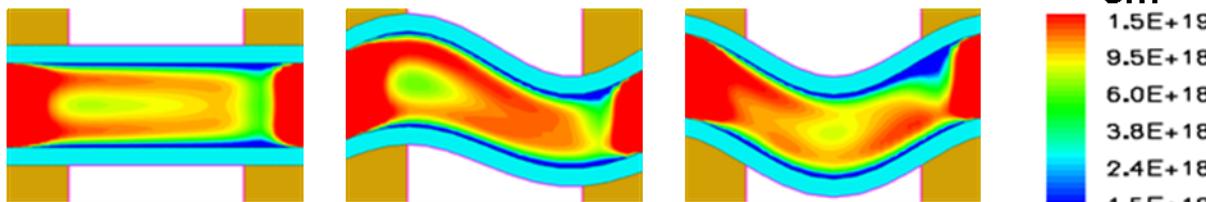
Longitudinal stress



Pa

-6.0E+08
-9.4E+08
-1.3E+09
-1.6E+09
-2.0E+09
-2.3E+09

Hole density



cm^{-3}

1.5E+19
9.5E+18
6.0E+18
3.8E+18
2.4E+18
1.5E+18

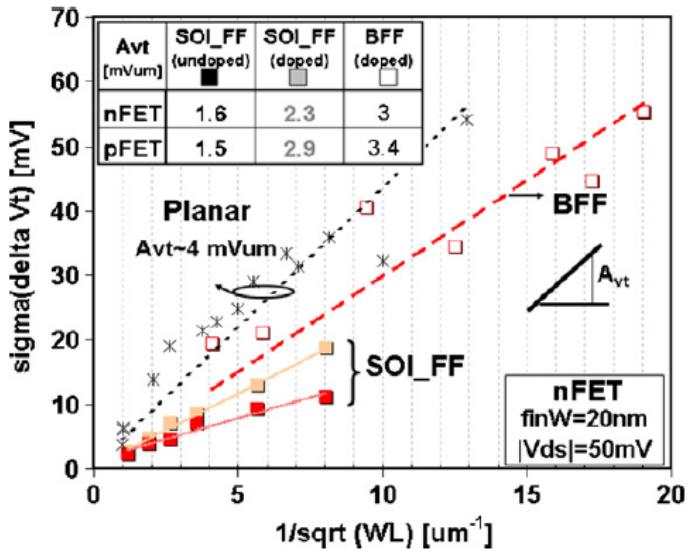
On-state Bias: $V_{gs}=V_{ds}=V_{DD}$

- Stress distribution changes inside the channel are bigger for LER fin.
- Most carriers move along the fin curvature.
 - the longer L

M. Choi, ISTD (2012)

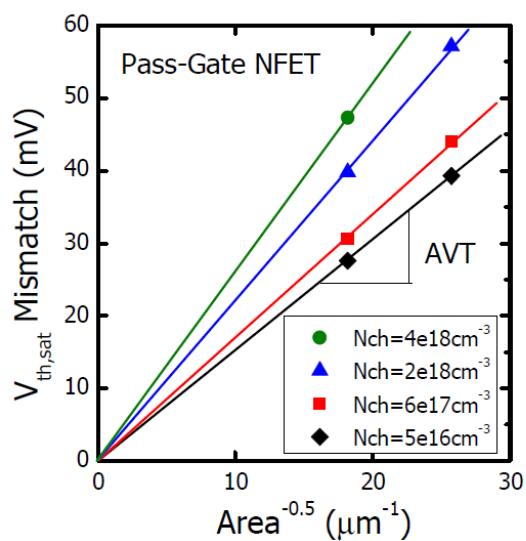
FinFET's RDF

Bulk & SOI FinFETs' Pelgrom Plots

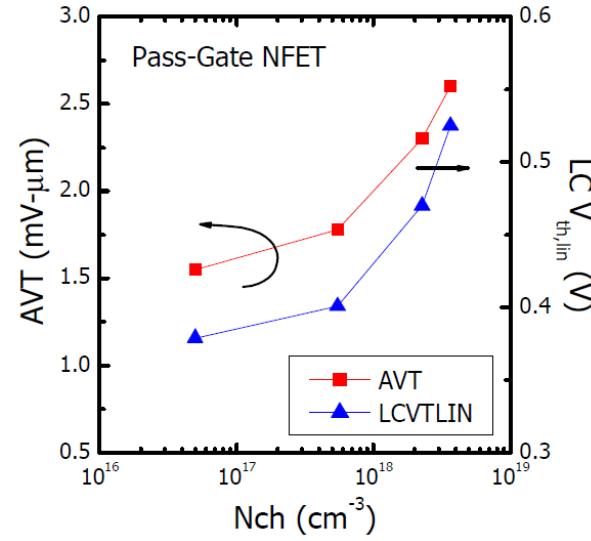


T. Chiarella, SSE (2010)

V_{TH} variations from the PassGate N-FinFETs



C.-H. Lin, VLSI-T (2012)



- The multiple doping profiles existed in a bulk FinFET (*i.e.* retrograde-well or/and HALO) generate large RDF, compared to a SOI FinFET.
- The A_{VT} of a FinFET will be comparable to a planar bulk MOSFET's once the fin doping concentration exceeds $2\text{e}18\text{cm}^{-3}$.

References

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3. Y. Li *et al.*, “Discrete Dopant Fluctuations in 20-nm/15-nm Gate Planar CMOS,” *IEEE Transactions on Electron Devices*, vol.55, no.6, pp.1449-1455, 2008.
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5. A.R. Brown *et al.*, “Impact of Metal Gate Granularity on Threshold Voltage Variability A Full-Scale Three-Dimensional Statistical Simulation Study,” *IEEE Electron Device Letters*, vol.31, no.11, pp.1199-1201, 2010.
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16. T. Chiarella *et al.*, “Benchmarking SOI and Bulk FinFET Alternatives for Planar CMOS Scaling Succession,” *Solid-State Electronics*, vol.54, pp.855-860, 2010.