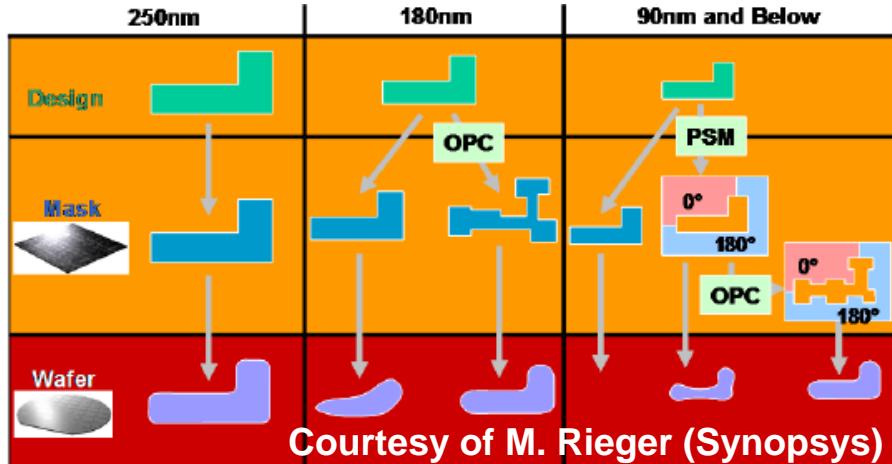


Lecture 12

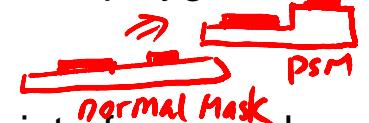
- **Process-induced Variations II: Systematic**
 - Lithographic Proximity Effect
 - Layout Dependent Strain
 - Well Proximity Effect

Reading: multiple research articles (reference list at the end of this lecture)

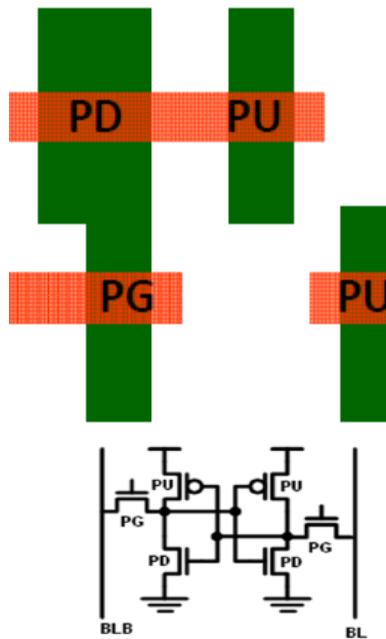
Lithography Proximity Effect (LPE)



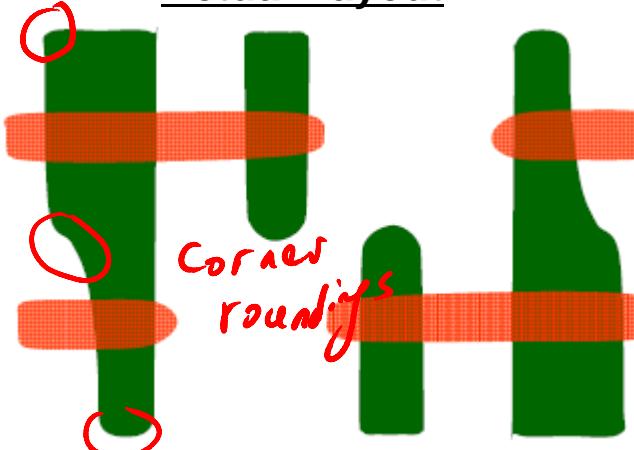
- Optical Proximity Correction (OPC)**
used to compensate for image errors due to diffraction effects by adding extra polygons to the pattern on the photomask
- Phase Shift Mask (PSM)**
used to reduce the light interference by changing the thickness of transmitting patterns on the photomask (i.e. creating a phase shift light)



Desired 6T SRAM Layout

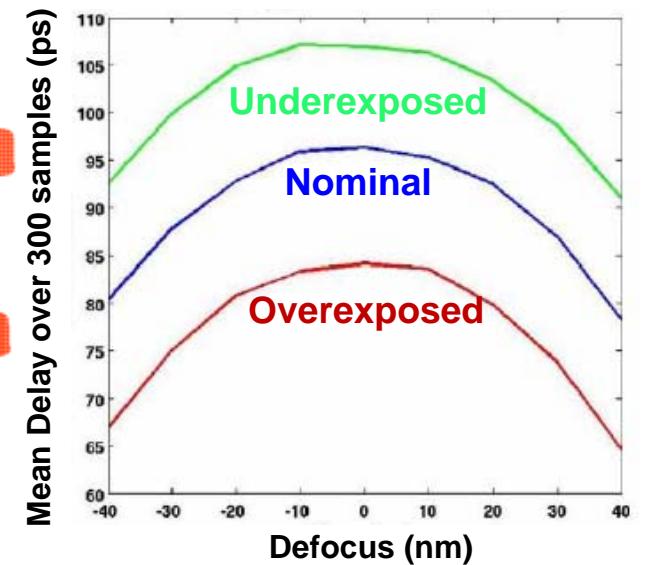


Actual Layout

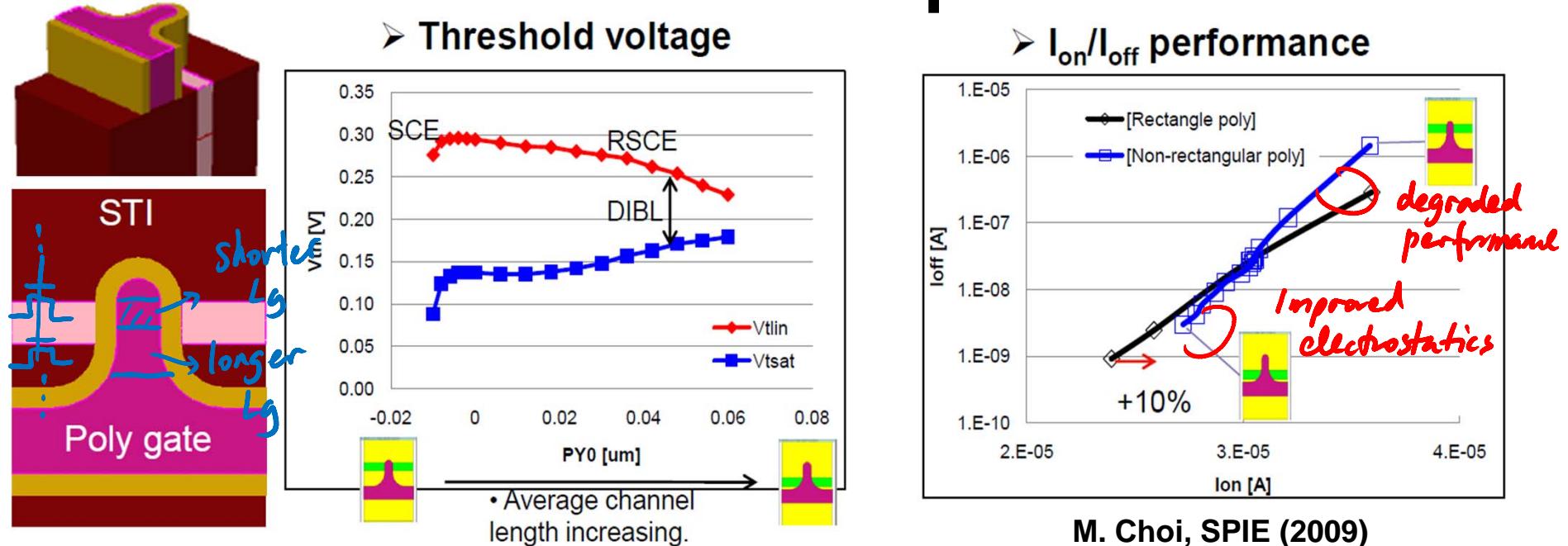


➤ These resolution enhancement techniques help to reduce the pattern distortions, yet still end with round corners.

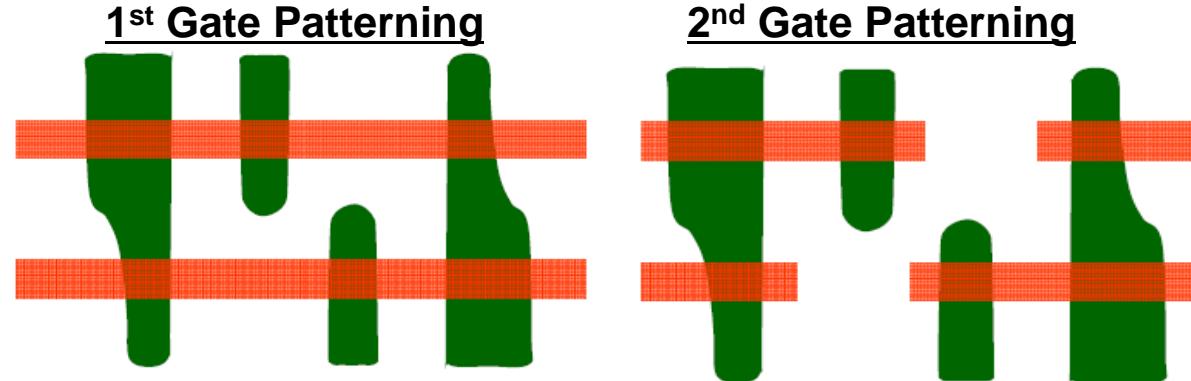
NAND2 Delay Distributions



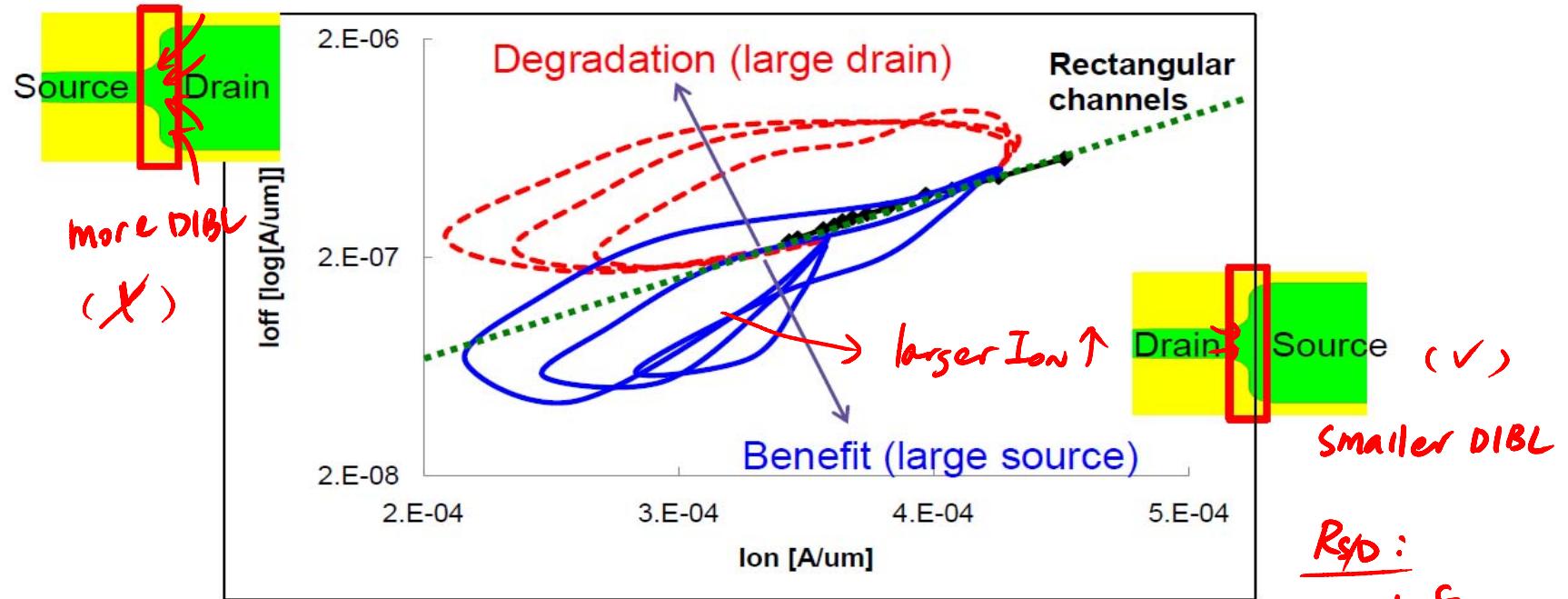
Impact of Poly Corner Rounding: Gate-Extension Dependence



- Poly corner rounding can be improved by using multiple patterning/exposure techniques.



Impact of Active Region Rounding: Asymmetric Source/Drain



- Large source structure provides better performance
 - 10% Ion gain or 3x I_{off} reduction
- Large drain structure degrades performance
 - 50% Ion degradation or 3x I_{off} leakage ↑

*due to the poor
electrostatics*

M. Choi, SPIE (2009)

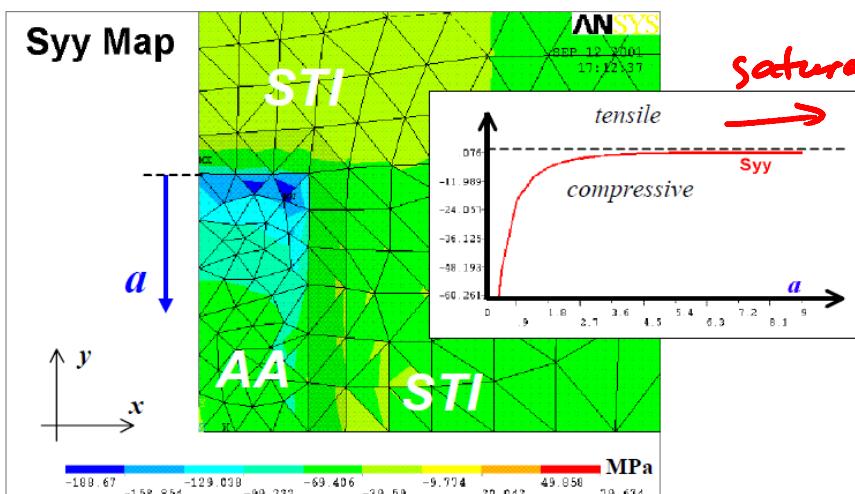
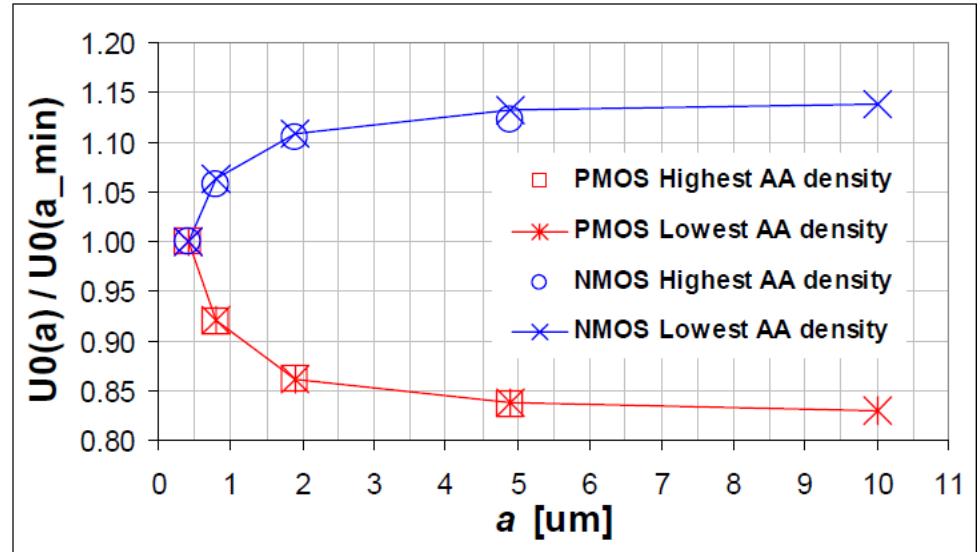
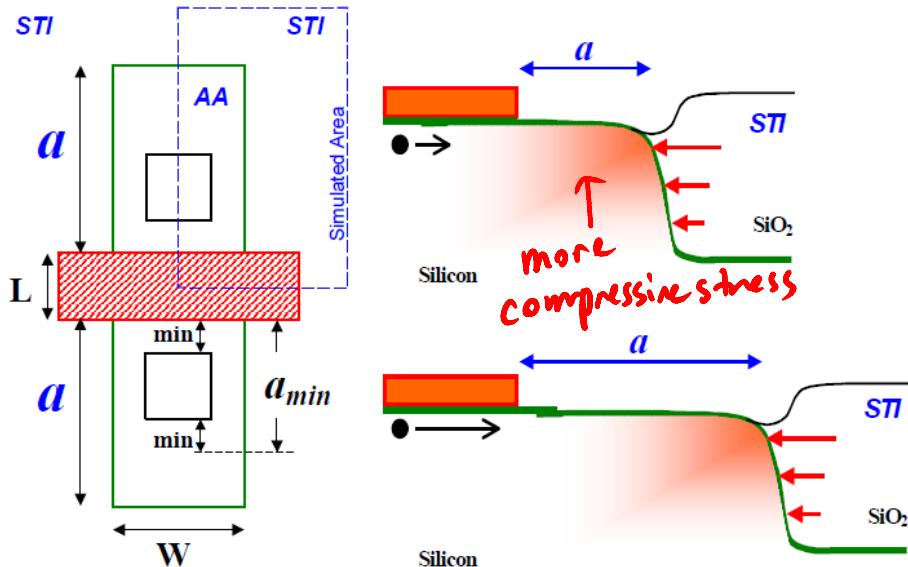
R_{SD} :

$\frac{I_{DS}}{I_{DS} + I_{DS'} \cdot \frac{V_{GS} - V_{TH}}{R_S}}$

$I_{DS} \propto (V_{GS} - V_{TH})^\alpha$

R_S plays a more
important role than R_D
does

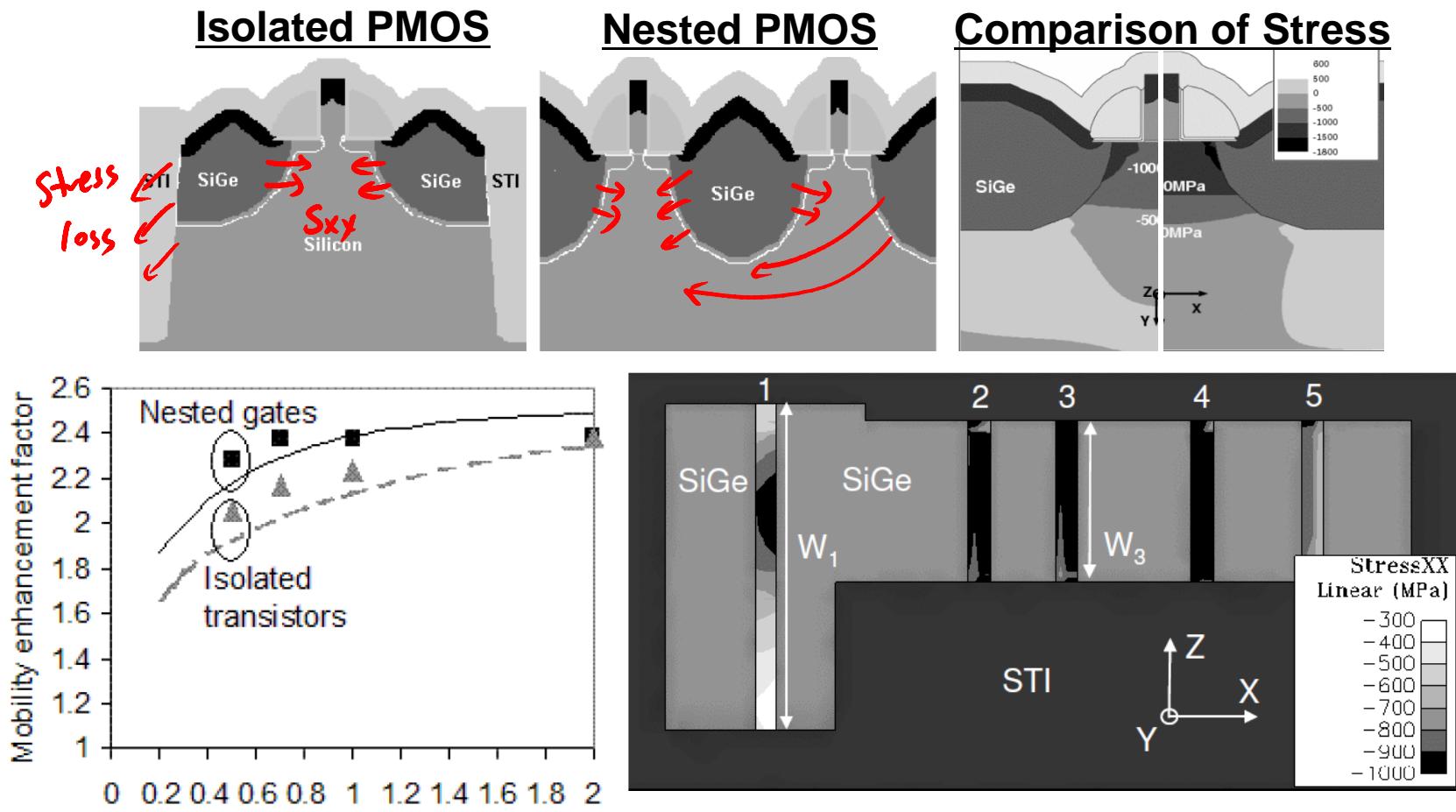
STI Proximity Effect



- Due to the different thermal expansion coefficients between Si and STI, there exists **biaxial compressive** residual stress in the active region after processing.
- STI-stress generally increases PMOS current and decreases NMOS current.
- Stress relaxes exponentially with increased distance from Si/STI boundary.

R. A. Bianchi, IEDM (2002)

Layout Dependent Strain: eSiGe Source/Drain

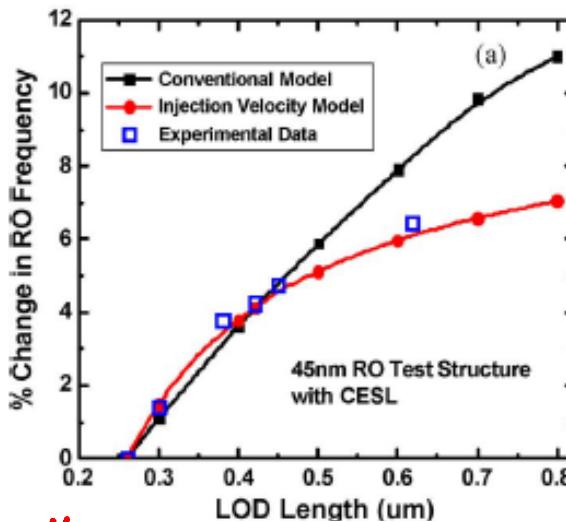
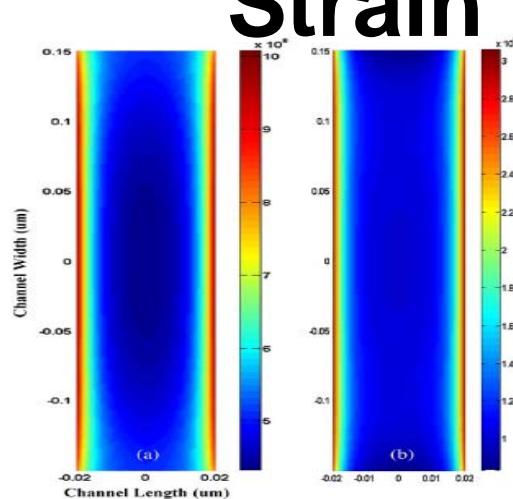
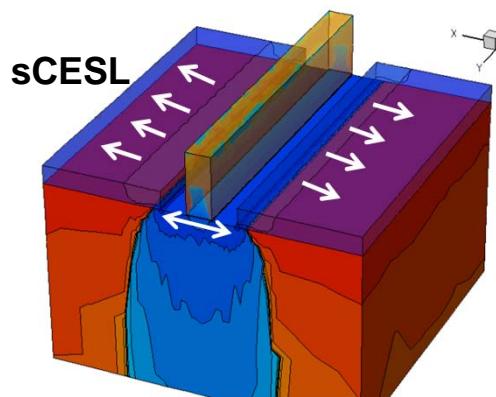


V. Moroz, SISPAD (2008)

Other Sources for Layout Dependent Strain

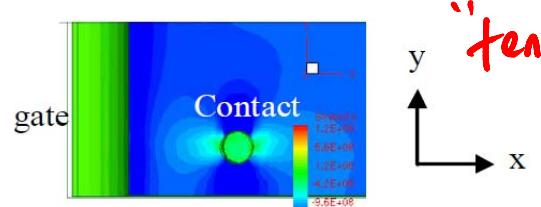
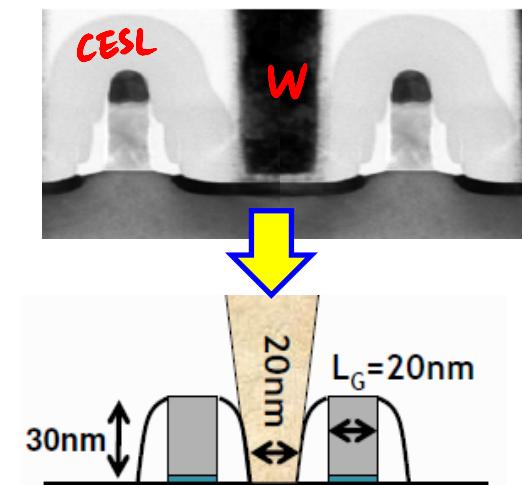
sCESL-induced Strain

N. Xu, TDMR (2011)

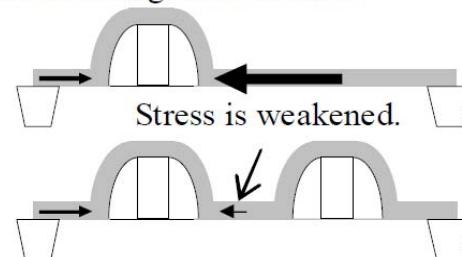


Contact-induced Strain

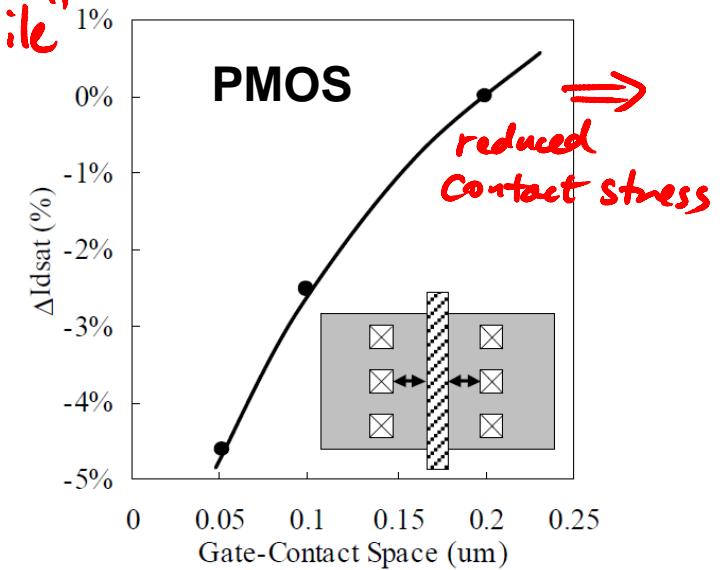
H. Aikawa, VLSI-T (2008)



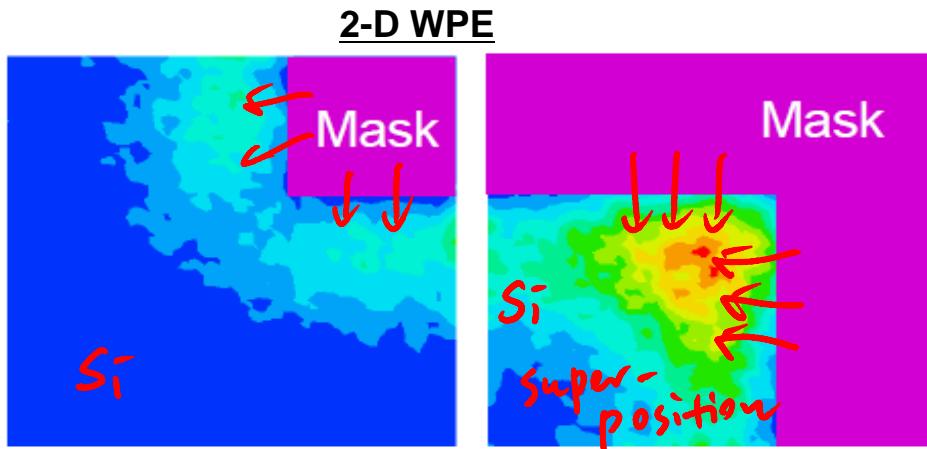
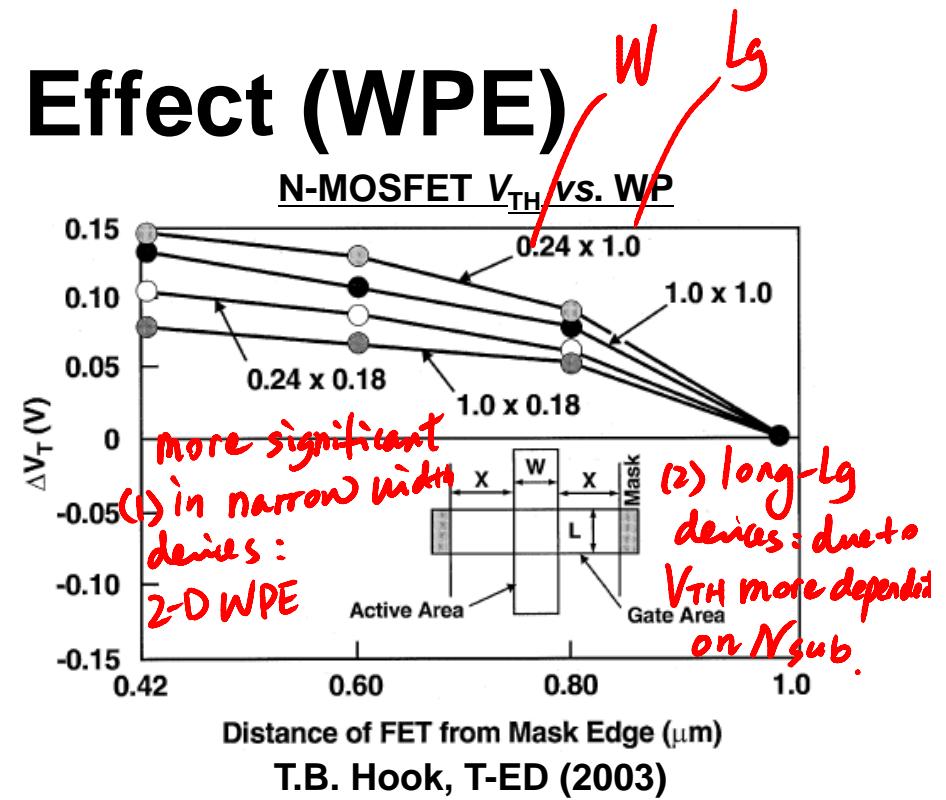
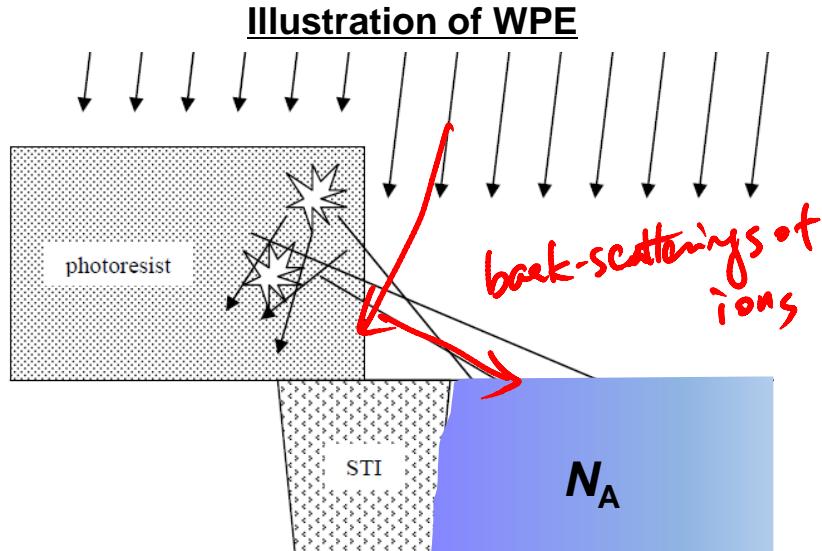
(a) Stress change near contact



(b) The effect of neighboring gates



Well Proximity Effect (WPE)

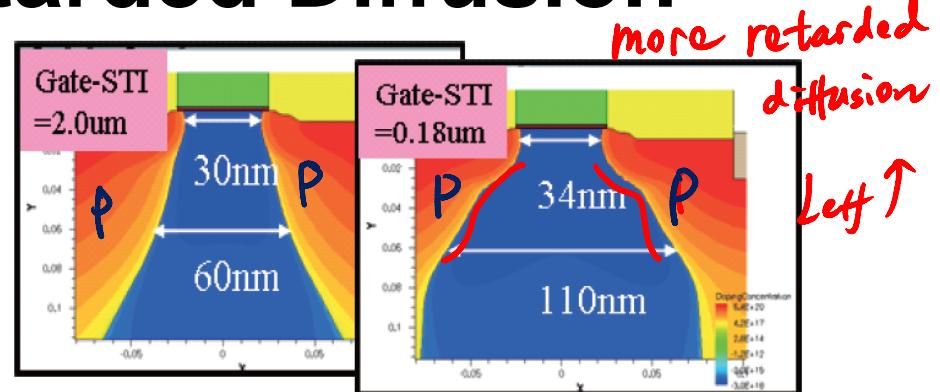


- During ion implantation, kinetic ions scatter back out of PR and become embedded in the Si near PR edge, causing V_{TH} shift.
- The affected distance is $\sim 1\mu\text{m}$.
- Small angle II helps, but never avoids WPE.

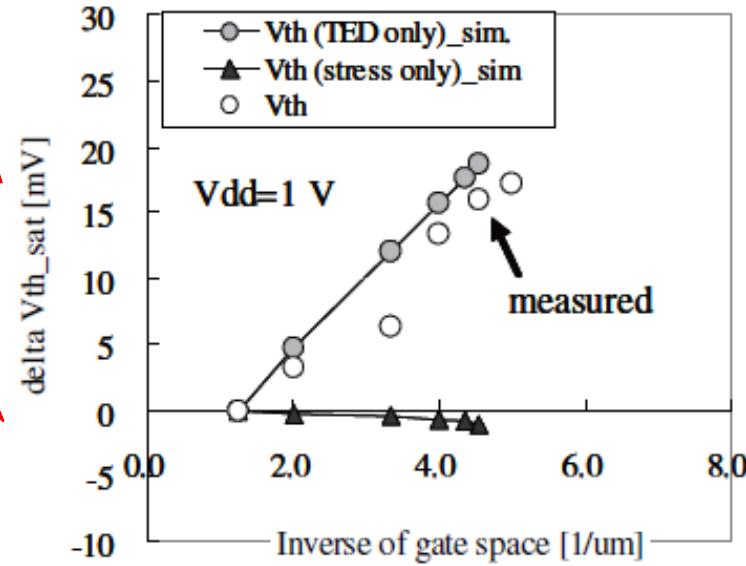
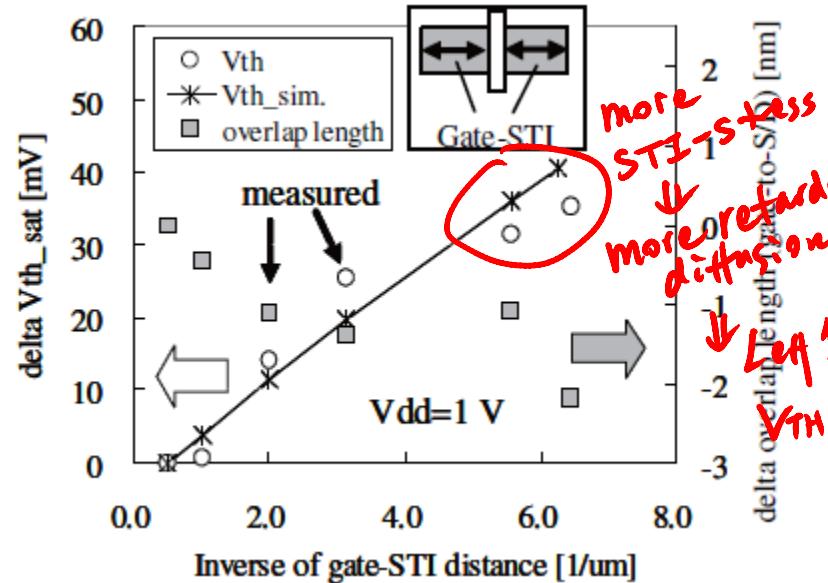
Another WPE: Stress-induced Enhanced/Retarded Diffusion

H. Tsuno, VLSI-T (2007)

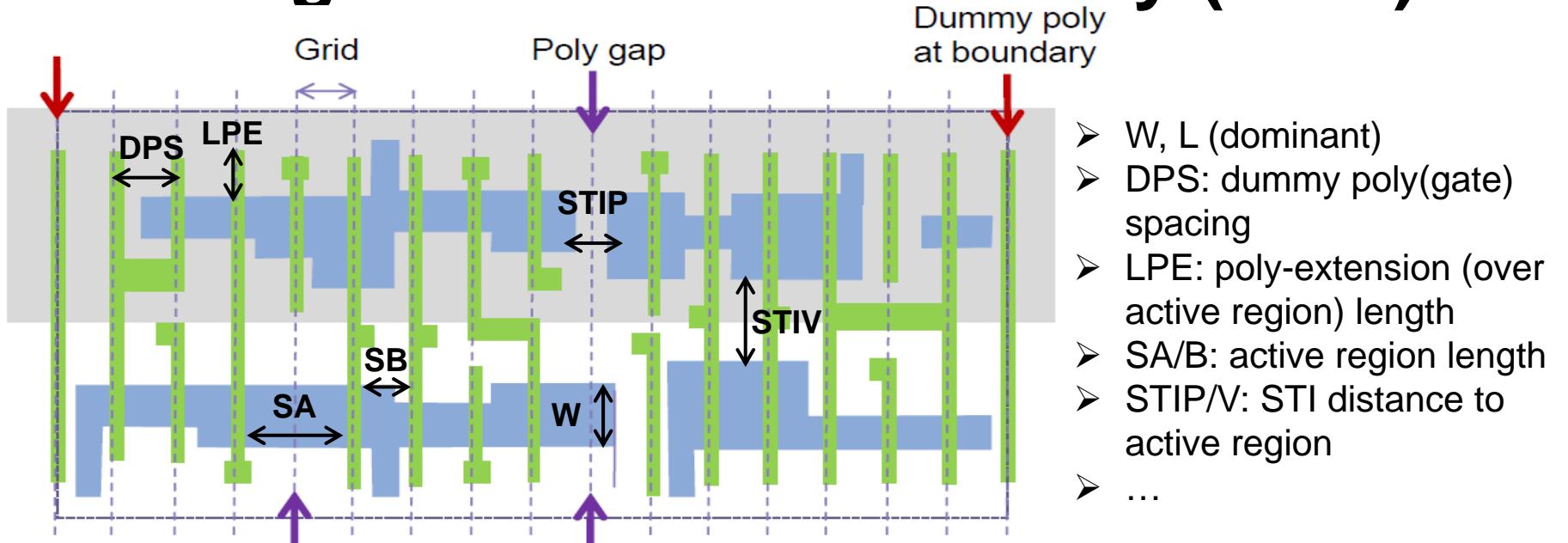
Layout parameters	NFET			PFET	
	B	As	P	B	As
shrinkage	B	As	P	B	As
Gate-STI	-9%	-17%	-34%	-23%	-43%
Gate space	1%	1%	3%	2%	4%
STI width	4%	8%	15%	11%	18%



N-MOSFET V_{TH} Shift vs. Inverse of (l) STI-Gate Distance and (r) Gate Spacing



Design for Manufacturability (DFM)



Carrier Mobility

$$\mu = \mu_{ref} \frac{1 + K_\mu \left(\frac{1}{SA + L/2} + \frac{1}{SB + L/2} \right)}{1 + K_\mu \left(\frac{1}{SA_{ref} + L/2} + \frac{1}{SB_{ref} + L/2} \right)}$$

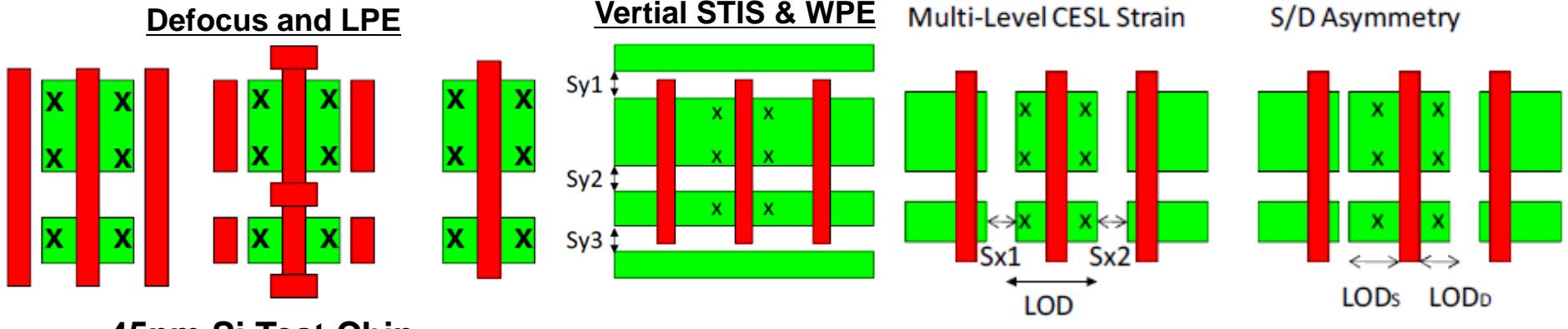
Threshold Voltage

$$V_{TO} = V_{TO_{ref}} + K_V \left(\frac{1}{SA + L/2} + \frac{1}{SB + L/2} - \frac{1}{SA_{ref} + L/2} - \frac{1}{SB_{ref} + L/2} \right)$$

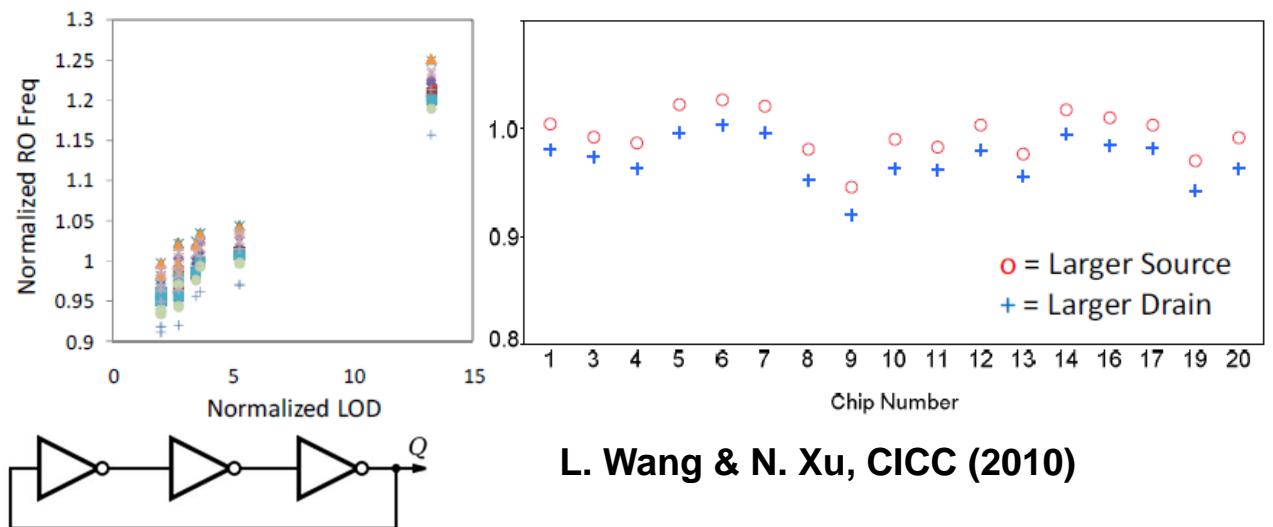
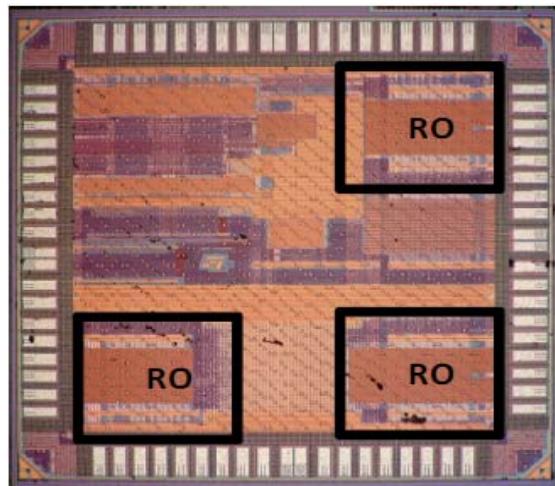
where $K_V = \frac{K_{VTO}}{1 + \frac{L_{KVTO}}{L^{LLODKVTO}} + \frac{W_{KVTO}}{W^{WLQDKVO}} + \frac{P_{KVTO}}{L^{LLODKVTO} W^{WLQDKVO}}}$

- Compact modeling is the best solution to leverage between the accuracy and design complexity.

Monitors for Systematic Variability



45nm Si Test Chip



L. Wang & N. Xu, CICC (2010)

- Ring oscillators (RO) and OFF-state transistors are often used to characterize transistors' performance and leakage.

Summary of Systematic Variability on Planar Bulk MOSFETs

Layout Variation	Typical I_{on} variation range	Typical V_{th} variation range
Length of diffusion (LOD) (SiGe or STI)	~30%	~50mV
Spacing to adjacent diffusion	~5%	~15mV
Active diffusion corners	~5%	~15mV
Poly spacing	~15%	~30mV
Poly corner rounding	~5%	~20mV
Well boundary (WPE)/ Dual stress liner (DSL)	~15%	~90mV
Contact to gate distance	~3%	~10mV

impacts of different systematic variability sources

Courtesy of X.-W. Lin (Synopsys)

- Layout-dependent strain and WPE play the dominant role on transistor performance's drift.

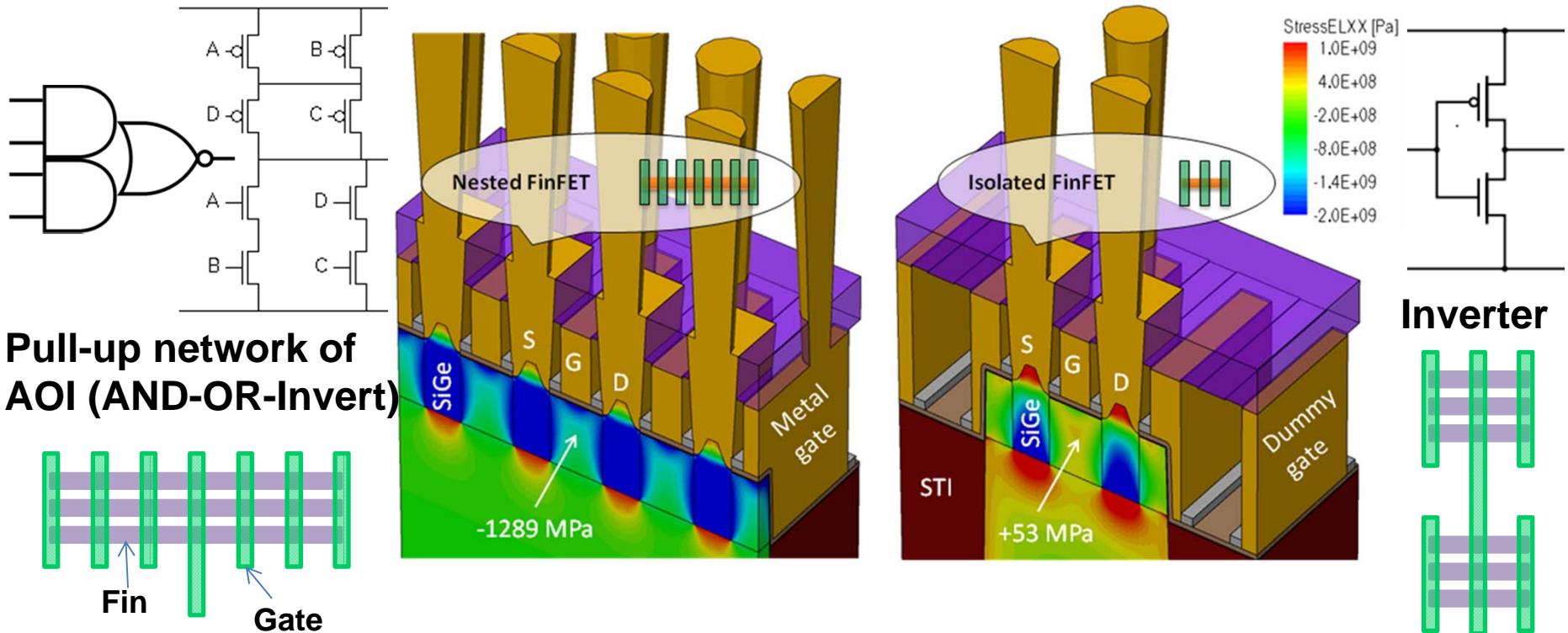
delay(ps) leakage power(nW)	no well proximity model		using well proximity model		
	25C/1.0V	value	ratio	value	ratio
inverter	cell rise	27.98	1	30.12	1.08
	cell fall	19.34	1	21.19	1.10
	leakage	4.654	1	2.448	0.53
NAND	cell rise	31.18	1	33.34	1.07
	cell fall	28.83	1	31.55	1.09
	leakage	5.095	1	3.007	0.59
NOR	cell rise	55.67	1	59.88	1.08
	cell fall	20.52	1	22.38	1.09
	leakage	10.107	1	6.222	0.62

standard logic circuit performance shift w/ WPE

Y.-M. Sheu, CICC (2005)

- Small active-region area cells suffer more from systematic variability.

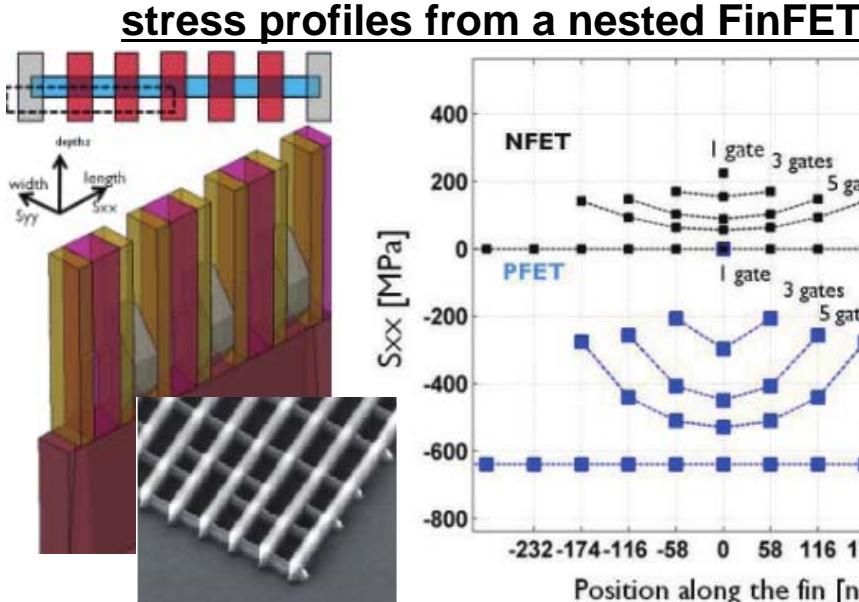
Impact of Layout Dependent Strain on FinFETs



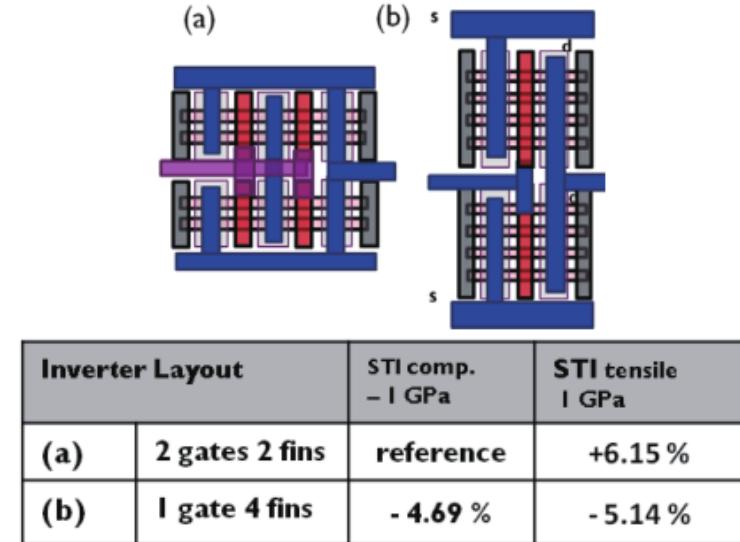
- Topologies of nested and isolated FinFET are unavoidable.
- Mobility of nested FinFET will be enhanced by ~80%.
- Stress of isolated FinFET is almost relaxed.

M. Choi, ISTD (2012)

Strained FinFET Inverter Performance



CMOS Inverter performance benchmark



- PMOS stress (induced by eSiGe) boosts with fin length and # of gates per fin and degrades with increasing fin pitch.
- NMOS stress (induced by tensile STI) boosts with increasing fin pitch, and degrades with increasing # of gates per fin.
- For a CMOS inverter, the best configuration comes from a multiple-gate yet moderate fin-pitch design.

M. G. Bardon, VLSI-T (2013)

References

1. T. B. Hook *et al.*, “Lateral Ion Implant Straggle and Mask Proximity Effect,” *IEEE Transactions on Electron Devices*, vol.50, no.9, pp. 1946-1951, 2003.
2. R.A. Bianchi *et al.*, “Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance,” *IEEE IEDM Tech. Dig.*, pp.117-120, 2002.
3. V. Moroz *et al.*, “The Impact of Layout on Stress-Enhanced Transistor Performance,” *SISPAD Tech. Dig.*, pp.143-146, 2005.
4. N. Xu *et al.*, “Physically based Modeling of Stress Induced Variation in Nanoscale Transistor Performance,” *IEEE Transactions on Device and Material Reliability*, vol.11, no.3, pp. 378-386, 2011.
5. H. Aikawa *et al.*, “Variability Aware Modeling and Characterization in Standard Cell in 45nm CMOS with Stress Enhancement Technique,” *Symp. VLSI Tech.*, pp.90-91, 2008.
6. H. Tsuno *et al.*, “Advanced Analysis and Modeling of MOSFET Characteristics Fluctuation Caused by Layout Variation,” *Symp. VLSI Tech.*, pp.204-205, 2007.
7. L. T.-N. Wang *et al.*, “Parameter-Specific Ring Oscillator for Process Monitoring at the 45nm Node,” *IEEE CICC Tech. Dig.*, 2010.
8. Y.-M. Sheu *et al.*, “Modeling Well Edge Proximity Effect on Highly-Scaled MOSFETs,” *IEEE CICC Tech. Dig.*, 2005.
9. M. Choi *et al.*, “14nm FinFET Stress Engineering with Epitaxial SiGe Source/Drain,” *International SiGe Technology and Device Meeting*, Berkeley, CA, 2012.
10. M. G. Bardon *et al.*, “Layout induced Stress Effects in 14nm and 10nm FinFETs and their Impact on Performance,” *Symp. VLSI Tech.Dig.*, pp. 114-115, 2013.