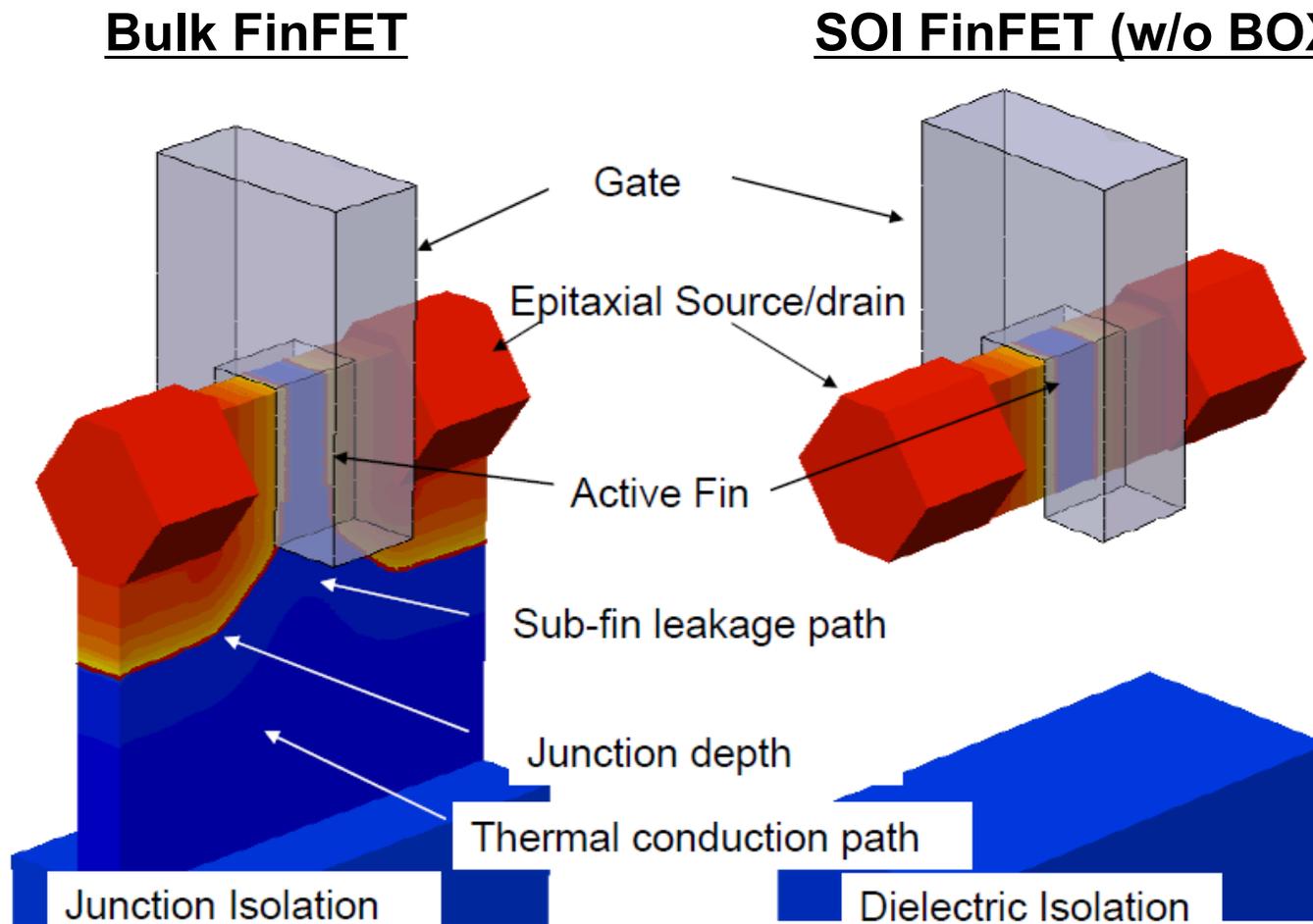


# Lecture 7

- Thin-Body MOSFET's Process I
  - SOI vs. Bulk FinFETs
  - Fin Patterning Techniques
  - High-κ/Metal Gate Technologies

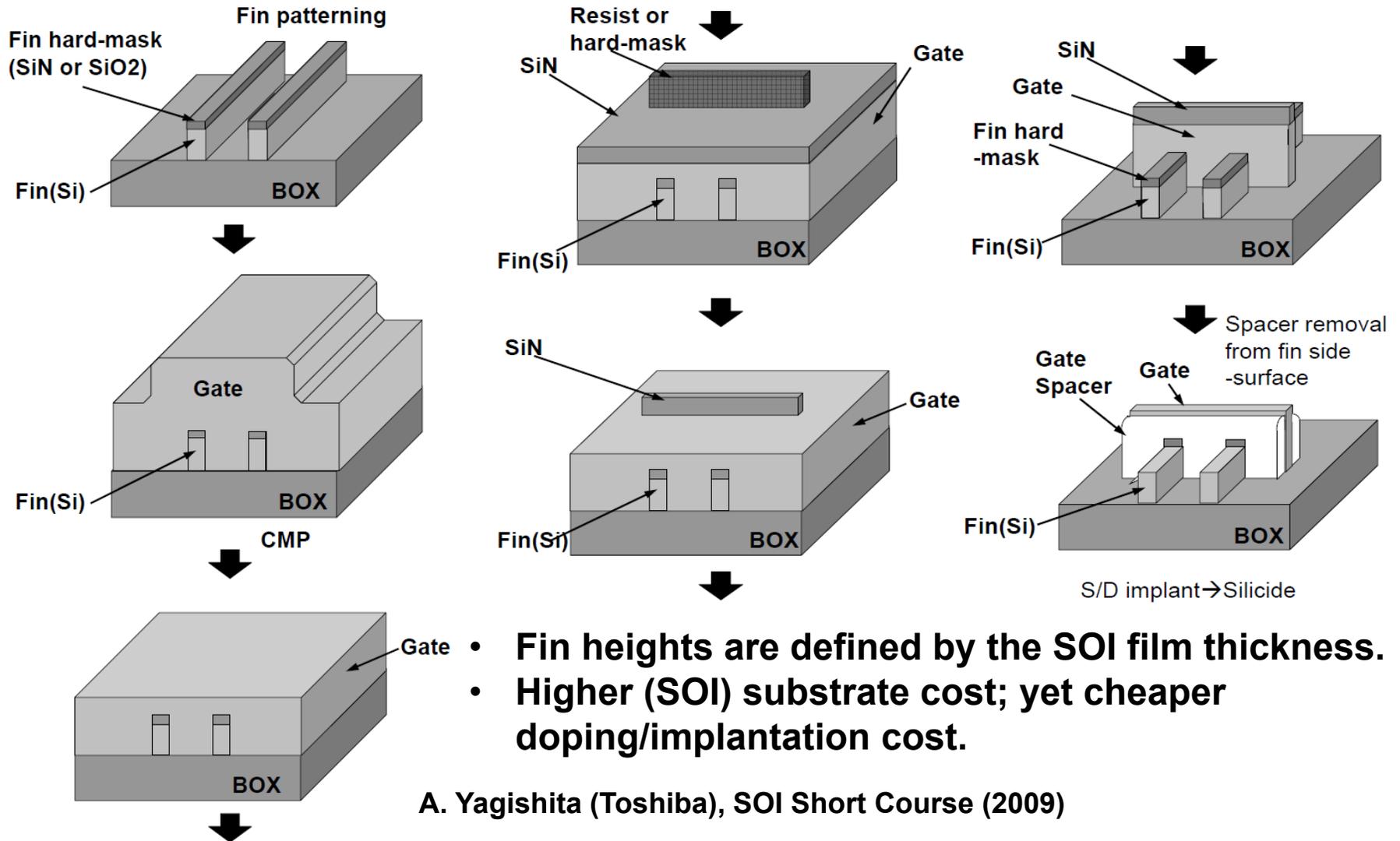
Reading: multiple research articles (reference list at the end of this lecture)

# SOI vs. Bulk FinFET: Overall Structure



T. Hook (IBM), FDSOI Workshop (2013)

# SOI FinFET Process Flow

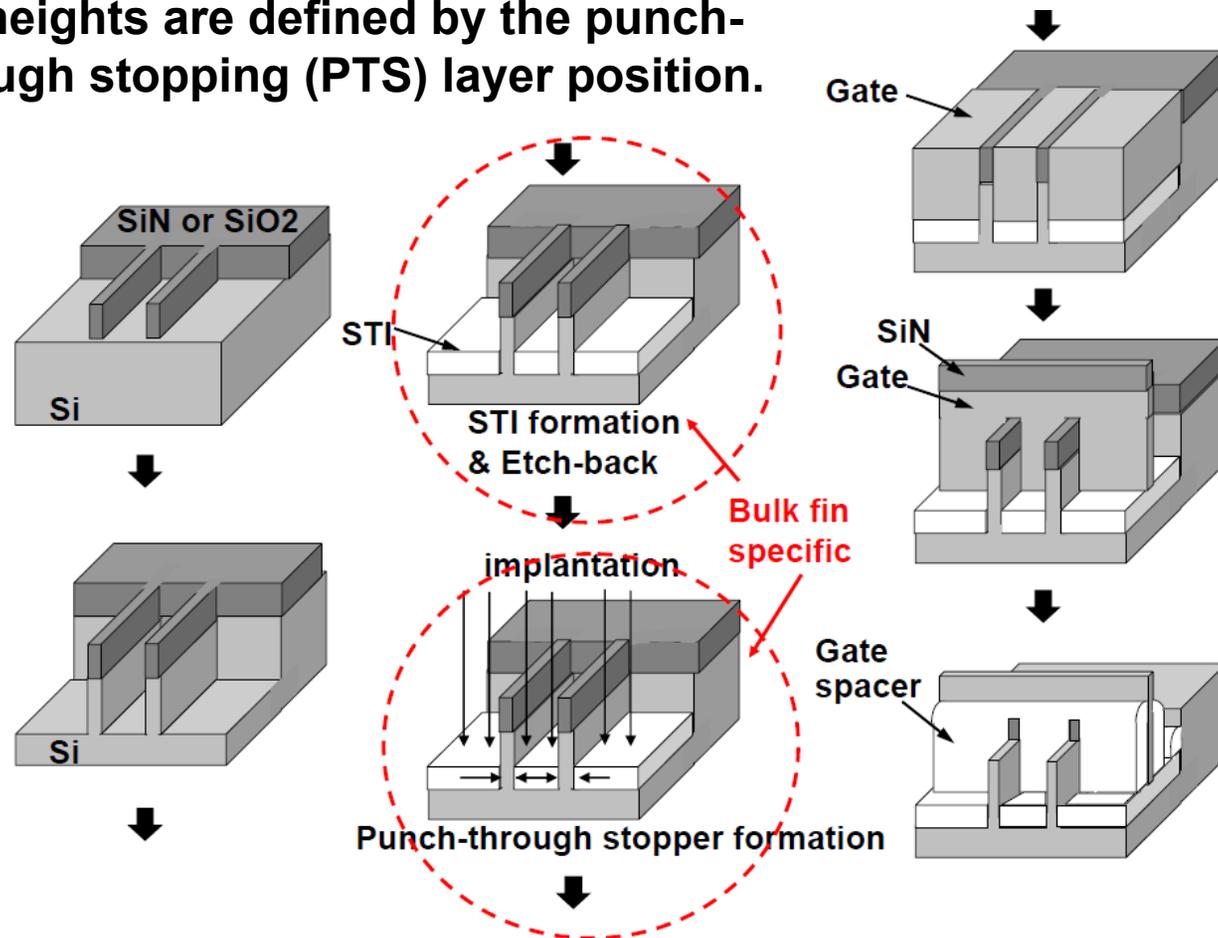


- Fin heights are defined by the SOI film thickness.
- Higher (SOI) substrate cost; yet cheaper doping/implantation cost.

A. Yagishita (Toshiba), SOI Short Course (2009)

# Bulk FinFET Process Flow

- Fin heights are defined by the punch-through stopping (PTS) layer position.

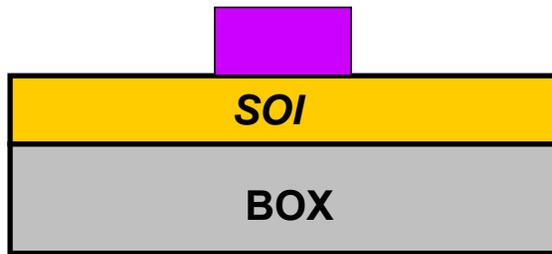


A. Yagishita (Toshiba), SOI Short Course (2009)

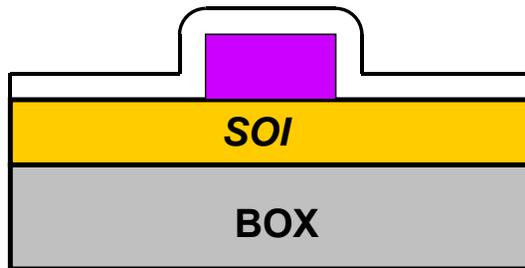
# Fin Patterning

Spacer Lithography  
a.k.a. Sidewall Image Transfer (SIT)  
or Self-Aligned Double Patterning (SADP)

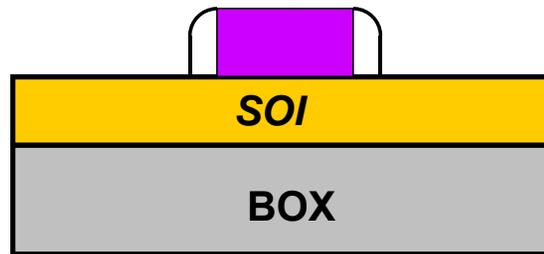
1. Deposit & pattern sacrificial layer



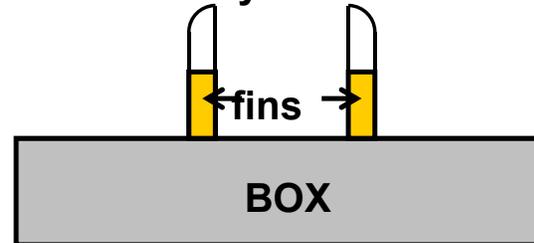
2. Deposit mask layer ( $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$ )



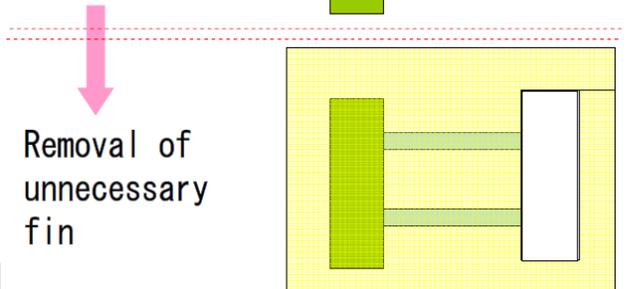
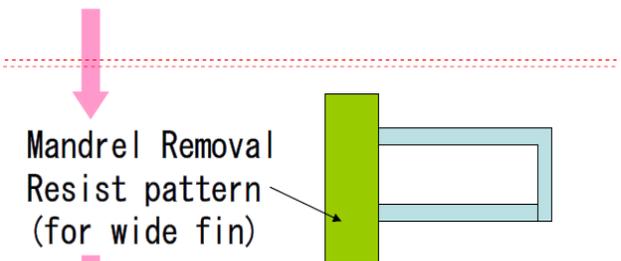
3. Etch back mask layer to form "spacers"



4. Remove sacrificial layer; etch SOI layer to form fins



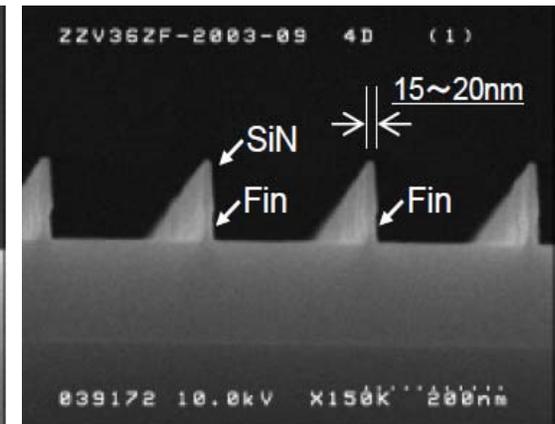
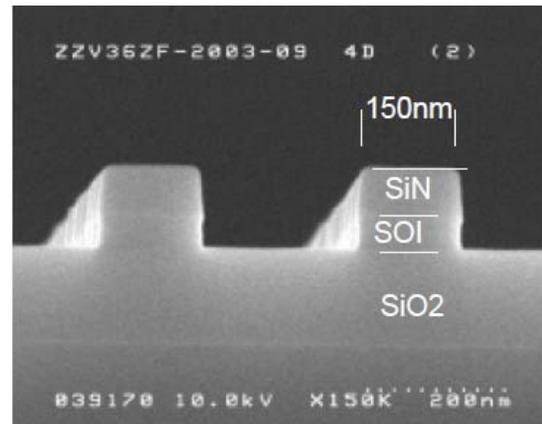
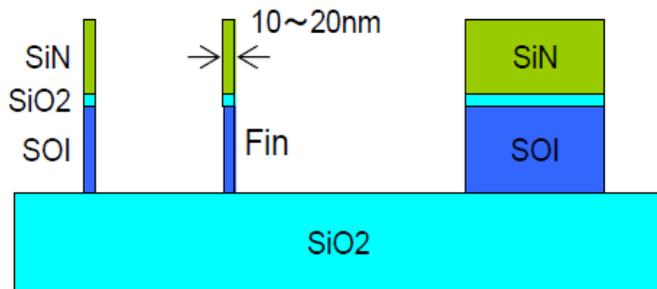
- Note that fin pitch is  $1/2\times$  that of patterned layer



- Extra lithography steps required to etch the unused fins.

# Benefit on Multiple Device Pitch

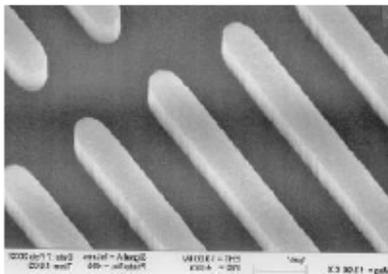
- By using spacer lithography technique, multiple fin pitches can be implemented using a single lithography step.



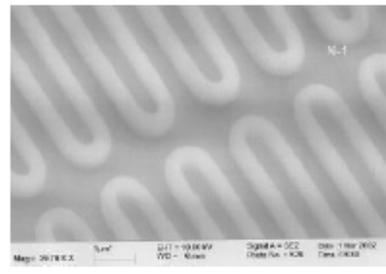
- 2<sup>n</sup> lines after n<sup>th</sup> lithography !**

A. Yagishita (Toshiba), SOI Short Course (2009)

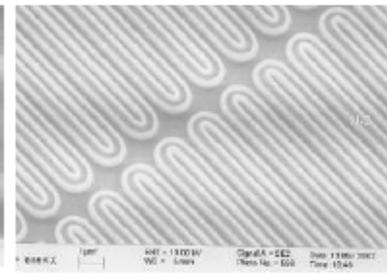
sacrificial structures



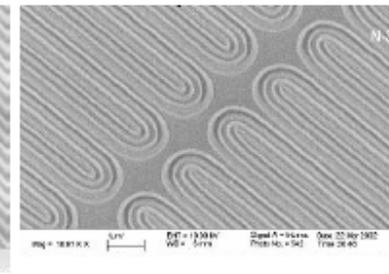
1st Spacers



2nd Spacers



3rd Spacers

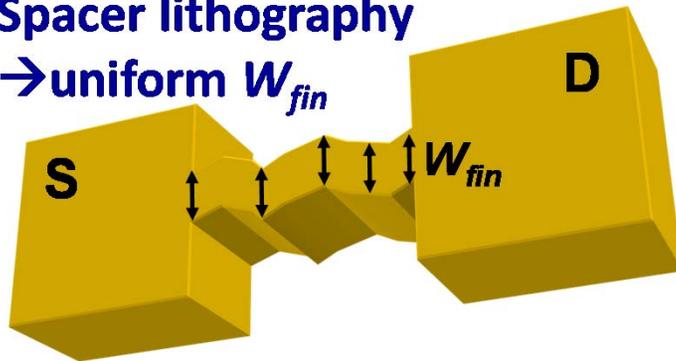


# Benefit on Fin Edge Roughness

Y.-K. Choi, IEDM (2002)

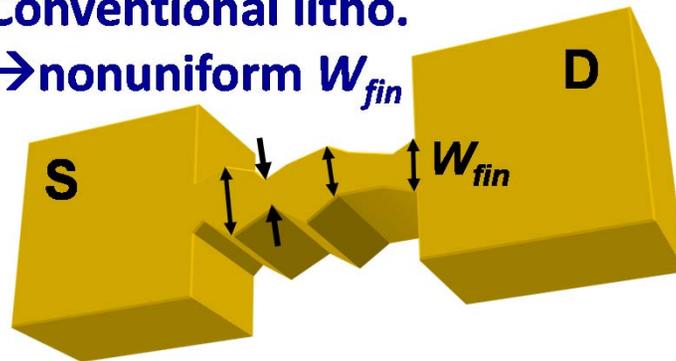
Spacer lithography

→ uniform  $W_{fin}$

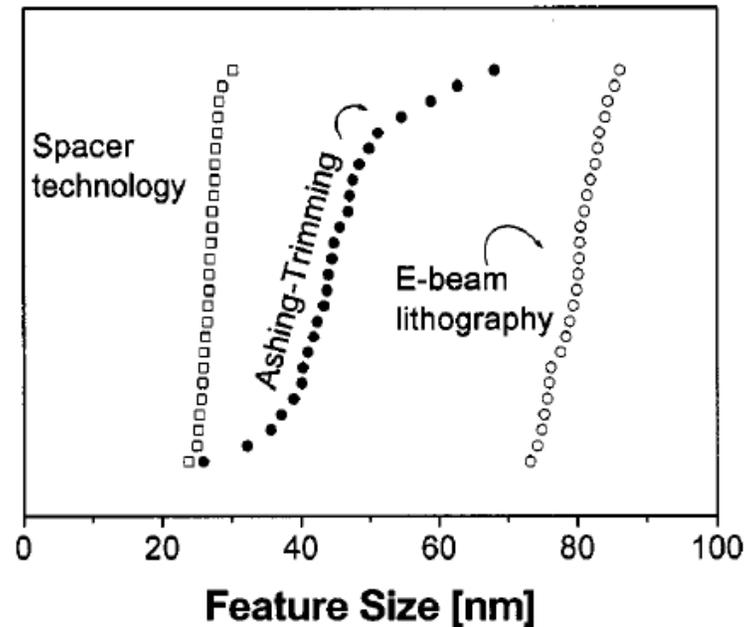


Conventional litho.

→ nonuniform  $W_{fin}$



Cumulative Distribution of CD

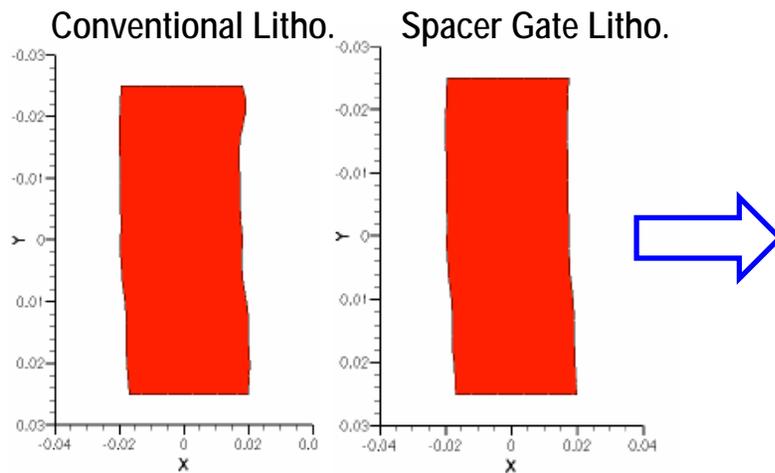
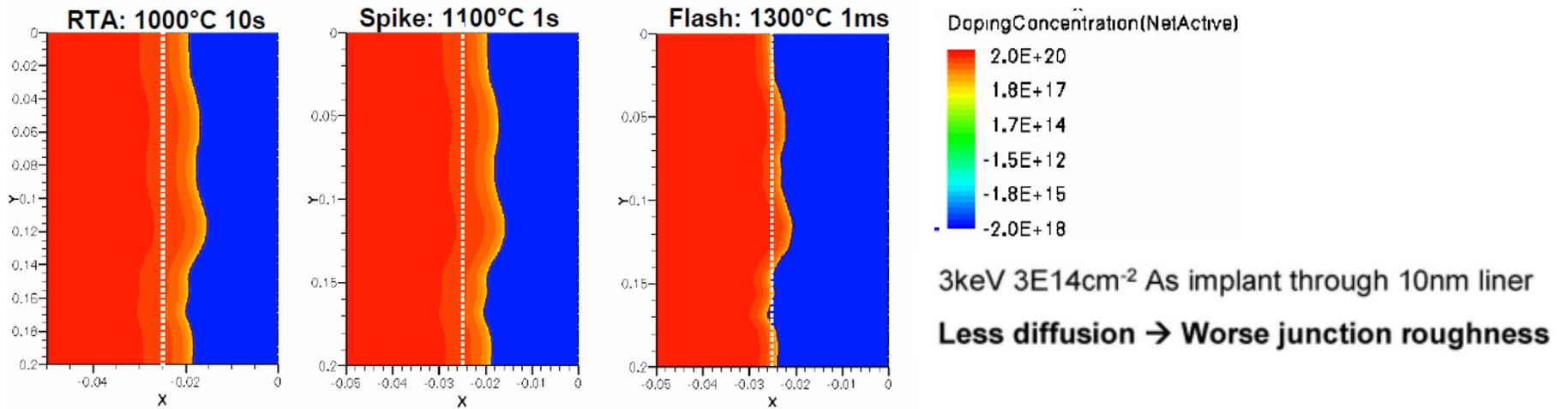


Y.-K. Choi, IEDM (2002)

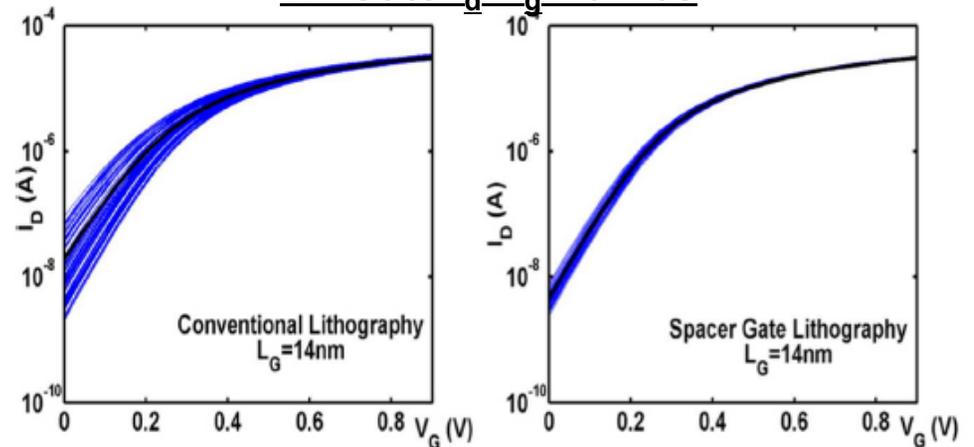
- Spacer lithography technique provides more uniform fin width than the conventional lithography, due to  $\sigma_{litho} > \sigma_{CVD}$

# Benefit on Gate Edge Roughness

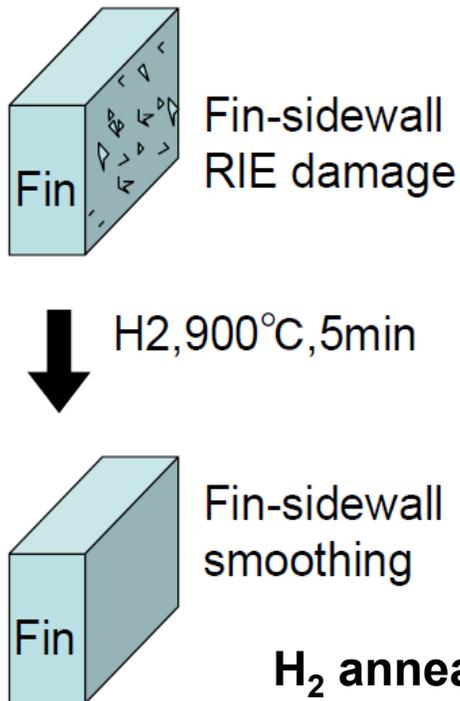
X. Sun, TSM (2010)



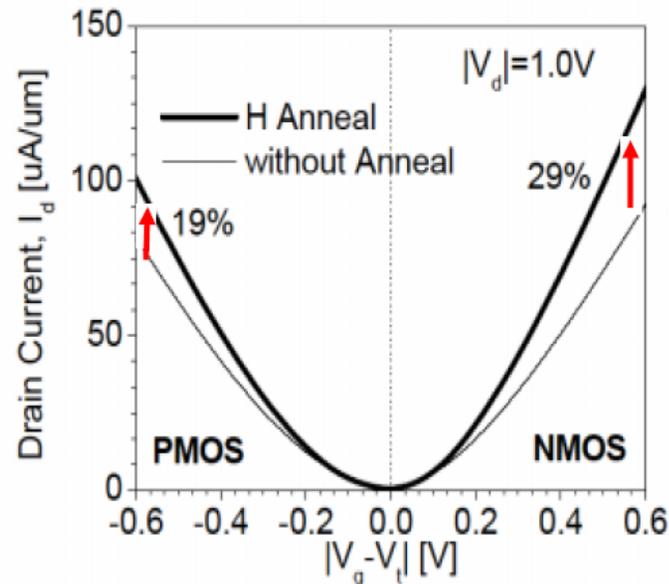
## Tri-Gate $I_d$ - $V_g$ Curves



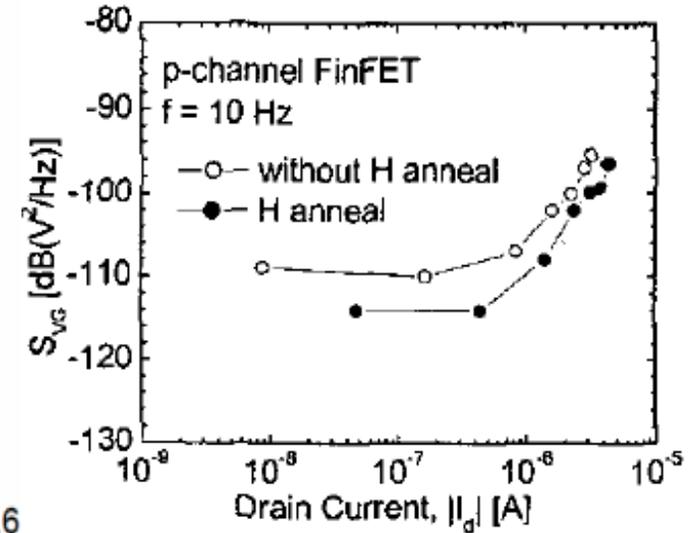
# Fin Sidewall Damage Removal by H<sub>2</sub> Annealing



**Mobility Improvement by H<sub>2</sub> Annealing**



**Equivalent Gate Input Noise**

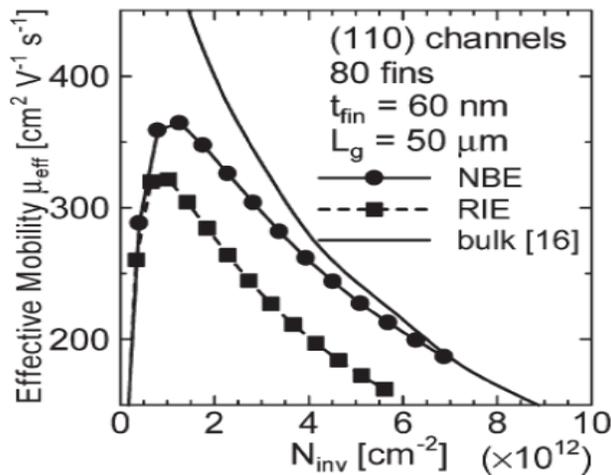
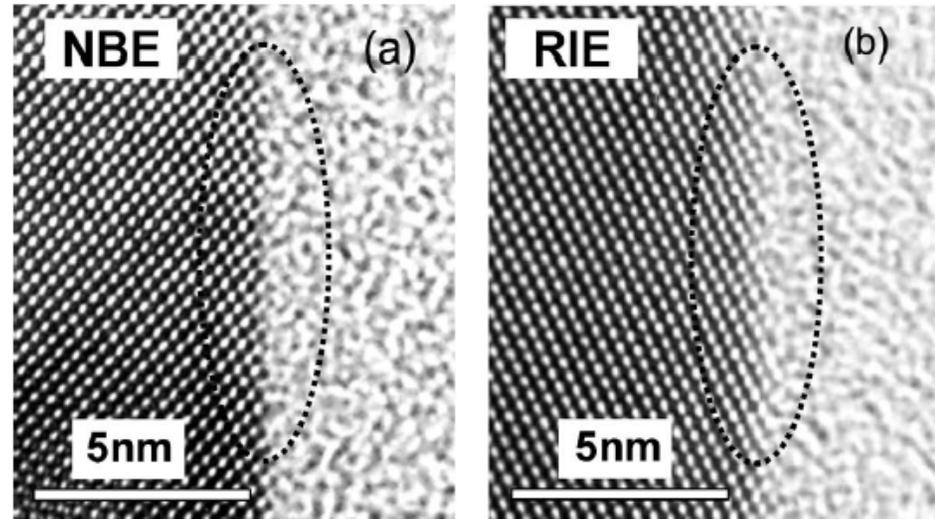
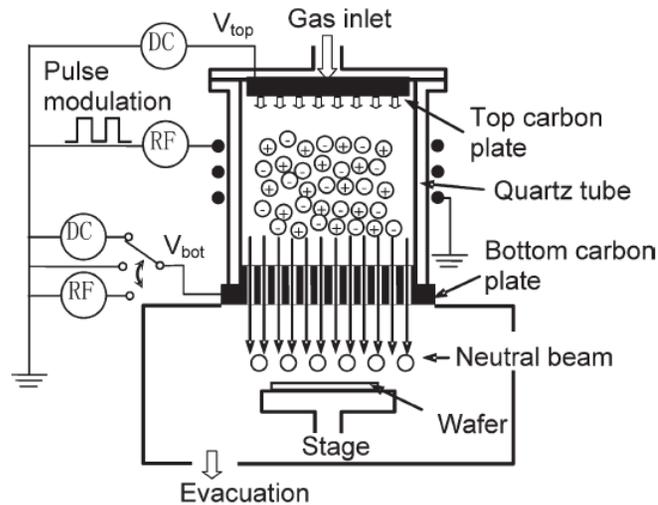


**H<sub>2</sub> annealing causes Si atoms remigration at fin sidewall surfaces**

- provides smaller surface roughness and lower  $D_{it}$ .
- reduces shape corners to mitigate “corner effect”.

Y.-K. Choi, IEDM (2002)

# Fin Sidewall Damage Removal by Neutral Beam Etching

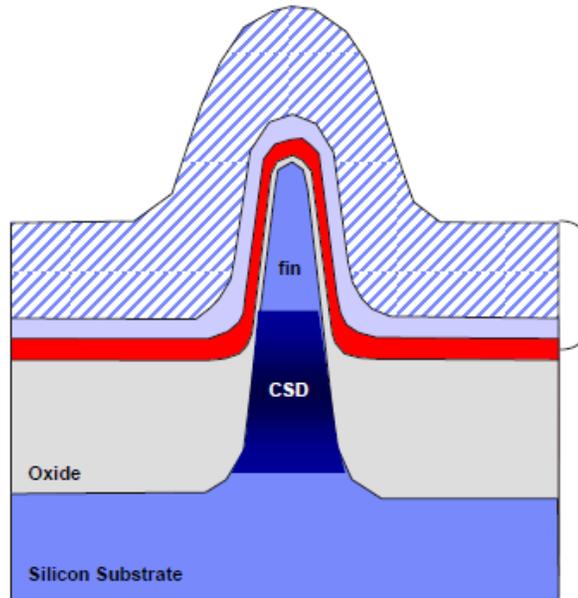


K. Endo, TED (2006)

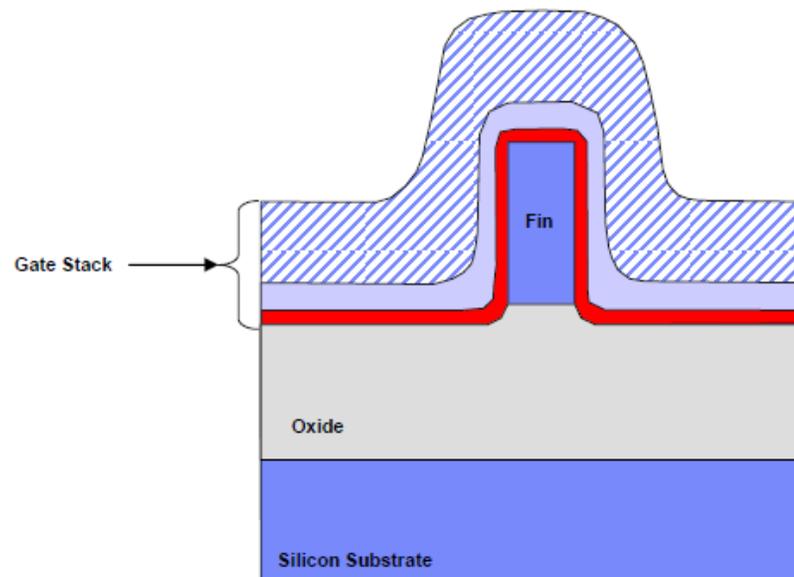
- Neutral Beam Etching: negative ions in the plasma can be neutralized by passing through the carbon aperture.
- TEM picture shows more abrupt fin/oxide interface after NBE  $\rightarrow$  Lower  $D_{it}$
- Higher fin mobility w/ NBE

# SOI vs. Bulk FinFET: Isolation

## Bulk FinFET



## SOI FinFET (w/o BOX)

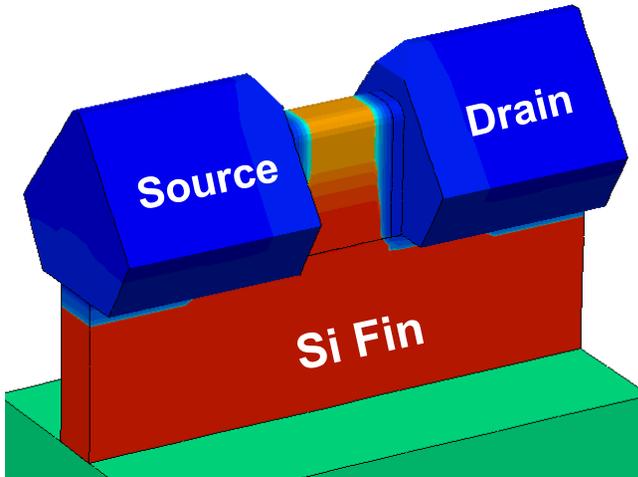


- Retrograde-well doping required as punch through-stop (PTS) layer.
- HALO is also often adopted.
- Tapered fin shape due to STI process.

- No doping process needed to avoid PT.
- Rectangular fin shape.

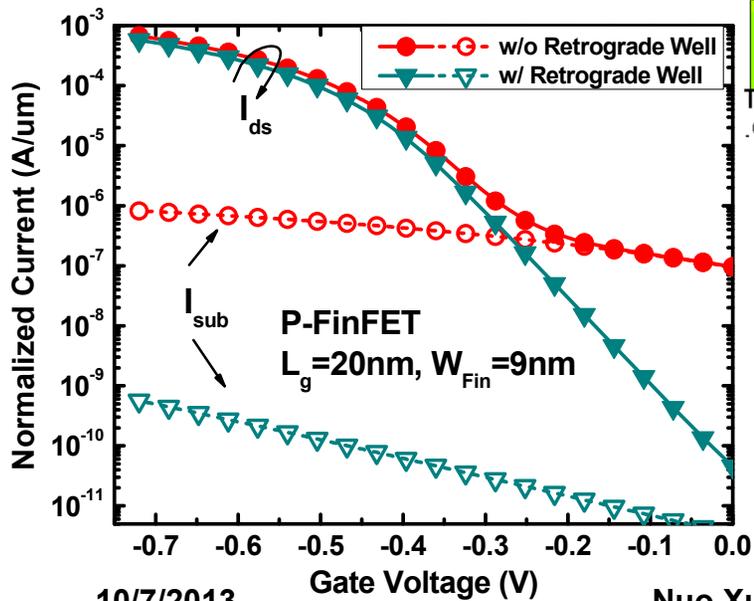
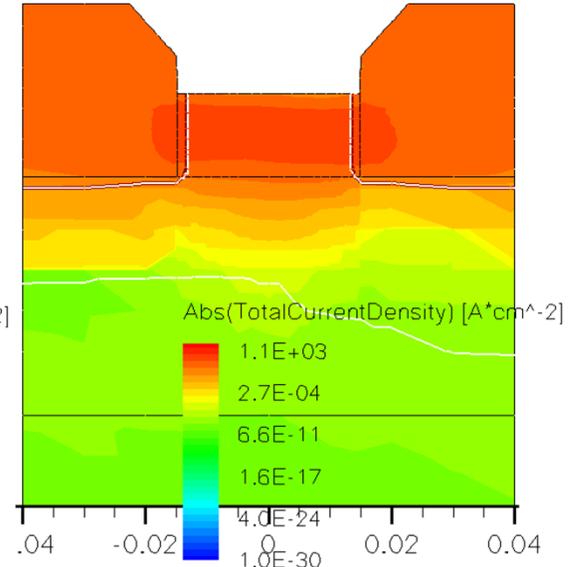
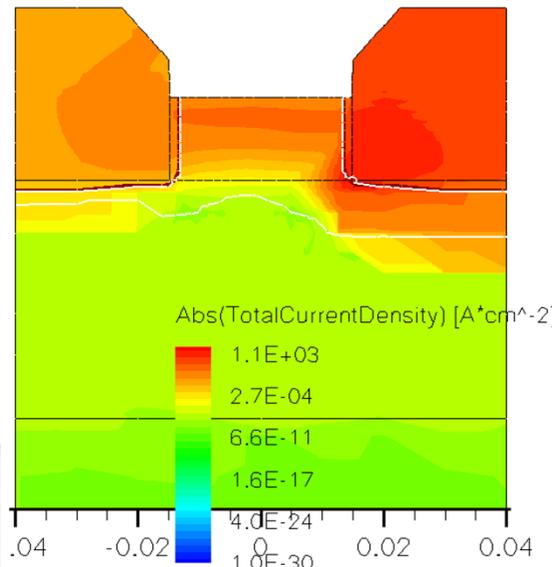
T. Hook (IBM), FDSOI Workshop (2013)

# Impacts of Retrograde Well Doping



w/ Retrograde Well Doping

w/o Retrograde Well Doping

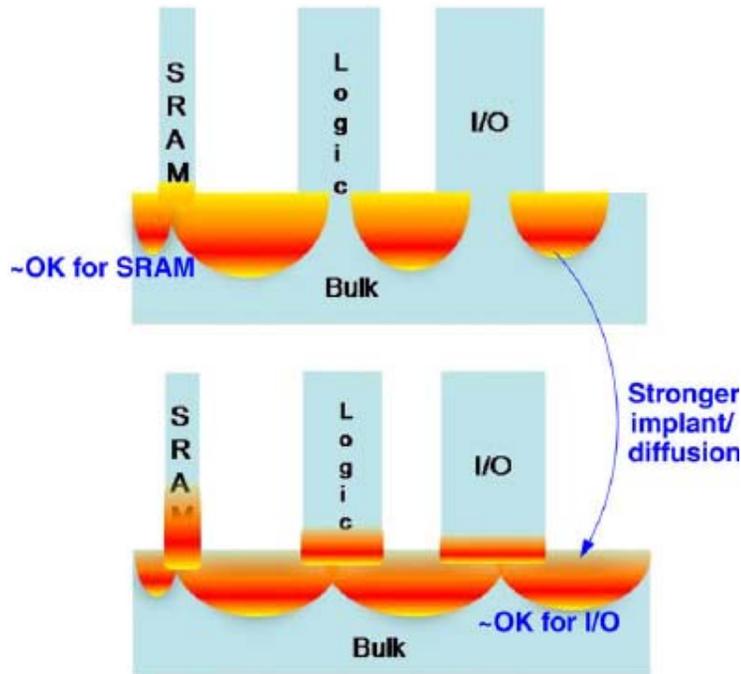


- Even with the finite steepness of retrograde well doping ( $\sim 15\text{nm/dec}$  in Si), it is still preferred to insert the doping peak around the fin base, causing some level of performance degradation in the fin.

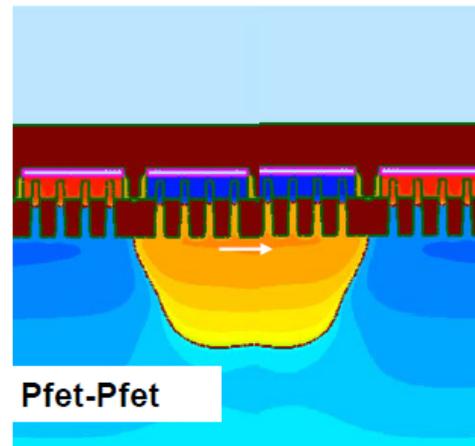
# More Issues for Bulk FinFET Isolation

Bulk FinFETs require

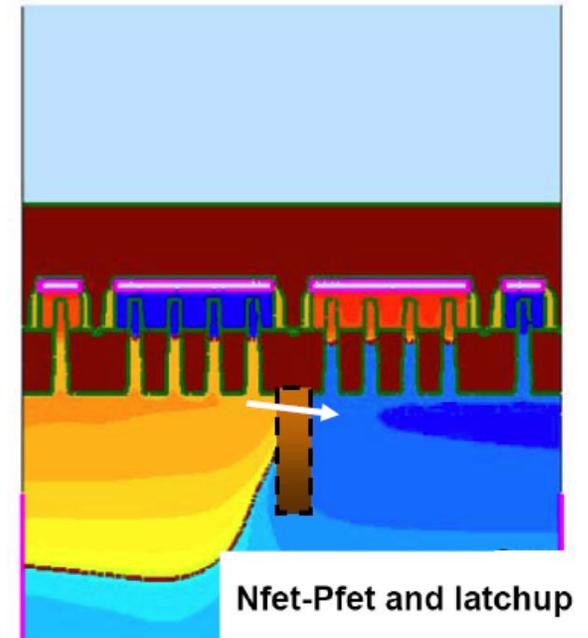
- Junction isolation masks and implants
- Well contacts
- Latchup prevention measures
  - Second STI
  - Heavily doped substrate



J. G. Fossum, SSE (2010)



Pfet-Pfet



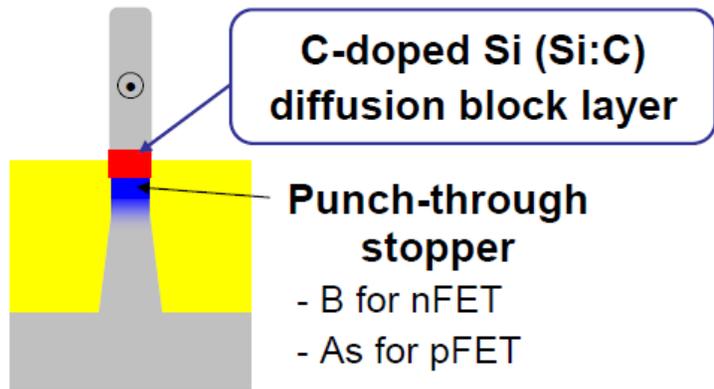
Nfet-Pfet and latchup

T. Hook (IBM), FDSOI Workshop (2013)

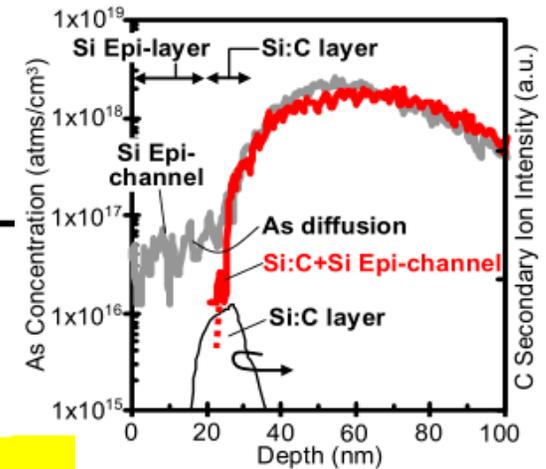
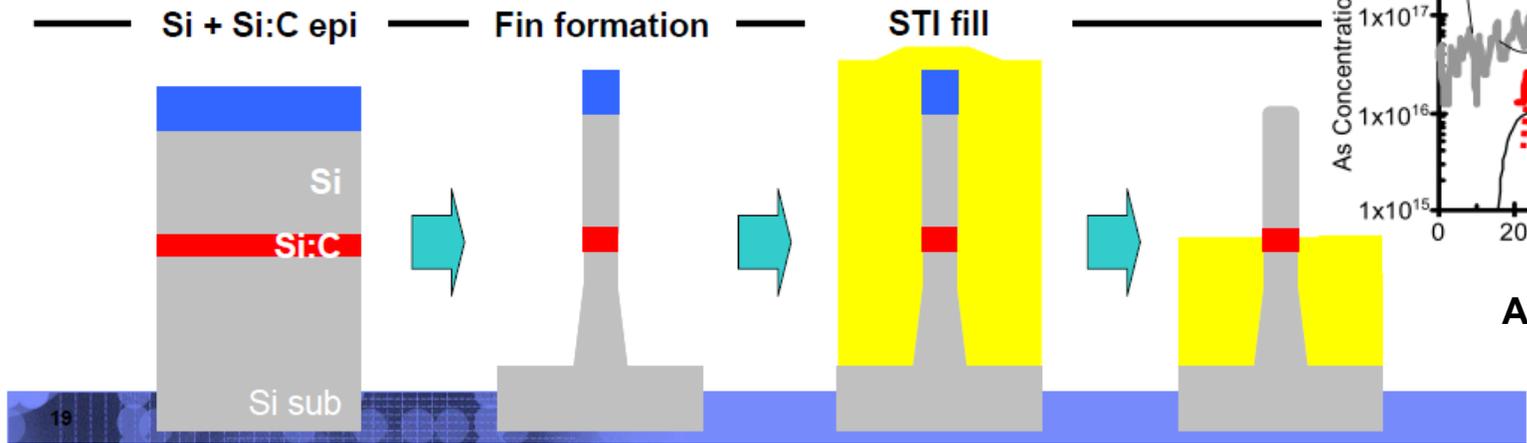
- **Single PTS doping can not be used for SoC circuits with multi-fin width.**
- **Additional STI required to separate N and P-bulk FinFET, to avoid CMOS latchup effect.**

# Steep Retrograde Well Doping in Bulk FinFET

SSRW formation using Si + Si:C epi before STI formation



Conc.  
 ✓ Thermal stability of Si:C layer  
 • Precipitates and clustering of C atoms → Defects in Si + Si:C epi layer  
 • C-diffusion

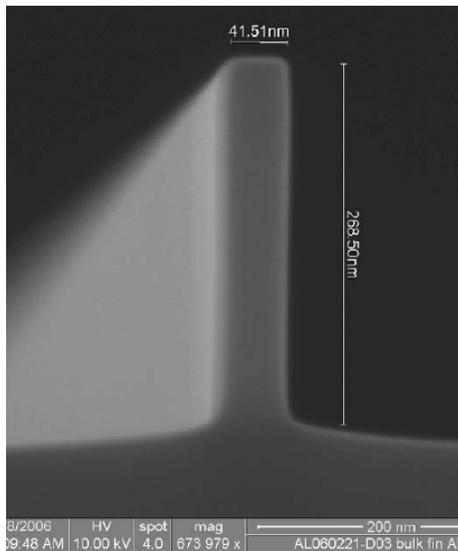


A. Hokazono, VLSI-T(2008) & IEDM(2009)

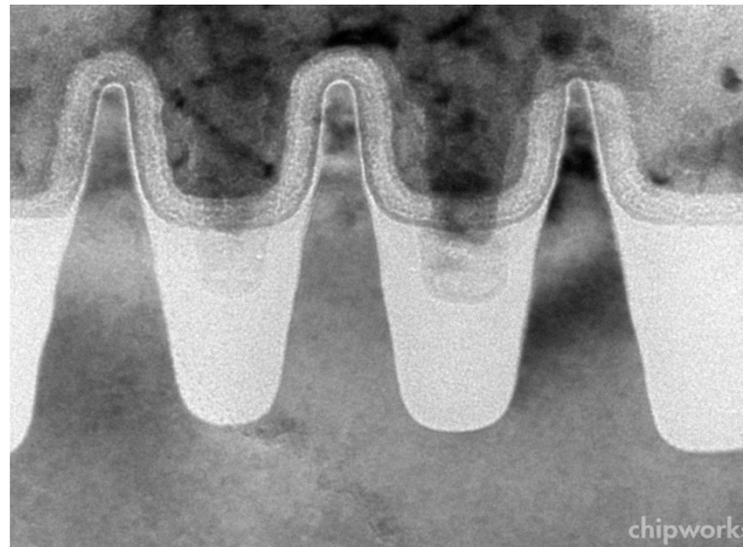
H. Bu (IBM), SOI Workshop (2011)

# Fin Shape Variations in Bulk FinFETs

Rectangular shape

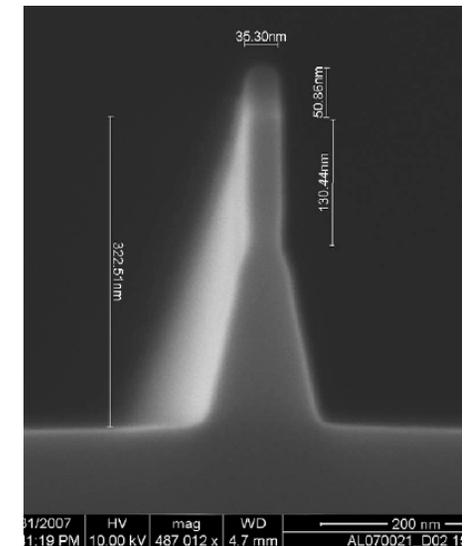


Trapezoidal shape (Intel's Tri-Gate)



Chipworks, 2012

"Hybrid"-shape



D. Shamiryan, SSE (2009)

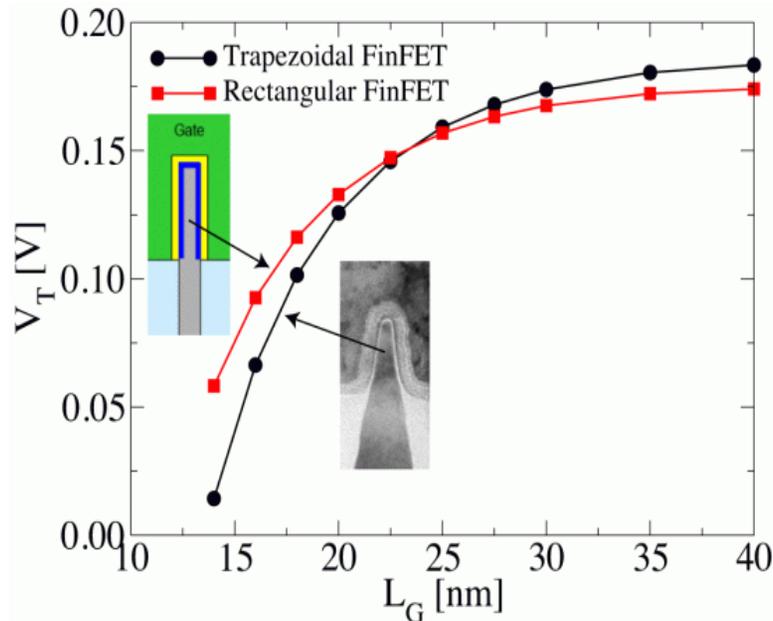
*Typical STI trench tilt: 70° ~ 85°*

**Key requirements for bulk fin shape (process perspective):**

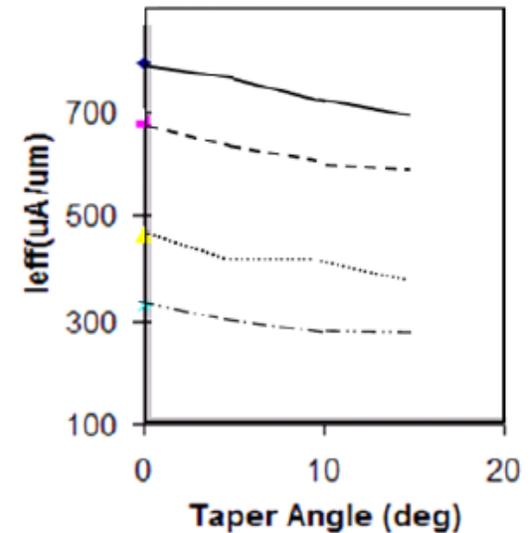
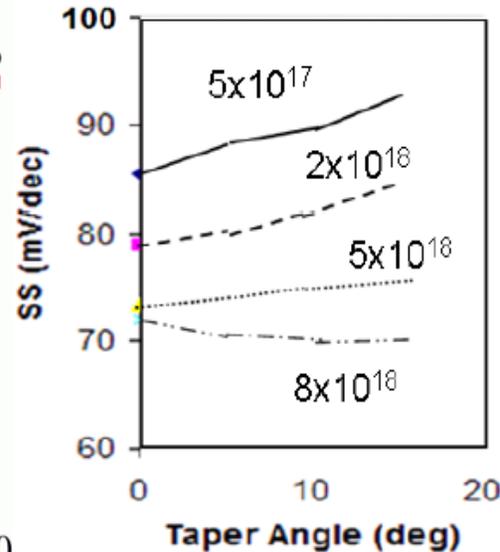
- Isolation trench refilling
- High aspect-ratio fin patterning

# Impacts of Fin Shape on Electrostatics

assuming same top fin width:



A. Arsenov's group, GSS Website (2012)



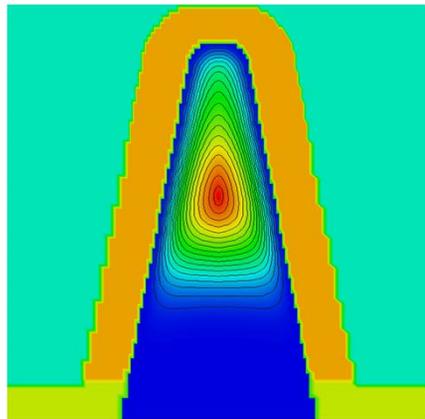
T. Hook (IBM), FDSOI Workshop (2013)

**Key requirements for bulk fin shape (device performance/reliability perspective):**

- Good electrostatic control
- Low corner electric field, to prevent TDDB or BTI

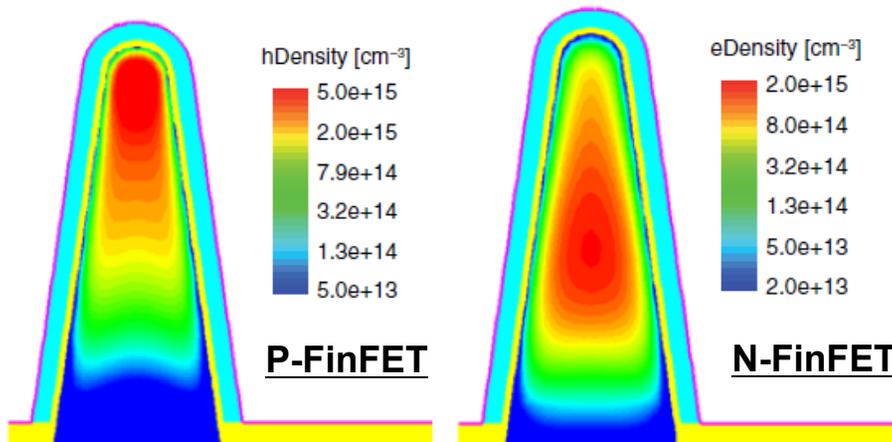
# Impacts of Fin Shape on Current

## Charge concentration across a FinFET X-section as increasing gate voltage



A. Arsenov's group, GSS Website (2012)

## Considering Quantum Mechanical + Strain Effect

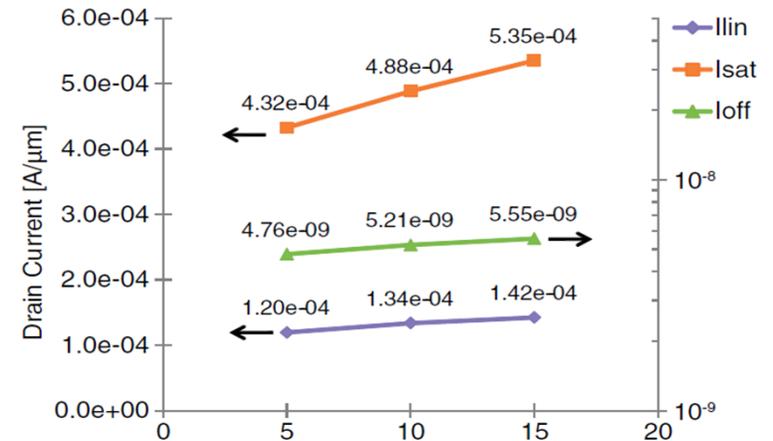


10/7/2013

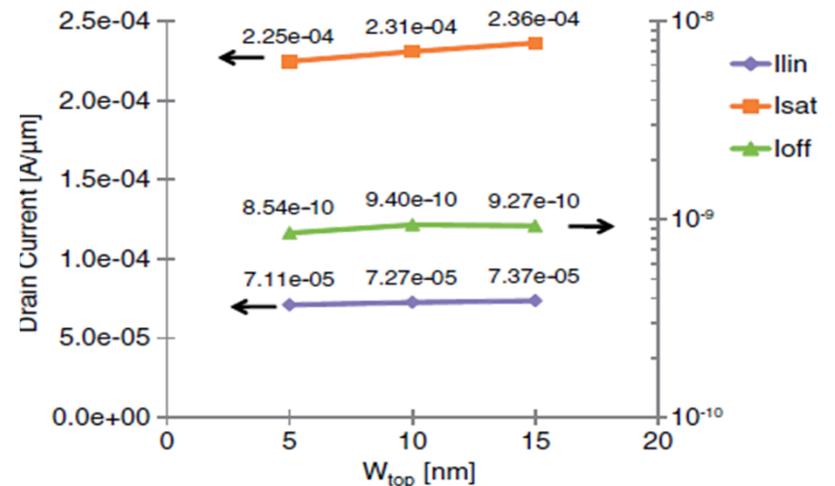
Nuo Xu

EE 290D, Fall 2013

## N-FinFET



## P-FinFET



Simulation Data from Synopsys Inc., (2013)

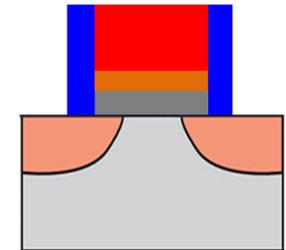
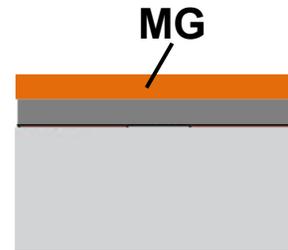
17

# High-κ/Metal Gate Technology

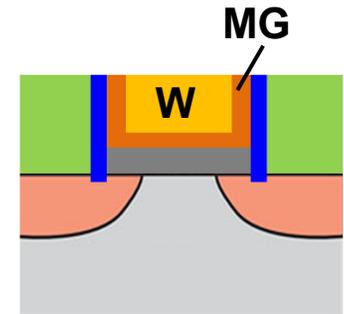
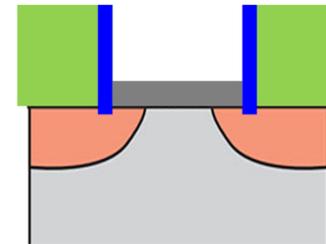
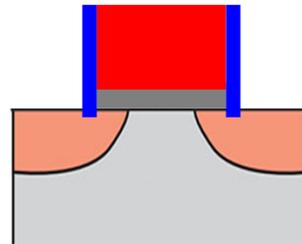
- SiN
- Low  $\kappa$
- High  $\kappa$
- Si
- Poly-Si
- Metal Gate
- W

Process Flow ➔

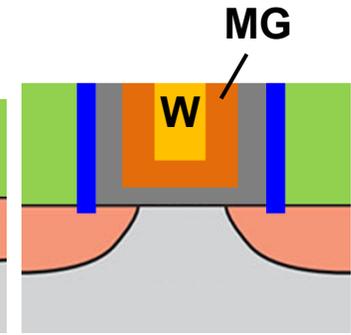
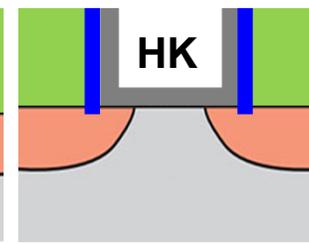
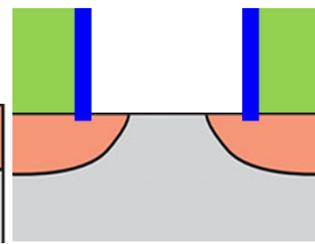
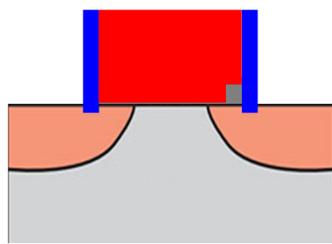
**Gate First / MIPS**  
(Metal-Inserted-Poly-Si Gate)



**High-κ First**

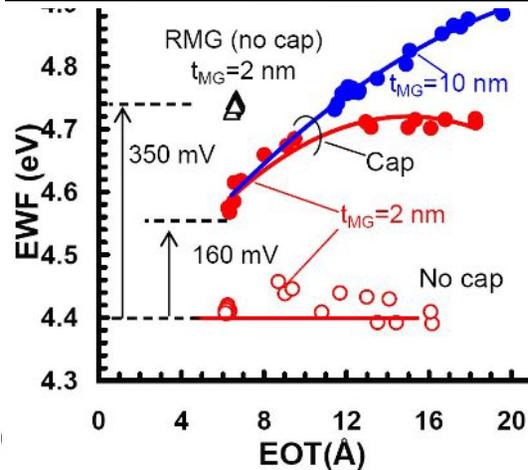


**Gate Last / RMG**  
(Replaced Metal Gate)

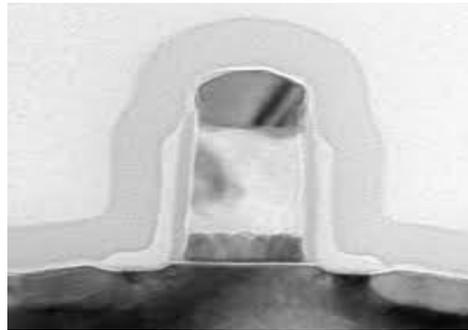


# Gate First vs. Gate Last

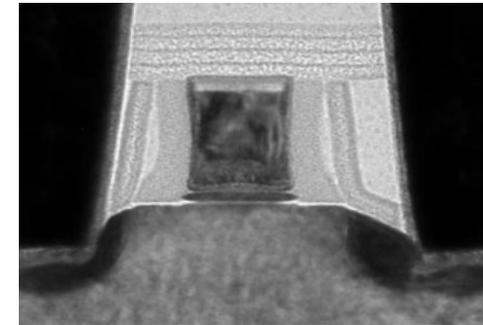
L. Ragnarsson, IEDM (2009)



**Gate-First (MIPS)**



**Gate-Last (RMG)**

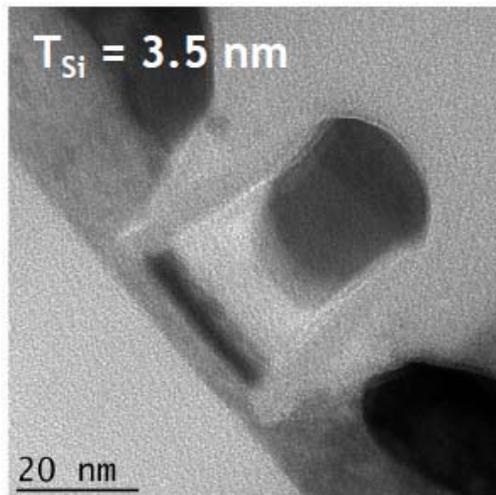


<b>High-κ Dielectric</b>	<b>First</b>	<b>First → Last</b>
<b>Metal Gate</b>	<b>First</b>	<b>Last</b>
<b>Thermal Budget</b>	<b>High</b>	<b>Low</b>
<b>EOT</b>	<b>Thick</b>	<b>Thin</b>
<b>Mobility</b>	<b>Low</b>	<b>High</b>
<b>Workfunction Control</b>	<b>Bad</b>	<b>Good</b>
<b>Cost</b>	<b>Low</b>	<b>High</b>
<b>Process Complexity</b>	<b>Low</b>	<b>High (CMP)</b>

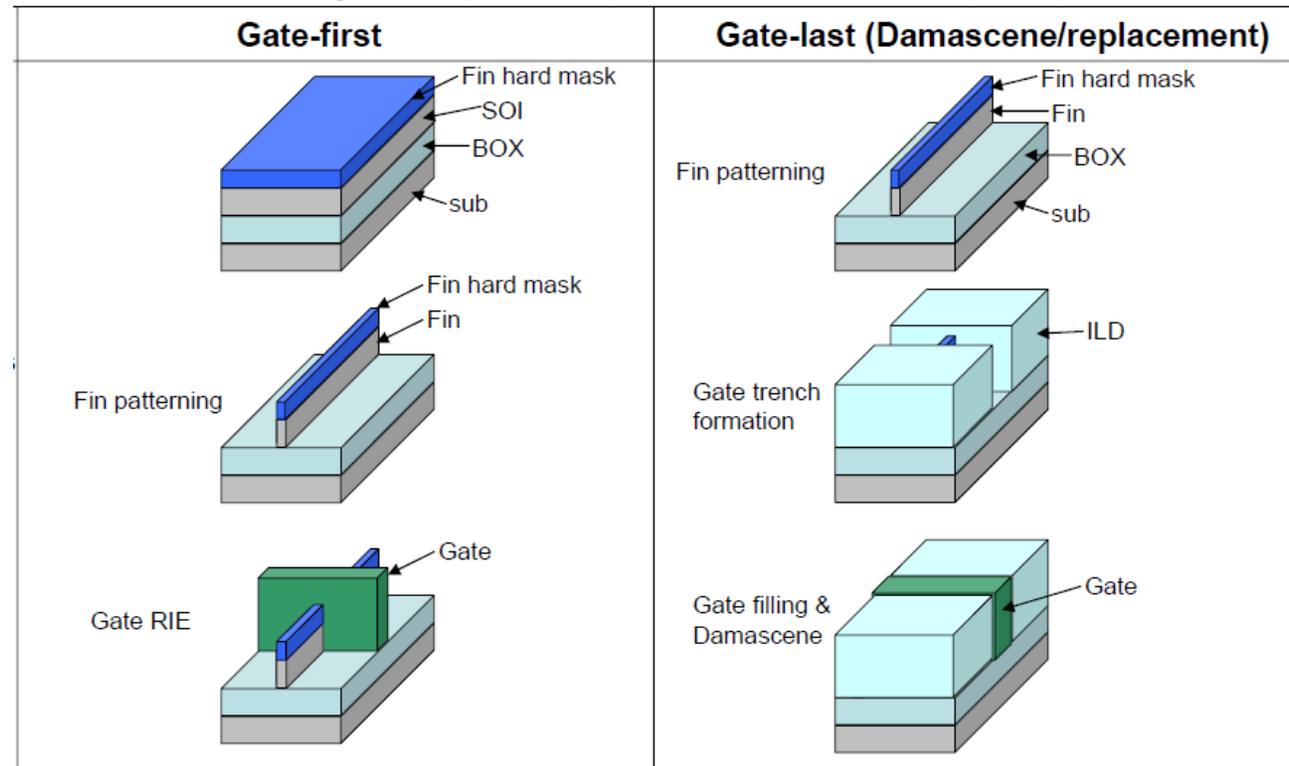
# Thin-Body MOSFET Gate Process

A. Yagishita (Toshiba), SOI Short Course (2009)

## IBM's ETSOI MOSFET



A. Khakifirooz, EDL (2012)



- Extremely-thin UTB SOI is not compatible with high- $\kappa$ -last process, due to the Si sacrifice during dummy (poly-Si) gate removal.
- FinFET RMG is challenging, due to the 3-D CMP process.
- **Cost is the dominant issue.**

# References

1. T. Hook, "FinFET Isolation Approaches and Ramifications: Bulk vs. SOI," *FDSOI Workshop at Hsinchu*, Taiwan, April, 2013.
2. A. Yagishita, "Process and Device Technologies for FinFET and Its Alternative Devices," *IEEE SOI Conference Short Course*, Foster City, CA, October, 2009.
3. X. Sun, T.-J. King Liu, "Spacer Gate Lithography for Reduced Variability due to Line Edge Roughness," *IEEE Transactions on Semiconductor Manufacturing*, Vol.23, No.2, pp.311-315, 2010.
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