EE 290D Module 1 Review - Device Physics

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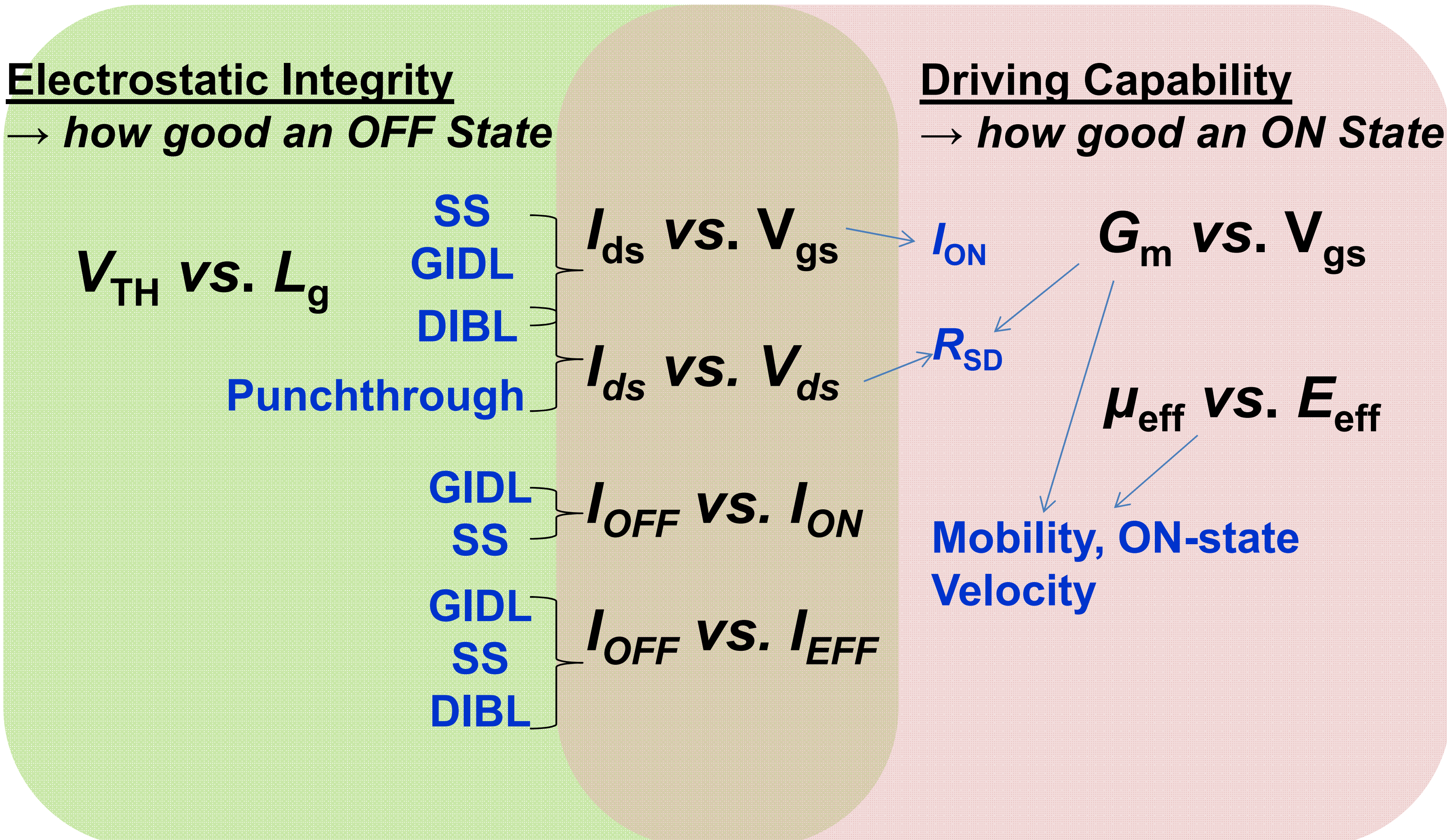
MOSFET Performance Metrics

- Mostly for Digital Logic Applications



Planar Bulk MOSFET

conventional devices are (100)/<110>

- **Solutions to reduce I_{OFF}**
  - Scale length: **(Lec.2)**

$$l = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} X_{dep}}$$

Increase N_{ch} → Use retrograde well doping or HALO
→ Use ultra-shallow-junctions (USJ)

- **Quantum confinement effect: (Lec.4)**
  - Quantum capacitance
  - Electrons show smaller T_{inv} than holes.
- **Sub-bands (Lec.4,5)**
  - Electrons: the lowest sub-bands from Δ_2 valleys.
  - Holes: the lowest sub-bands from HHs.
- **Carrier mobility: (Lec.5)**
  - Electron's mobility is 3 times the hole's.

Ultra-Thin-Body MOSFET

conventional devices are (100)/<110>

- **Solutions to reduce I_{OFF}** (Lec.3)
  - Scale length: $$l = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}}$$

Reduce Si body thickness → Reduce BOX thickness

- **Quantum confinement effect:** (Lec.4)
  - Electrons show smaller T_{inv} than holes.
- **Sub-bands** (Lec.4,5)
  - Electrons: the lowest sub-bands from Δ_2 valleys.
  - Holes: the lowest sub-bands from HHs.
- **Carrier mobility:** (Lec.5)
  - Electron's mobility is 3 times the hole's.

FinFET

conventional devices are (110)/<110>

- **Solutions to reduce I_{OFF}** **(Lec.3)**
  - scale length: $$l = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{ox} W_{Fin}}$$
- **Quantum confinement effect:** **(Lec.5)**
  - Holes show smaller T_{inv} than electrons.
- **Sub-bands** **(Lec.5)**
  - Electrons: the lowest sub-bands from Δ_4 valleys.
  - Holes: the lowest sub-bands from HHs, w/ smaller m^* than (100).
- **Carrier mobility:** **(Lec.5)**
  - E_{eff} is largely reduced compared to single gate FET.
  - Electron's mobility is comparable to hole's.
  - (100) N-FinFET (w/ 45^0 rotated layout) doesn't show performance advantage over (110) N-FinFETs (w/ conventional layout direction).

Short-Channel MOSFET General

- **Gate-Induced Drain Leakage (GIDL)** **(Lec.2, 3)**
  - Limiting the I_{OFF} to above 10pA/um.
  - Insensitive to L_g, sensitive to $L_{overlap}$
  - Sensitive to S/D junction doping steepness; FinFET should show better GIDL than planar bulk MOSFET w/ high channel doping.
- **Reverse Narrow Width Effect:** **(Lec.2)**
  - Good to enhance electrostatics, by the quasi-planar gate control
- **Apparent Mobility** **(Lec.5)**
  - Degrades with L_g scaling, due to gate or S/D edge defects.
  - The limiting velocities in Si MOSFET would still be saturation/drift velocities.
- **Series Resistance** **(Lec.5)**

High-κ Gate Dielectrics

- **Extra Scattering Mechanisms** **(Lec.4, 5)**
  - Remote coulomb scatterings will be enhanced for thin-body MOSFETs.
  - Remote phonon scatterings can be mitigated by using metal gate, and are no longer important in future CMOS technologies.

- ***EOT* and *EOT*$_{elec}$** **(Lec.4)**

Semiconductor Band Structure Theories

- **Qualitative understanding:** **(Lec.4)**
  - Effective mass: quantum-confinement and transport masses
  - Scattering types: (in-)elastic and intra-/inter-valleys
  - Scattering mechanisms: phonon, surface roughness, coulomb
  - Velocity saturation in Si is due to enhanced optical phonon emissions.