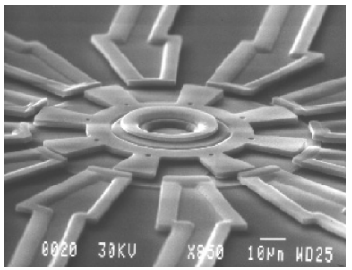
"Foundry" MEMS: The MUMPS Process

MUMPS: MultiUser MEMS ProcesS

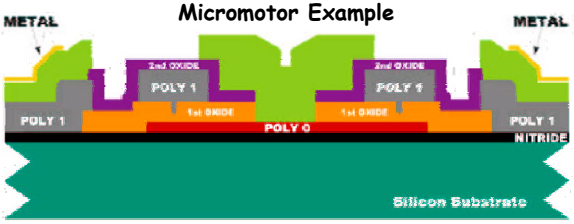
- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm^2 dies

Micromotor fabricated via MUMPS



MUMPS: MultiUser MEMS ProcesS

Micromotor Example



Material Layer	Thickness (μm)	Lithography Level Name
Nitride	0.6	--
Poly 0	0.5	POLY0 (HOLE0)
First Oxide	2.0	DIMPLE ANCHOR1
Poly 1	2.0	POLY1 (HOLE1)
Second Oxide	0.75	POLY1_POLY2_VIA ANCHOR2
Poly 2	1.5	POLY2 (HOLE2)
Metal	0.5	METAL (HOLEM)

Masks in polyMUMPS

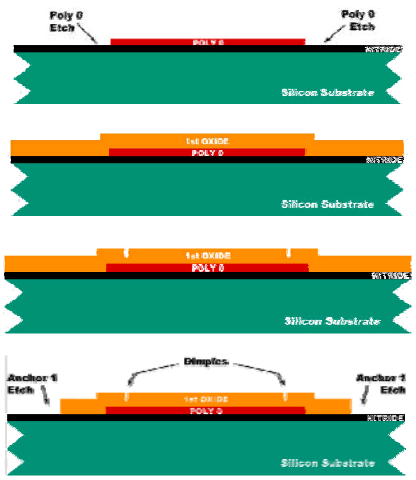
Minimum set of masks that must be used in MUMPS

Mnemonic level name	Field type	Purpose
POLY0	light	pattern ground plane
ANCHOR1	dark	open holes for Poly 1 to Nitride or Poly 0 connection
DIMPLE	dark	create dimples/bushings for Poly 1
POLY1	light	pattern Poly 1
POLY1_POLY2_VIA	dark	open holes for Poly 1 to Poly 2 connection
ANCHOR2	dark	open holes for Poly 2 to Nitride or Poly 0 connection
POLY2	light	pattern Poly 2
METAL	light	pattern Metal
HOLE0	dark	provide holes for POLY0
HOLE1	dark	provide release holes for POLY1
HOLE2	dark	provide release holes for POLY2
HOLEM	dark	provide release holes in METAL

Extra masks for more flexibility & ease of release

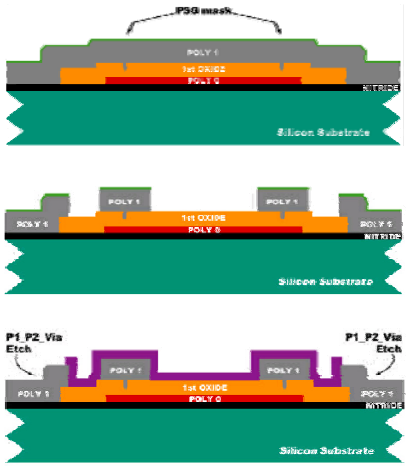
- Field type:
  - Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
  - Dark field (df): in layout, boxes represent holes to be cut out

MUMPS Process Flow



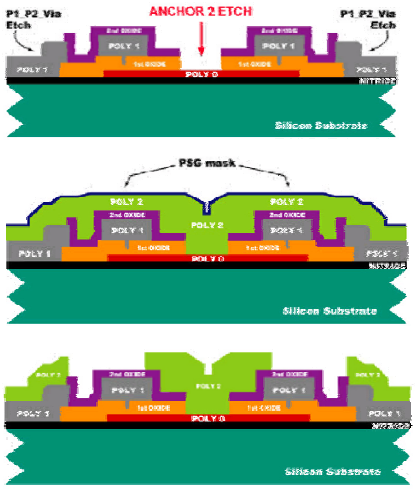
- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 μm of PSG as the 1st sacrificial layer
- Lithography using the DIMPLE(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1 (df) mask (align to poly0)
- RIE anchor vias down to the nitride surface

MUMPS Process Flow (cont.)



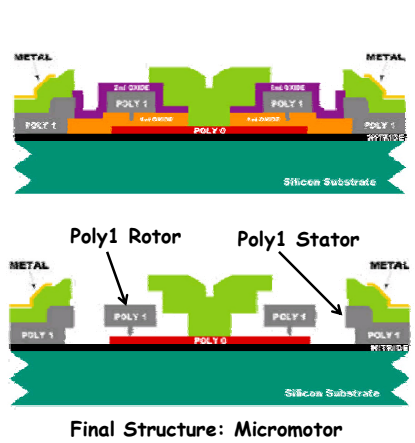
- LPCVD 2 μm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  - This both dopes the polysilicon and reduces its residual stress
- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then …
- RIE the polysilicon
- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA (df) mask to define contacts to the poly1 layer (align to poly1)

MUMPS Process Flow (cont.)



- Recoat with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings
- LPCVD 1.5 μm undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress
- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask

MUMPS Process Flow (cont.)



Final Structure: Micromotor

- Lithography using the METAL (df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer
- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed

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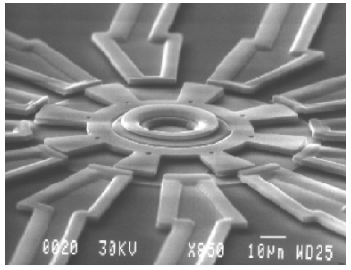
Micromotor fabricated via MUMPS



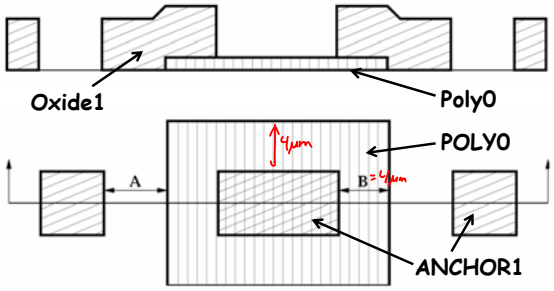
polyMUMPS Minimum Feature Constraints

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

	Nominal [μm]	Min Feature [μm]	Min Spacing [μm]
POLY0, POLY1, POLY2	3	2	2
POLY1_POLY2_VIA	3	2	2
ANCHOR1, ANCHOR2	3	3	2
DIMPLE	3	2	3
METAL	3	3	3
HOLE1, HOLE2	4	3	3
HOLEM	5	4	4

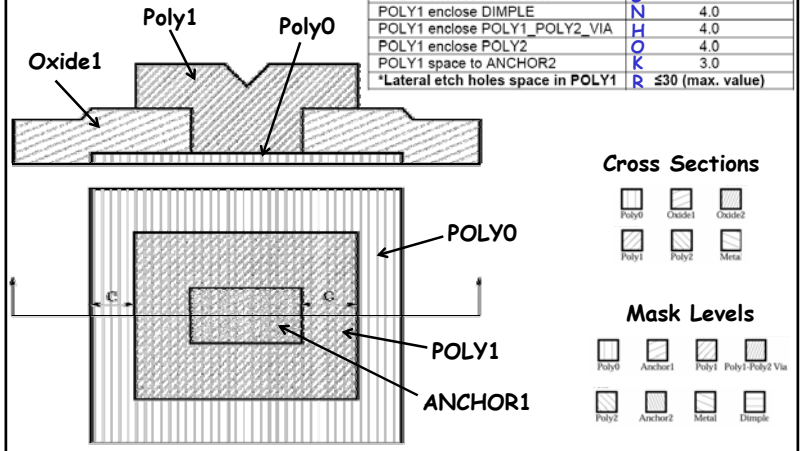
MUMPS Design Rules

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0



MUMPS Design Rules (cont.)

Rule		Min. Value (μm)
POLY1 enclose ANCHOR1	G	4.0
POLY1 enclose DIMPLE	N	4.0
POLY1 enclose POLY1_POLY2_VIA	H	4.0
POLY1 enclose POLY2	O	4.0
POLY1 space to ANCHOR2	K	3.0
*Lateral etch holes space in POLY1	R	≤30 (max. value)



MUMPS Design Rules (cont.)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY1 enclose ANCHOR1	G	2.6	4.0
POLY1 enclose DIMPLE	N	2.13	4.0
POLY1 enclose POLY1_POLY2_VIA	H	2.9, 2.11	4.0
POLY1 enclose POLY2	O	2.14	4.0
POLY1 space to ANCHOR2	K	2.11	3.0
*Lateral etch holes space in POLY1	R	2.15	≤30 (max. value)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY2 enclose ANCHOR2	J	2.7,2.10	5.0
POLY2 enclose POLY1_POLY2_VIA	L	2.9	4.0
POLY2 cut-in POLY1	P	2.14	5.0
POLY2 cut-out POLY1	Q	2.14	4.0
POLY2 enclose METAL	M	2.12	3.0
POLY2 space to POLY1	I	2.10	3.0
HOLE2 enclose HOLE1	T	2.16	2.0
HOLEM enclose HOLE2	U	2.16	2.0
*Lateral etch holes space in POLY2	S	2.15	≤30 (max. value)

MUMPS Design Rules (cont.)

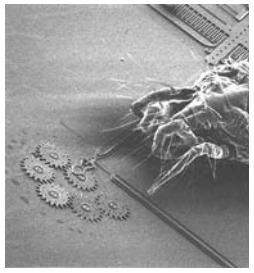
Level 1	Level 2	Min. Feature	Min. Spacing	Enclose	Spacing	Cut- In	Cut- Out
POLY0	-	2	2				
	ANCHOR1			4/B/2.5	4/A/2.5		
	POLY1			4/C/2.6			
	ANCHOR2			5/E/2.8	5/F/2.8		
	POLY2			5/D/2.7			
POLY1	-	2	2 / 2.5[4]				
	POLY0						
	ANCHOR1			4/G/2.6			
	ANCHOR2				3/K/2.11		
	POLY2			4/0/2.14			
	DIMPLE			4/N/2.13			
	POLY1_POLY2_VIA			4/H/2.9			
POLY2	-	2	2 / 2.5[2]				
	POLY0						
	POLY1				3/I/2.10	5/P/2.14	4/Q/2.14
	VIA			4/L/2.9			
	ANCHOR2			5/J/2.7			
	METAL			3/M/2.12			
HOLEM	HOLE2			2/U/2.16			
HOLE2	HOLE1			2/T/2.16			

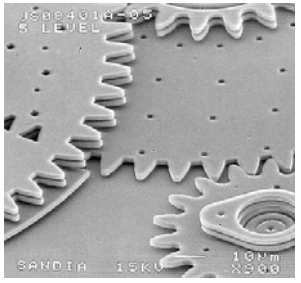
TABLE 2.7. PolyMUMPs design rule reference sheet. Table shows minimum dimensions (μm), rule name, and figure number, respectively.

The Sandia SUMMIT Process

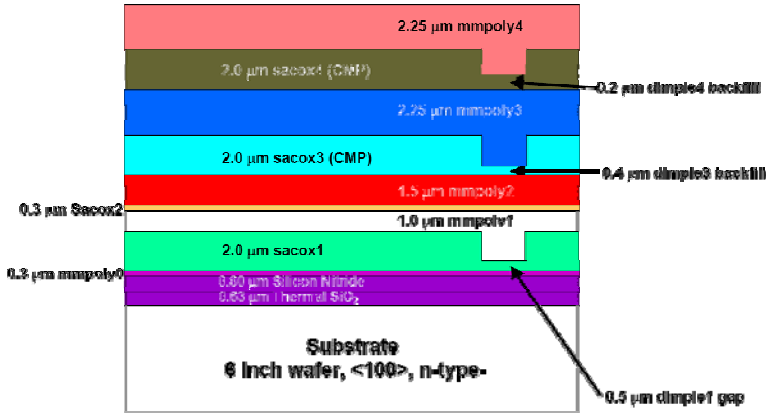
Sandia's SUMMiT V

- SUMMiT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process
  - Five-layer polysilicon surface micromachining process
  - One electrical interconnect layer & 4 mechanical layers
  - Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  - 14 masks





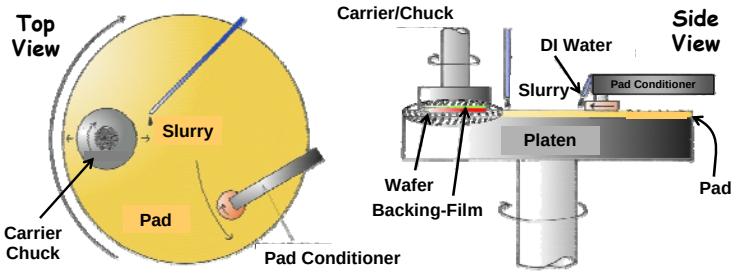
SUMMiT V Layer Stack



- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized

Chemical Mechanical Polishing (CMP)

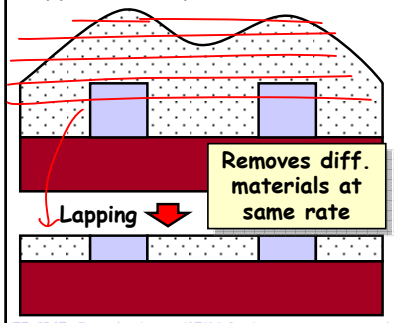
- Used to planarize the top surface of a semiconductor wafer or other substrate
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad
  - Wafer and pad are pressed together
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing



CMP: Not the Same as Lapping

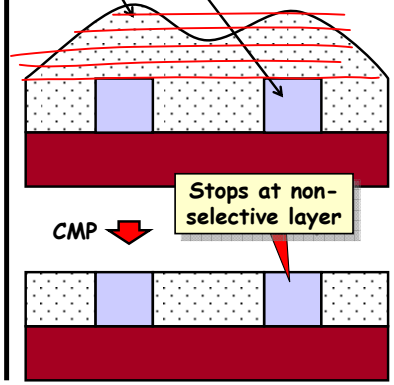
Lapping

- Lapping is merely the removal of material to flatten a surface without selectivity
- Everything is removed at approximately the same rate

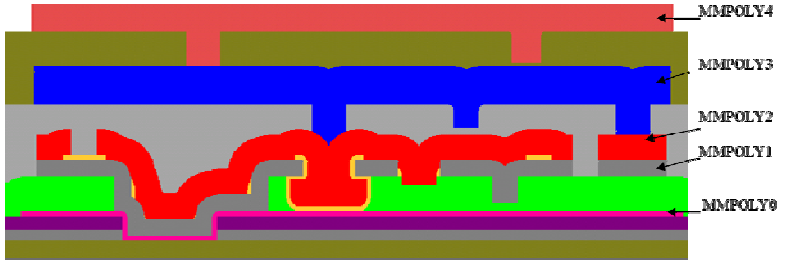


Chemical Mechanical Polishing

- CMP is selective to certain films, and not selective to others



Actual SUMMiT Cross-Section



- No CMP until after the first three polySi layers
- 1 µm mmpoly1 and 1.5 µm mmpoly2 can be combined to form a 2.5 µm polysilicon film
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions

EE C245 – ME C218
Introduction to MEMS Design
Fall 2009

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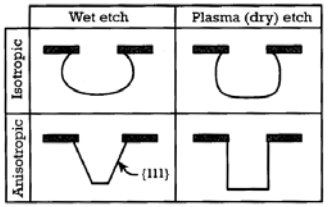
Lecture Module 6: Bulk Micromachining

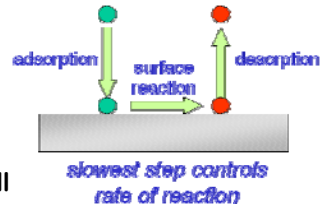
Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - Bulk Micromachining
  - Anisotropic Etching of Silicon
  - Boron-Doped Etch Stop
  - Electrochemical Etch Stop
  - Isotropic Etching of Silicon
  - Deep Reactive Ion Etching (DRIE)

Bulk Micromachining

- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - Isotropic vs. anisotropic
  - Reaction-limited
    - Etch rate dep. on temp.
  - Diffusion-limited
    - Etch rate dep. on mixing
    - Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - Desired shape
  - Etch depth and uniformity
  - Surface roughness (e.g., sidewall roughness after etching)
  - Process compatiblity (w/ existing layers)
  - Safety, cost, availability, environmental impact



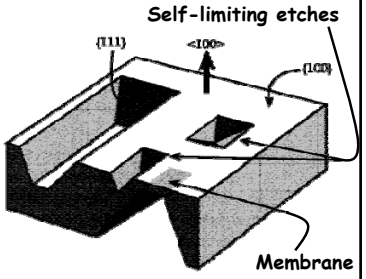


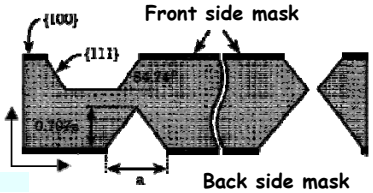
Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength,at which point it breaks.
  - Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm²)
  - Young's Modulus near that of stainless steel
  - {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - Mechanical properties uniform, no intrinsic stress
  - Mechanical integrity up to 500°C
  - Good thermal conductor
  - Low thermal expansion coefficient
  - High piezoresistivity

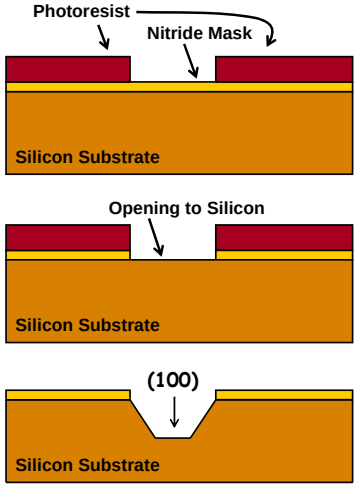
Anisotropic Etching of Silicon

- Etching of Si w/ KOH
  - $Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-$
  - $4H_2O + 4e^- \rightarrow 4(OH)^- + 2H_2$
- Crystal orientation dependent etch rates
  - {110}:{100}:{111}=600:400:1
  - {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
  - {111} plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
  - {111} forms protective oxide
  - {111} smoother than other crystal planes → good for optical MEMS (mirrors)



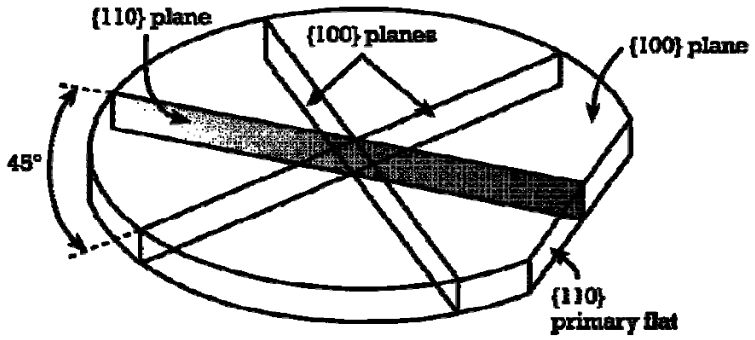


Anisotropic Etching of Silicon



- Deposit nitride:
  - Target = 100nm
  - 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - RIE using SF_6
  - Remove PR in PRS2000
- Etch the silicon
  - Use 1:2 KOH:H_2O (wt.), stirred bath @ 80°C
  - Etch Rates:
    - (100) Si → 1.4 μm/min
    - Si_3N_4 → ~ 0 nm/min
    - SiO_2 → 1-10 nm/min
    - Photoresist, Al → fast
- Micromasking by H_2 bubbles leads to roughness
  - Stir well to displace bubbles
  - Can also use oxidizer for (111) surfaces
  - Or surfactant additives to suppress bubble formation

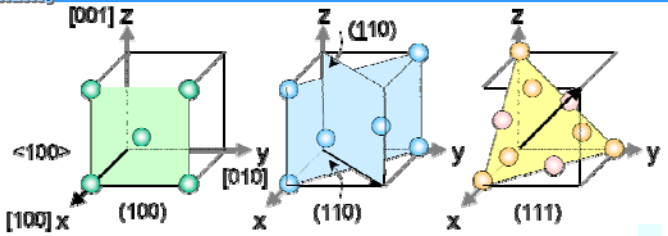
Silicon Wafers



{100} type wafer

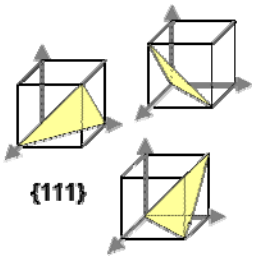
[Maluf]

Silicon Crystallography

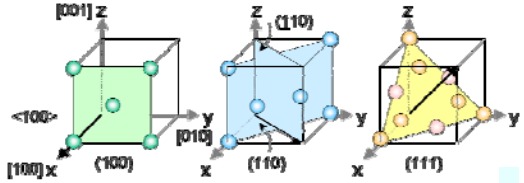


Miller Indices (h k l):

- Planes
  - Reciprocal of plane intercepts with axes
  - e.g., for (110), intercepts: (x,y,z) = (1,1,∞); reciprocals: (1,1,0) → (110)
  - (unique), {family}
- Directions
  - One endpoint of vector @ origin
  - [unique], <family>



Determining Angles Between Planes



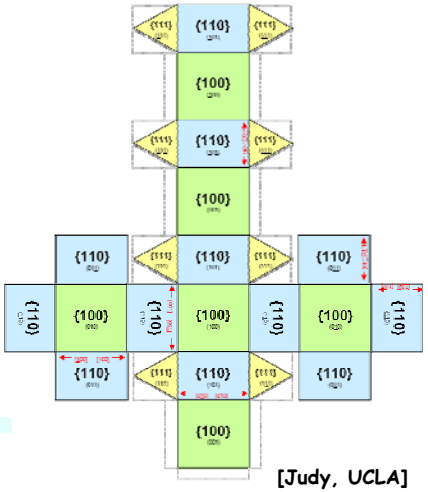
- The angle between vectors [abc] and [xyz] is given by:

$$ax + by + cz = \left|(a,b,c)\right| \cdot \left|(x,y,z)\right| \cdot \cos\theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1}\left[\frac{ax + by + cz}{\left|(a,b,c)\right| \cdot \left|(x,y,z)\right|}\right]$$

- For {100} and {110} → 45°
- For {100} and {111} → 54.74°
- For {110} and {111} → 35.26°, 90°, and 144.74°

Silicon Crystal Origami

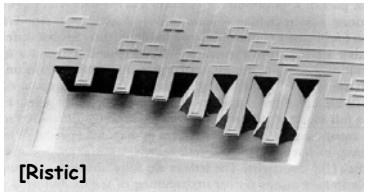


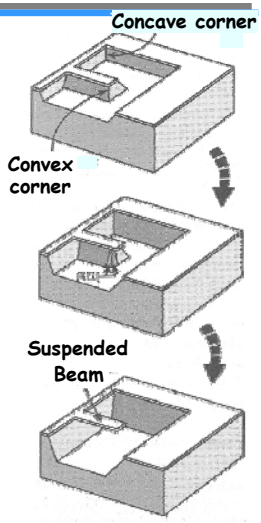
- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
- Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]

Undercutting Via Anisotropic Si Etching

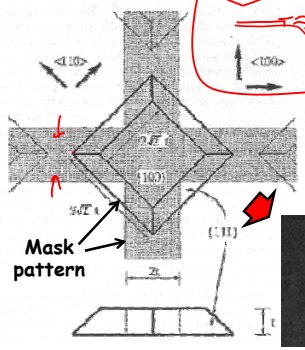
- Concave corners bounded by {111} are not attacked
- … but convex corners bounded by {111} are attacked
  - Two {111} planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
  - Result: can undercut regions around convex corners

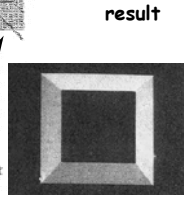


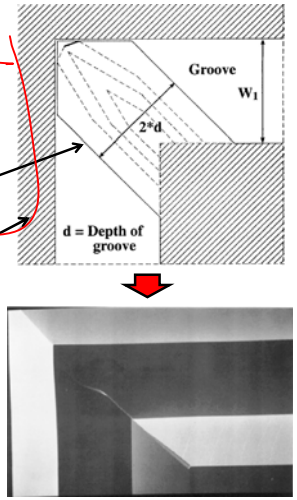


Corner Compensation

- Protect corners with "compensation" areas in layout
- Below: Mesa array for self-assembly structures [Smith 1995]







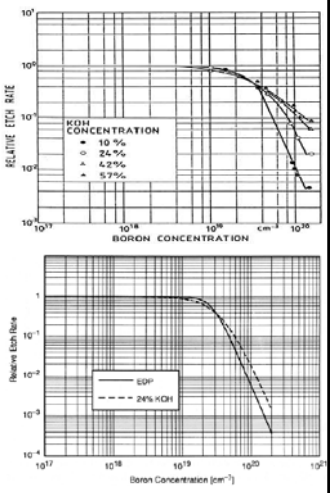
Other Anisotropic Silicon Etchants

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - Etch rate (100) = 0.5-1.5 μm/min
  - Al safe, IC compatible
  - Etch ratio (100)/(111) = 10-35
  - Etch masks: SiO_2 , $Si3N_4$ ~ 0.05-0.25 nm/min
  - Boron doped etch stop, up to 40× slower
- EDP (115°C)
  - Carcinogenic, corrosive
  - Etch rate (100) = 0.75 μm/min
  - Al may be etched
  - R(100) > R(110) > R(111)
  - Etch ratio (100)/(111) = 35
  - Etch masks: SiO_2 ~ 0.2 nm/min, Si_3N_4 ~ 0.1 nm/min
  - Boron doped etch stop, 50× slower

Boron-Doped Etch Stop

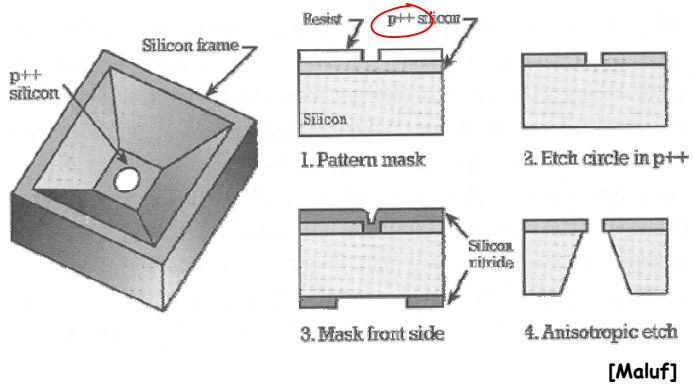
Boron-Doped Etch Stop

- Control etch depth precisely with boron doping (p++)
  - [B] > 10^{20} cm^{-3} reduces KOH etch rate by 20-100×
  - Can use gaseous or solid boron diffusion
  - Recall etch chemistry:
    $Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-$
    $4H_2O + 4e^- \rightarrow 4(OH)^- + 2H_2$
  - At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH^-
- Result:
  - Beams, suspended films
  - 1-20 μm layers possible



Ex: Micronozzle

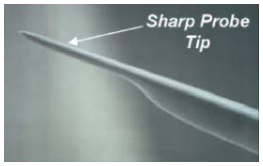
- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

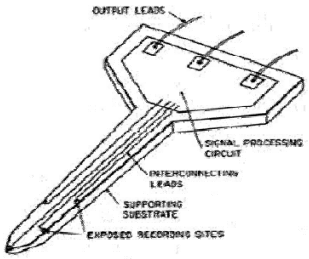


[Maluf]

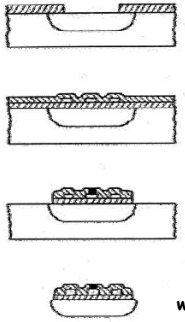
Ex: Microneedle

- Below: micro-neurostimulator
  - Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
- Wise Group, Univ. of Michigan





Multi-Channel Recording Array Structure



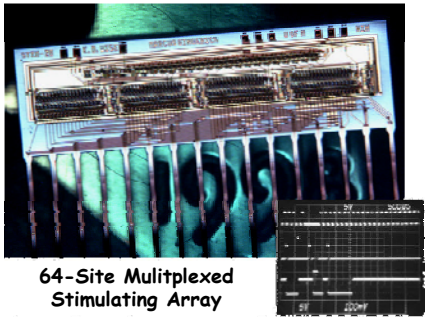
Selectively diffuse p++ into substrate

Deposit interconnect pattern and insulate conductors

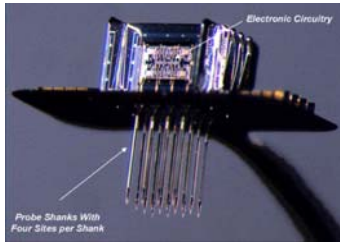
Pattern dielectric and metallize recording sites

Dissolve away the wafer (no mask needed)

Ex: Microneedles (cont.)



64-Site Mulitplexed Stimulating Array



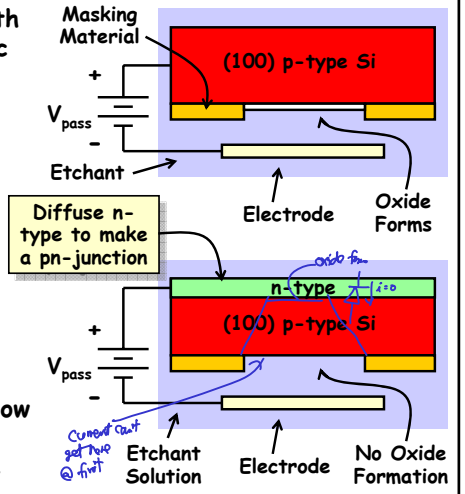
[Wise, U. of Michigan]

- Micromachined with on-chip CMOS electronics
- Both stimulation and recording modes
- 400 mm site separations, extendable to 3D arrays
- Could be key to neural prosthesis systems focusing on the central nervous system

Electrochemical Etch Stop

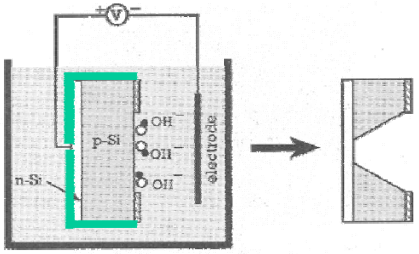
Electrochemical Etch Stop

- When silicon is biased with a sufficiently large anodic potential relative to the etchant → get oxidation (i.e., electrochemical passivation), which then prevents etching
- For passivation to occur, current flow is required
- If current flow can be prevented → no oxide growth, and etching can proceed
  - Can prevent current flow by adding a reverse-biased diode structure



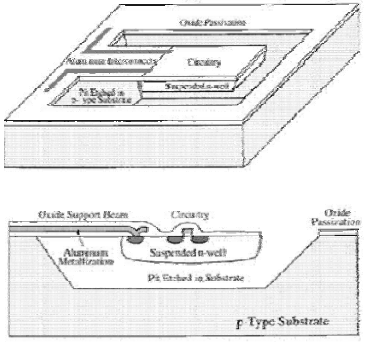
Electrochemical Etch Stop

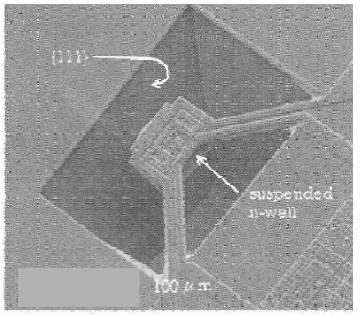
- Electrochemical etch stop
  - n-type epitaxial layer grown on p-type wafer forms p-n junction diode
  - $V_p > V_n \rightarrow$ electrical conduction (current flow)
  - $V_p < V_n \rightarrow$ reverse bias current (very little current flow)
- Passivation potential: potential at which thin SiO_2 film forms
  - different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- Setup:
  - p-n diode in reverse bias
  - p-substrate floating → etched
  - n-layer above passivation potential → not etched



Electrochemical Etching of CMOS

- N-type Si well with circuits suspended f/ SiO_2 support beam
- Thermally and electrically isolated
- If use TMAH etchant, Al bond pads safe

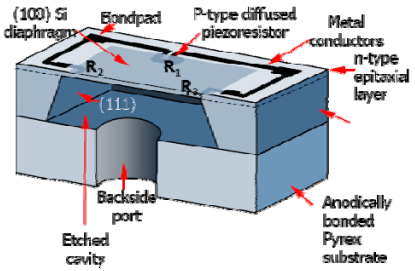


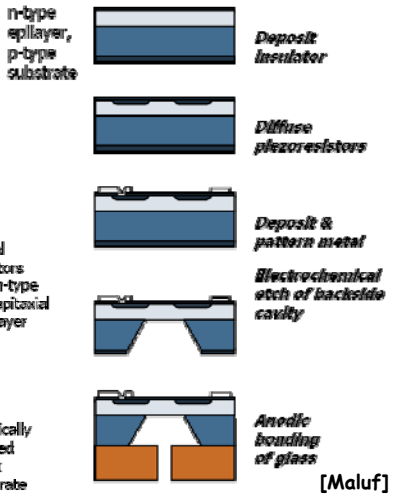


[Reay, et al. (1994)]
[Kovacs Group, Stanford]

Ex: Bulk Micromachined Pressure Sensors

- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection < 1 μm

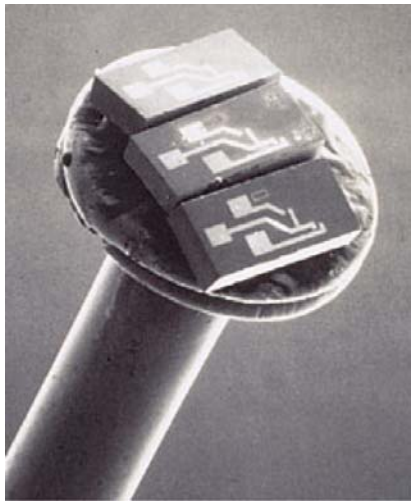




[Maluf]

Ex: Pressure Sensors

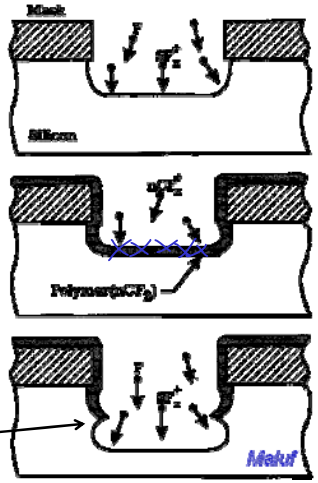
- Below: catheter tip pressure sensor [Lucas NovaSensor]
  - Only 150×400×900 μm³



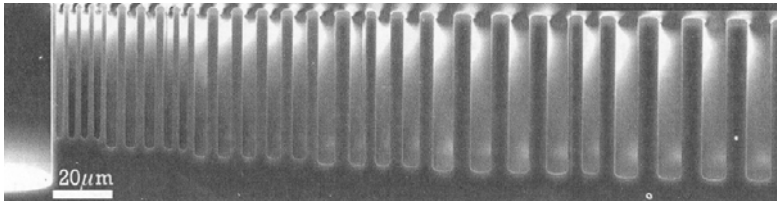
Deep Reactive-Ion Etching (DRIE)

The Bosch process:

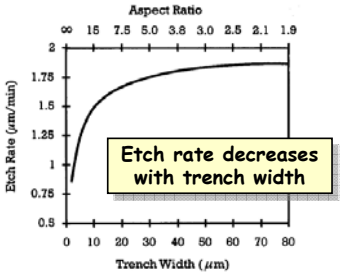
- Inductively-coupled plasma
- Etch Rate: 1.5-4 μm/min
- Two main cycles in the etch:
  - Etch cycle (5-15 s): SF_6 (SF_x^+) etches Si
  - Deposition cycle: (5-15 s): C_4F_8 deposits fluorocarbon protective polymer $(CF_2^-)_n$
- Etch mask selectivity:
  - SiO_2 ~ 200:1
  - Photoresist ~ 100:1
- Issue: finite sidewall roughness
  - scalloping < 50 nm
- Sidewall angle: 90° ± 2°



DRIE Issues: Etch Rate Variance

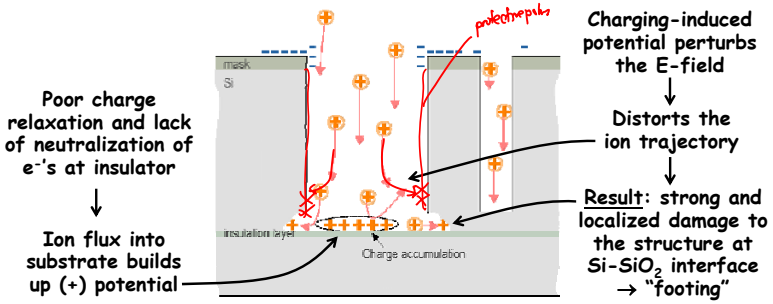


- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)



DRIE Issues: "Footing"

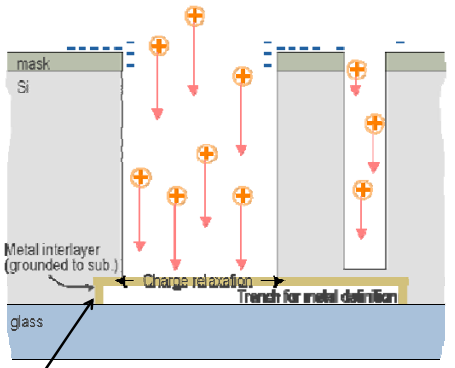
- Etch depth precision
  - Etch stop: buried layer of SiO_2
  - Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- Problem: Lateral undercut at Si/SiO_2 interface → "footing"
  - Caused by charge accumulation at the insulator



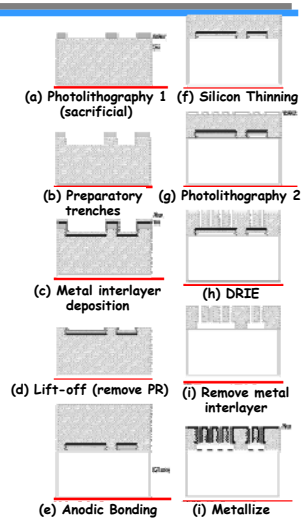
Recipe-Based Suppression of "Footing"

- Use higher process pressure to reduce ion charging [Nozawa]
  - High operating pressure → concentration of (-) ions increases and can neutralize (+) surface charge
  - Issue: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- Adjust etch recipe to reduce overetching [Schmidt]
  - Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
  - Issue: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use lower frequency plasma to avoid surface charging [Morioka]
  - Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - Allows e^-'s to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench

Metal Interlayer to Prevent "Footing"



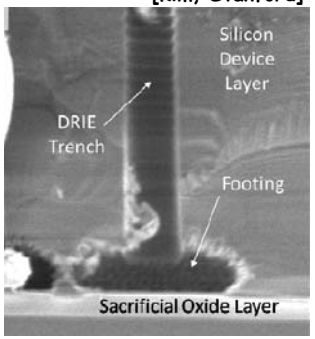
Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

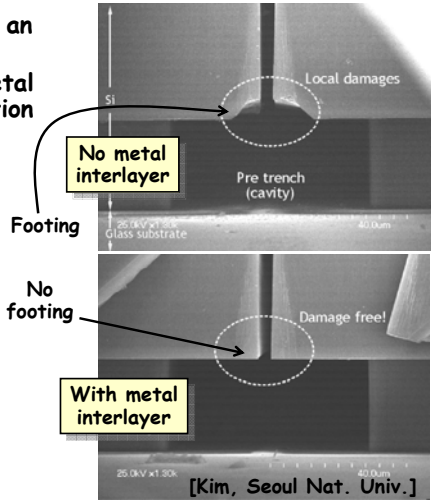


Footing Prevention (cont.)

- Below: DRIE footing over an oxide stop layer
- Right: efficacy of the metal interlayer footing prevention approach

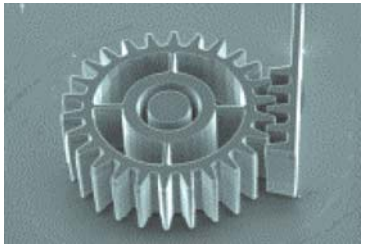
[Kim, Stanford]





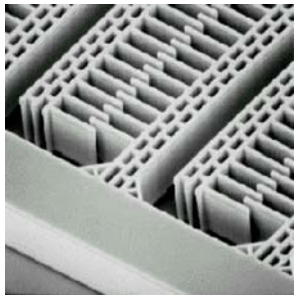
[Kim, Seoul Nat. Univ.]

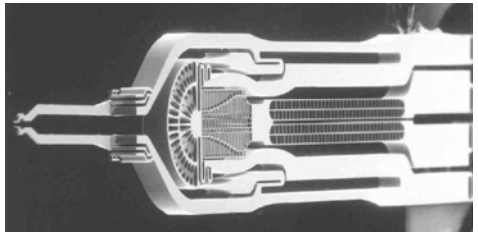
DRIE Examples



High aspect-ratio gear

Tunable Capacitor [Yao, Rockwell]



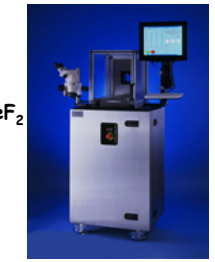


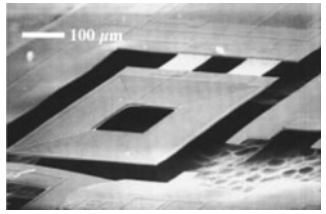
Microgripper [Keller, MEMS Precision Instruments]

Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride (XeF_2)
  $2XeF_{2(g)} + Si_{(s)} \rightarrow 2Xe_{(g)} + SiF_{4(g)}$
- Set-up:
  - Xe sublimes at room T
  - Closed chamber, 1-4 Torr
  - Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 μm/min, isotropic
- Etch masks: photoresist, SiO_2, Si_3N_4, Al, other metals
- Issues:
  - Etched surfaces have granular structure, 10 μm roughness
  - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

Xactix XeF_2 Etcher

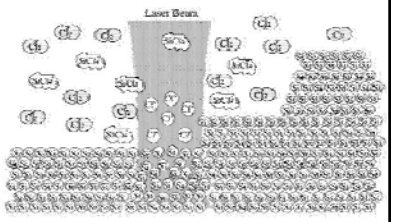




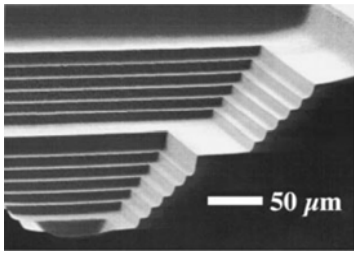
Inductor w/ no substrate [Pister]

Laser-Assisted Chemical Etching

- Laser creates Cl radicals from Cl_2 → reaction forms $SiCl_2$
- Etch rate: 100,000 μm³/s
  - Takes 3 min. to etch 500×500×125 μm³ trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file



- At right:
  - Laser assisted etching of a 500x500 μm² terraced silicon well
  - Each step is 6 μm-deep



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