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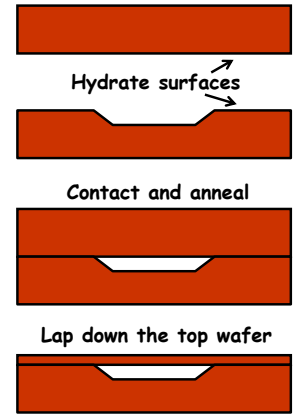
Wafer Bonding

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Fusion Bonding

- Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces
- Procedure:**
 - Prepare surfaces: must be smooth and particle-free
 - Clean & hydrate: O_2 plasma, hydration, or HF dip
 - When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together
 - Anneal at $600-1200^\circ C$ to bring the bond to full strength
- Result:** a bond as strong as the silicon itself!



Hydrate surfaces

Contact and anneal

Lap down the top wafer

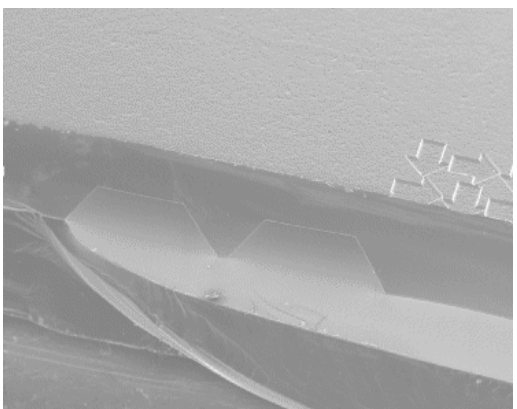
Works for Si-to-Si bonding and Si-to- SiO_2 bonding

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Fusion Bonding Example

- Below:** capacitive pressure sensor w/ fusion-bonded features



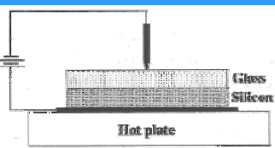
[Univ. of Southampton]

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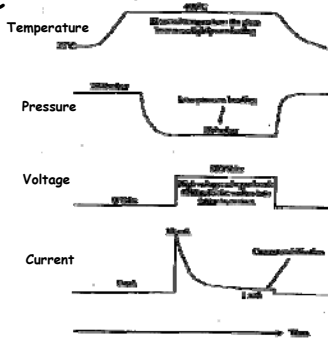
Anodic Bonding

- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:**
 - Press Si and glass together
 - Elevate temperature: $180-500^\circ C$
 - Apply (+) voltage to Si: 200-1500V
 - (+) voltage repels Na^+ ions from the glass surface
 - Get net (-) charge at glass surface
 - Attractive force between (+) Si and (-) glass \rightarrow intimate contact allows fusing at elevated temp.
 - Current drops to zero when bonding is complete



Hot plate

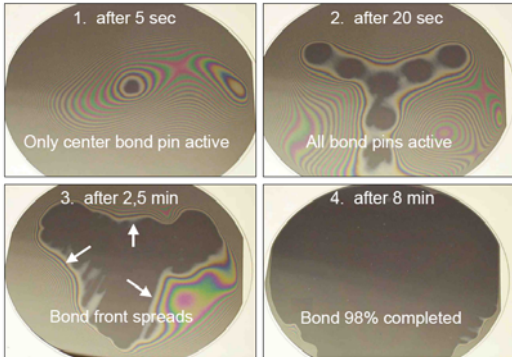
Glass Silicon



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Anodic Bonding (cont.)

- Advantage:** high pressure of electrostatic attraction smooths out defects
- Below:** 100 mm wafers, Pyrex glass 500 μm -thick, 430°C, 800V, N_2 @ 1000 mbar



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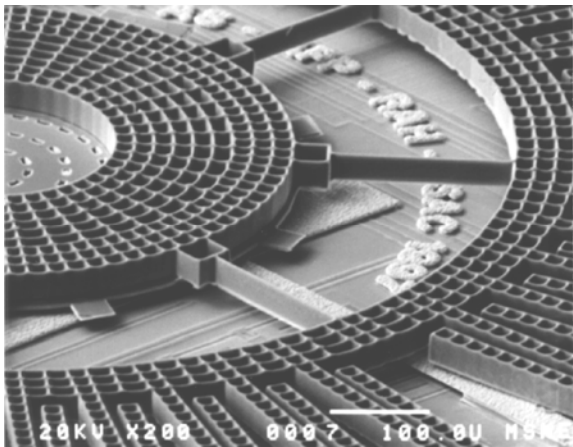
Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- Eutectic bonding**
 - Uses eutectic point in metal-Si phase diagrams to form silicides
 - Au and Si have eutectic point at 363°C
 - Low temperature process
 - Can bond slightly rough surfaces
 - Issue:** Au contamination of CMOS
- Solder bonding**
 - PbSn (183°C), AuSn (280°C)
 - Lower-T process
 - Can bond very rough surfaces
 - Issue:** outgassing (not good for encapsulation)
- Thermocompression**
 - Commonly done with electroplated Au or other soft metals
 - Room temperature to 300°C
 - Lowest-T process
 - Can bond rough surfaces with topography

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Thermocompression Bonding

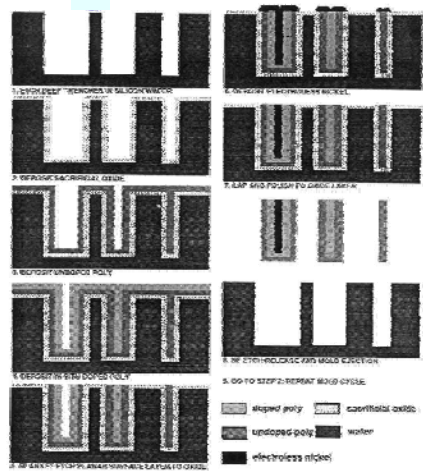
- Below:** Transfer of hexsil actuator onto CMOS wafer



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Hexsil MEMS

- Achieves high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Design with honeycomb structure for strength

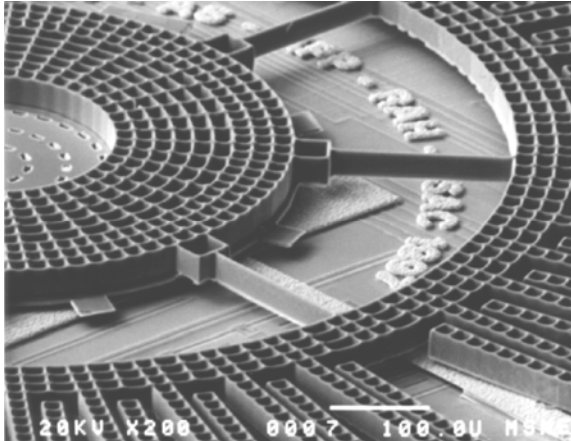


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Hexsil MEMS Actuator

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- Below: Transfer of hexsil actuator onto CMOS wafer



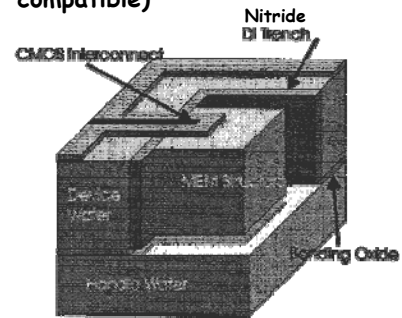
[Singh, et al, Transducers'97]

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Silicon-on-Insulator (SOI) MEMS

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- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

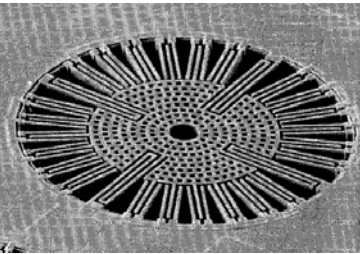


	Cross Section	Top View
Silicon		
SiO ₂		
SOI starting material		
Silicon		
Nitride		
Trench and Backfill		
Integrated Circuitry		
Structure definition and release		

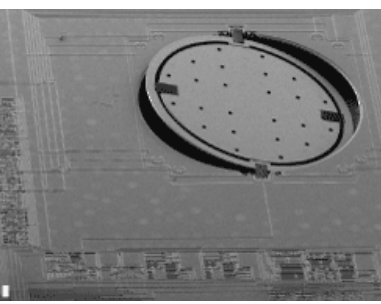
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SOI MEMS Examples

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Micromirror [Analog Devices]



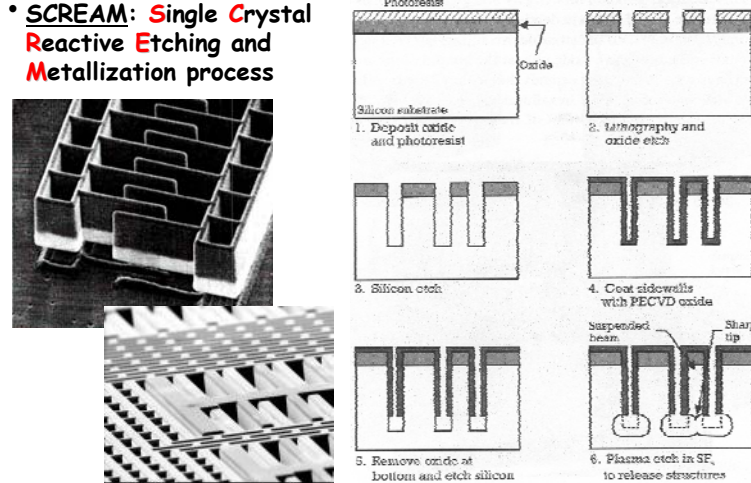
[Brosnihan]

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The SCREAM Process

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- SCREAM: Single Crystal Reactive Etching and Metallization process



1. Deposit oxide and photoresist
2. Lithography and oxide etch
3. Silicon etch
4. Coat sidewalls with PECVD oxide
5. Remove oxide at bottom and etch silicon
6. Plasma etch in SF₆ to release structures

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