EE C245 – ME C218
Introduction to MEMS Design
Fall 2011

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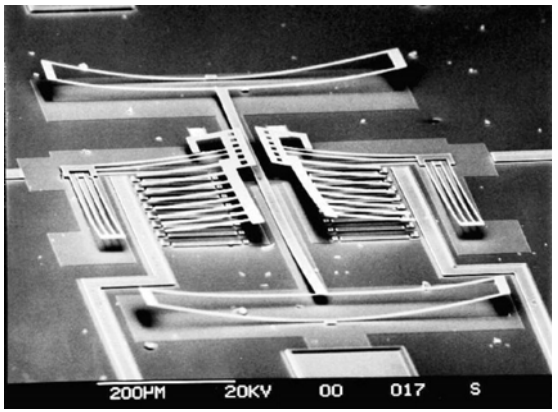
Lecture Module 5: Surface Micromachining

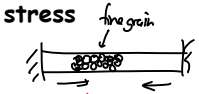
Vertical Stress Gradients

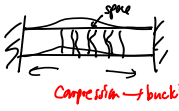
- Variation of residual stress in the direction of film growth
- Can warp released structures in z-direction



Stress in Polysilicon Films

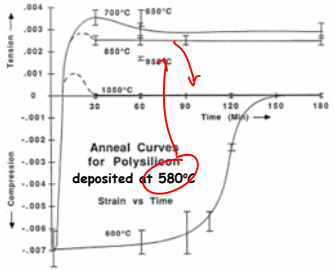
- Stress depends on crystal structure, which in turn depends upon the deposition temperature
- Temperature ≤ 600°C
  - Films are initially amorphous, then crystallize
  - Get equiaxed crystals, largely isotropic
  - Crystals have higher density → tensile stress
  - Small stress gradient
- Temperature ≥ 600°C
  - Columnar crystals grow during deposition
  - As crystals grow vertically and in-plane they push on neighbors → compressive stress
  - Positive stress gradient

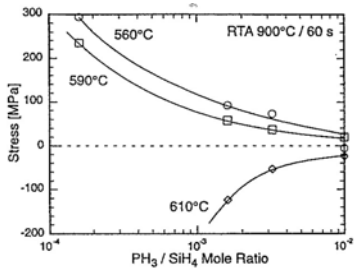




Annealing Out Polysilicon Stress

- Control polySi stress by annealing at high temperatures
  - Typical anneal temperatures: 900-1150°C
  - Grain boundaries move, relax
  - Can dope while annealing by sandwiching the polysilicon between similarly doped oxides (symmetric dopant drive-in), e.g. using 10-15 wt. % PSG

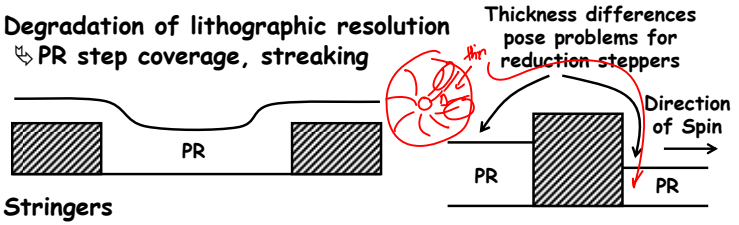




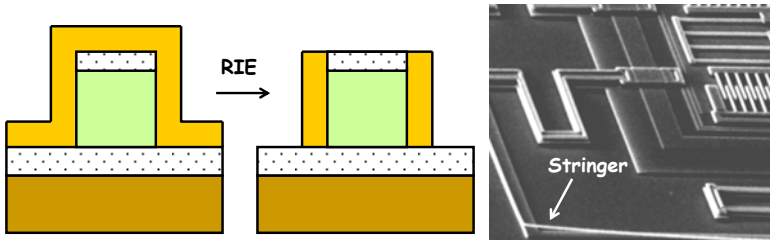
- Rapid thermal anneal (RTA) also effective (surprisingly)

Topography Issues

- Degradation of lithographic resolution
  - PR step coverage, streaking

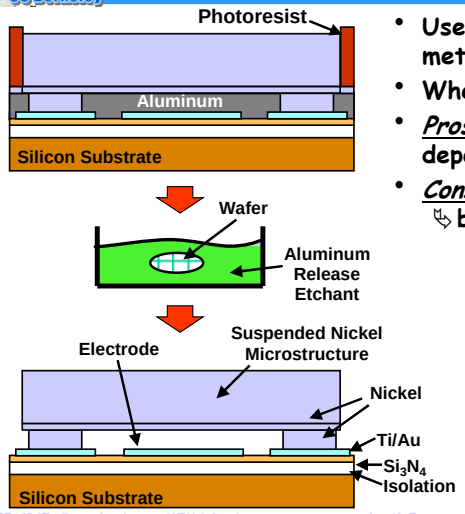


- Stringers
  - Problematic when using anisotropic etching, e.g., RIE

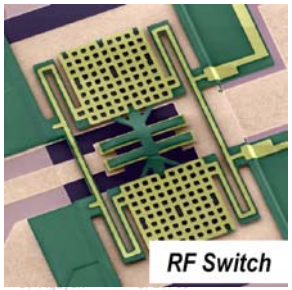


Nickel Surface-Micromachining Process Flow

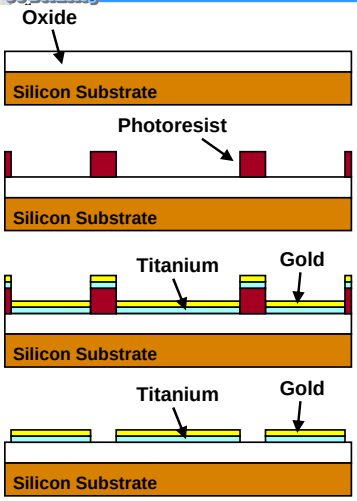
Electroplating: Metal MEMS



- Use electroplating to obtain metal μstructures
- When thick: call it "LIGA"
- *Pros*: fast low temp deposition, very conductive
- *Cons*: drift, low mech. *Q*
  - but may be solvable?

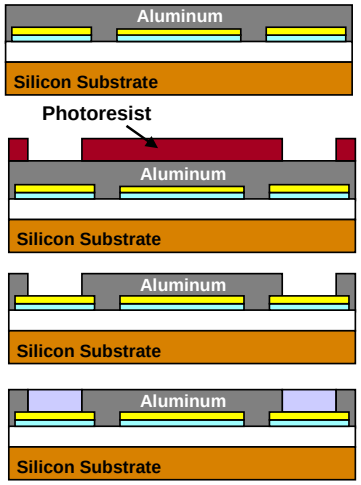


Nickel Metal Surface-Micromachining



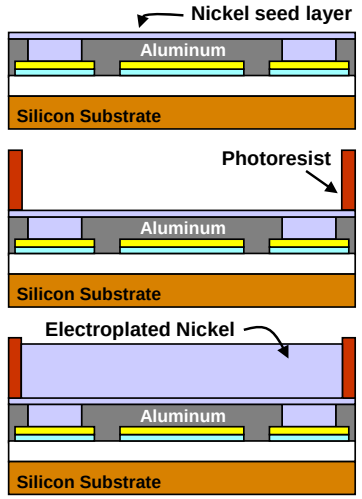
- Deposit isolation LTO:
  - Target = 2μm
  - 1 hr. 40 min. LPCVD @450°C
- Densify the LTO
  - Anneal @950°C for 30 min.
- Define metal interconnect via lift-off
  - Spin photoresist and pattern lithographically to open areas where interconnect will stay
  - Evaporate a Ti/Au layer
    - Target = 30nm Ti
    - Target = 270nm Au
  - Remove photoresist in PRS2000→ Ti/Au atop the photoresist also removed

Nickel Metal Surface-Micromachining



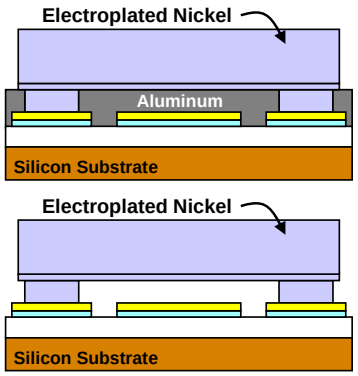
- Evaporate Al to serve as a sacrificial layer
  - Target = 1μm
- Lithography to define anchor openings
- Wet etch the aluminum to form anchor vias
  - Use solution of $H_3PO_4/HNO_3/H_2O$
- Remove photoresist in PRS2000
- Electroplate nickel to fill the anchor vias
  - Use solution of nickel sulfamate @ 50°C
  - Time the electroplating to planarize the surface

Nickel Metal Surface-Micromachining



- Evaporate a thin film of nickel to serve as a seed layer for subsequent Ni electroplating
  - Target = 20nm
- Form a photoresist mold for subsequent electroplating
  - Spin 6 um-thick AZ 9260 photoresist
  - Lithographically pattern the photoresist to delineate areas where nickel structures are to be formed
- Electroplate nickel structural material through the PR mold
  - Use a solution of nickel sulfamate @ 50°C
  - Cathode-to-anode current density ~ 2.5 mA/cm²

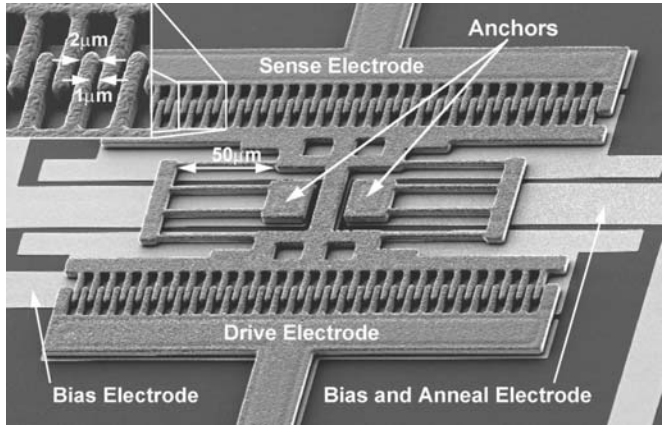
Nickel Metal Surface-Micromachining



- Strip the PR in PRS2000
- Remove the Ni seed layer in Ni wet etchant
- Release the structures
  - Use a $K_4Fe(CN)_6/NaOH$ etchant that attacks Al while leaving Ni and Au intact
  - Etch selectivity > 100:1 for Al:Ni and Al:Au

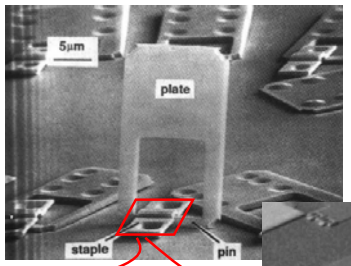
Nickel Surface-Micromachining Example

- Below: Surface-micromachined in nickel using the described process flow



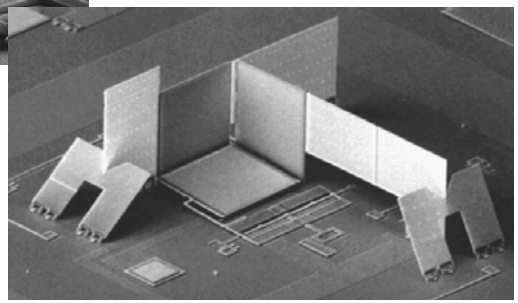
3D "Pop-up" MEMS

Pop-Up MEMS



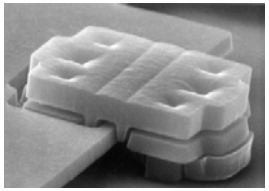
First MEMS hinge
[K. Pister, et al., 1992]

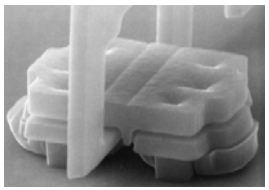
Corner Cube Reflector
[v. Hsu, 1999]



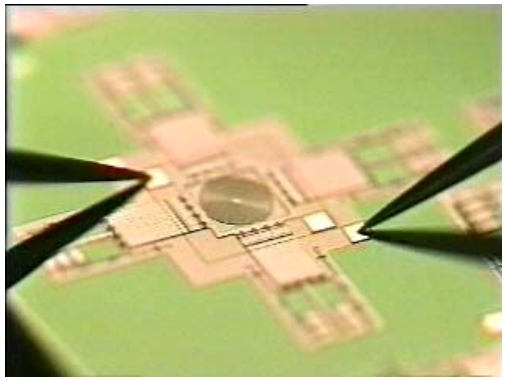
Pop-Up MEMS

- Pictured: hinged Campanile made in SUMMiT process, assembled using probes [Elliot Hui, et al.]



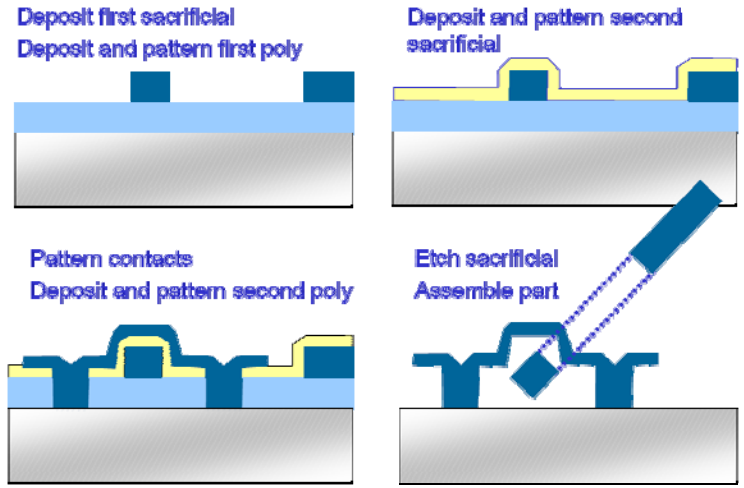


3D Direct-Assembled Tunable *L*



[Ming Wu, UCLA]

Hinge Process Flow

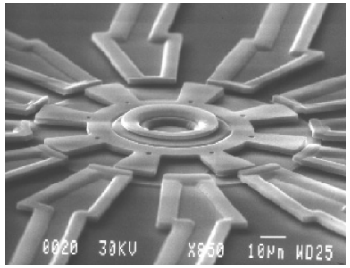


"Foundry" MEMS: The MUMPS Process

MUMPS: MultiUser MEMS ProcesS

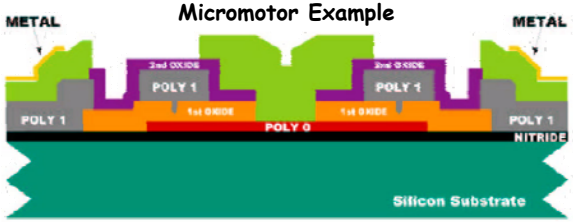
- Originally created by the Microelectronics Center of North Carolina (MCNC) → now owned by MEMSCAP in France
- Three-level polysilicon surface micromachining process for prototyping and "foundry" services
- Designed to service as many users as possible; basically an attempt to provide a universal MEMS process
- 8 photomasks
- $4,900 for 1 cm^2 dies

Micromotor fabricated via MUMPS



MUMPS: MultiUser MEMS ProcesS

Micromotor Example



Material Layer	Thickness (μm)	Lithography Level Name
Nitride	0.6	--
Poly 0	0.5	POLY0 (HOLE0)
First Oxide	2.0	DIMPLE ANCHOR1
Poly 1	2.0	POLY1 (HOLE1)
Second Oxide	0.75	POLY1_POLY2_VIA ANCHOR2
Poly 2	1.5	POLY2 (HOLE2)
Metal	0.5	METAL (HOLEM)

Masks in polyMUMPS

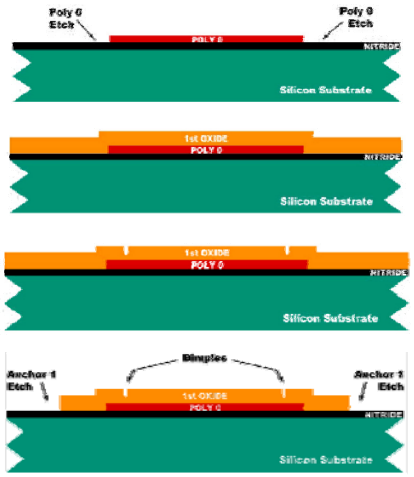
Minimum set of masks that must be used in MUMPS

Mnemonic level name	Field type	Purpose
POLY0	light	pattern ground plane
ANCHOR1	dark	open holes for Poly 1 to Nitride or Poly 0 connection
DIMPLE	dark	create dimples/bushings for Poly 1
POLY1	light	pattern Poly 1
POLY1_POLY2_VIA	dark	open holes for Poly 1 to Poly 2 connection
ANCHOR2	dark	open holes for Poly 2 to Nitride or Poly 0 connection
POLY2	light	pattern Poly 2
METAL	light	pattern Metal
HOLE0	dark	provide holes for POLY0
HOLE1	dark	provide release holes for POLY1
HOLE2	dark	provide release holes for POLY2
HOLEM	dark	provide release holes in METAL

Extra masks for more flexibility & ease of release

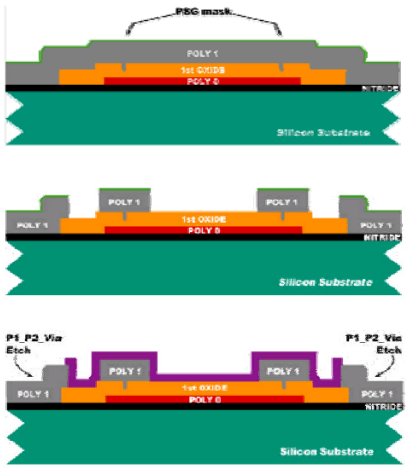
- Field type:
  - Light (or clear) field (cf): in layout, boxes represent features that will stay through fabrication
  - Dark field (df): in layout, boxes represent holes to be cut out

MUMPS Process Flow



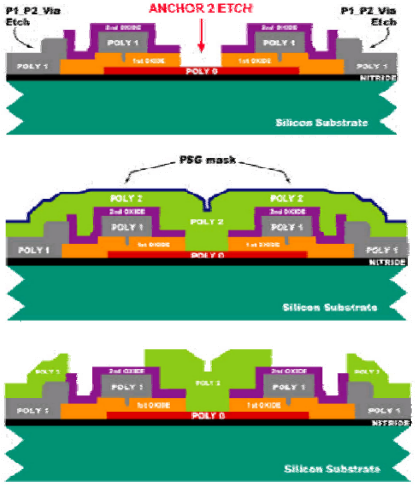
- Deposit PSG on the starting n-type (100) wafers
- Anneal to heavily dope the wafers
- Remove the PSG
- LPCVD 600 nm of low stress nitride
- LPCVD 500 nm of polysilicon
- Lithography using the POLY0(cf) mask and RIE etching to pattern the poly0 ground plane layer
- LPCVD 2 μm of PSG as the 1st sacrificial layer
- Lithography using the DIMPLE(df) mask (align to poly0)
- RIE 750 nm deep to form dimple vias
- Lithography using the ANCHOR1 (df) mask (align to poly0)
- RIE anchor vias down to the nitride surface

MUMPS Process Flow (cont.)



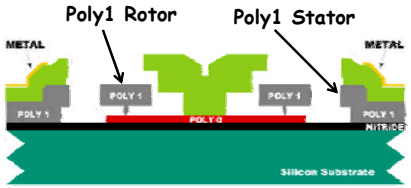
- LPCVD 2 μm undoped polysilicon
- LPCVD 200 nm of PSG
- Anneal for 1 hr. @ 1050°C
  - This both dopes the polysilicon and reduces its residual stress
- Lithography using the POLY1(cf) mask to define structures (align to anchor1)
- RIE the PSG to create a hard mask first, then …
- RIE the polysilicon
- LPCVD 750 nm of PSG
- Lithography using the P1_P2_VIA (df) mask to define contacts to the poly1 layer (align to poly1)

MUMPS Process Flow (cont.)



- Recoat with photoresist and do lithography using the ANCHOR2(df) mask to define openings where poly2 contacts nitride or poly0 (align to poly0)
- RIE the PSG at ANCHOR2 openings
- LPCVD 1.5 μm undoped polysilicon
- LPCVD 200 nm PSG as a hard mask and doping source
- Anneal for 1 hr @ 1050°C to dope the polysilicon and reduce residual stress
- Lithography using the POLY2(cf) mask (align to anchor2)
- RIE PSG hard mask
- RIE poly2 film
- Remove PR and hard mask

MUMPS Process Flow (cont.)



Final Structure: Micromotor

- Lithography using the METAL (df) mask (align to poly2)
- Evaporate titanium (Ti) (as an adhesion layer for gold)
- Evaporate gold (Au)
- Liftoff to remove PR and define metal interconnects
- Coat wafers with protective PR
- Dice wafers
- Ship to customer

- Customer releases structures by dipping and agitating dies in a 48.8 wt. % HF solution or via vapor phase HF
- Anti-stiction dry, if needed

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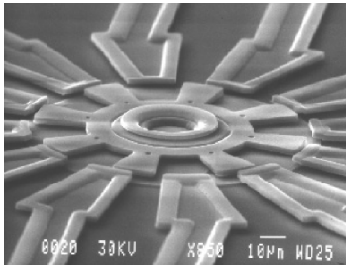
Micromotor fabricated via MUMPS



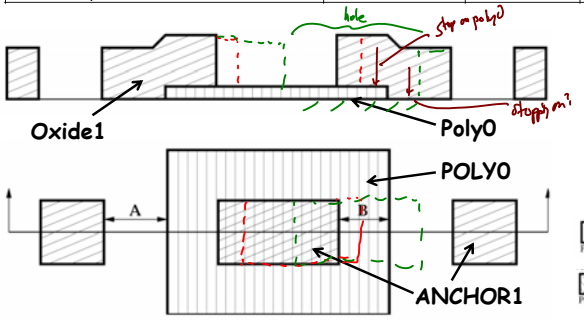
polyMUMPS Minimum Feature Constraints

- Minimum feature size
  - Determined by MUMPS' photolithographic resolution and alignment precision
  - Violations result in missing (unanchored), under/oversized, or fused features
  - Use minimum feature only when absolutely necessary

	Nominal [μm]	Min Feature [μm]	Min Spacing [μm]
POLY0, POLY1, POLY2	3	2	2
POLY1_POLY2_VIA	3	2	2
ANCHOR1, ANCHOR2	3	3	2
DIMPLE	3	2	3
METAL	3	3	3
HOLE1, HOLE2	4	3	3
HOLEM	5	4	4

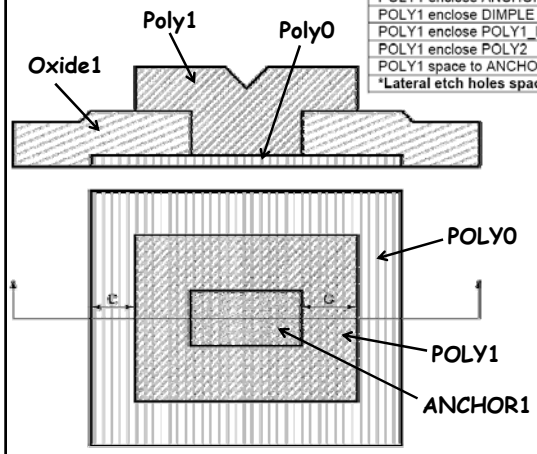
MUMPS Design Rules (cont.)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0



MUMPS Design Rules (cont.)

Rule		Min. Value (μm)
POLY1 enclose ANCHOR1	G	4.0
POLY1 enclose DIMPLE	N	4.0
POLY1 enclose POLY1_POLY2_VIA	H	4.0
POLY1 enclose POLY2	O	4.0
POLY1 space to ANCHOR2	K	3.0
*Lateral etch holes space in POLY1	R	≤30 (max. value)



MUMPS Design Rules (cont.)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY0 space to ANCHOR1	A	2.5	4.0
POLY0 enclose ANCHOR1	B	2.5	4.0
POLY0 enclose POLY1	C	2.6	4.0
POLY0 enclose POLY2	D	2.7	5.0
POLY0 enclose ANCHOR2	E	2.8	5.0
POLY0 space to ANCHOR2	F	2.8	5.0

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY1 enclose ANCHOR1	G	2.6	4.0
POLY1 enclose DIMPLE	N	2.13	4.0
POLY1 enclose POLY1_POLY2_VIA	H	2.9, 2.11	4.0
POLY1 enclose POLY2	O	2.14	4.0
POLY1 space to ANCHOR2	K	2.11	3.0
*Lateral etch holes space in POLY1	R	2.15	≤30 (max. value)

Rule	Rule Letter	Figure #	Min. Value (μm)
POLY2 enclose ANCHOR2	J	2.7,2.10	5.0
POLY2 enclose POLY1_POLY2_VIA	L	2.9	4.0
POLY2 cut-in POLY1	P	2.14	5.0
POLY2 cut-out POLY1	Q	2.14	4.0
POLY2 enclose METAL	M	2.12	3.0
POLY2 space to POLY1	I	2.10	3.0
HOLE2 enclose HOLE1	T	2.16	2.0
HOLEM enclose HOLE2	U	2.16	2.0
*Lateral etch holes space in POLY2	S	2.15	≤30 (max. value)

MUMPS Design Rules (cont.)

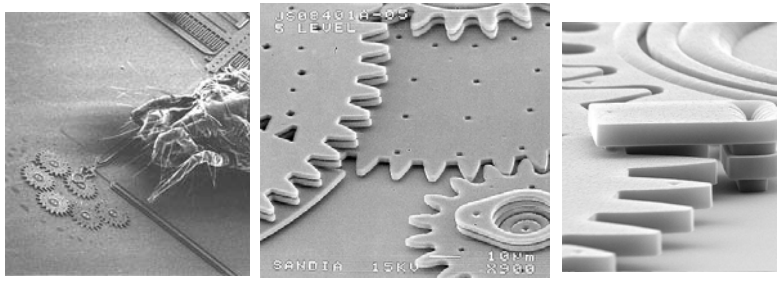
Level 1	Level 2	Min. Feature	Min. Spacing	Enclose	Spacing	Cut- In	Cut- Out
POLY0	-	2	2				
	ANCHOR1			4/B/2.5	4/A/2.5		
	POLY1			4/C/2.6			
	ANCHOR2			5/E/2.8	5/F/2.8		
	POLY2			5/D/2.7			
POLY1	-	2	2 / 2.5[2]				
	POLY0						
	ANCHOR1			4/G/2.6			
	ANCHOR2				3/K/2.11		
	POLY2			4/0/2.14			
	DIMPLE			4/N/2.13			
	POLY1_POLY2_VIA			4/H/2.9			
POLY2	-	2	2 / 2.5[2]				
	POLY0						
	POLY1				3/I/2.10	5/P/2.14	4/Q/2.14
	VIA			4/L/2.9			
	ANCHOR2			5/J/2.7			
	METAL			3/M/2.12			
HOLEM	HOLE2			2/U/2.16			
HOLE2	HOLE1			2/T/2.16			

TABLE 2.7. PolyMUMPs design rule reference sheet. Table shows minimum dimensions (μm), rule name, and figure number, respectively.

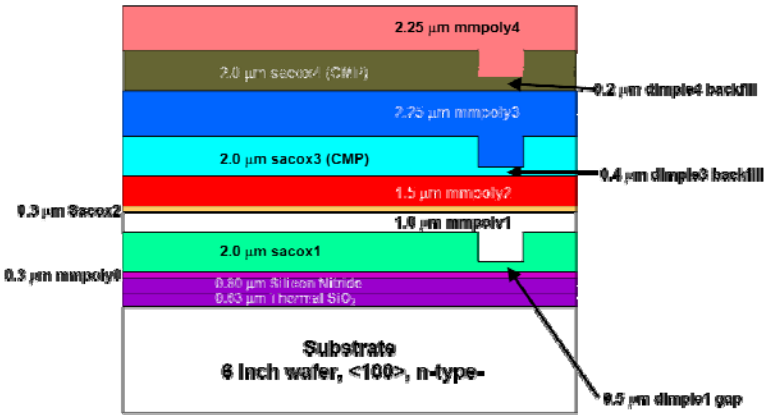
The Sandia SUMMIT Process

Sandia's SUMMiT V

- SUMMiT V: "Sandia Ultra-planar Multi-level MEMS Technology 5" fabrication process
  - Five-layer polysilicon surface micromachining process
  - One electrical interconnect layer & 4 mechanical layers
  - Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized
  - 14 masks



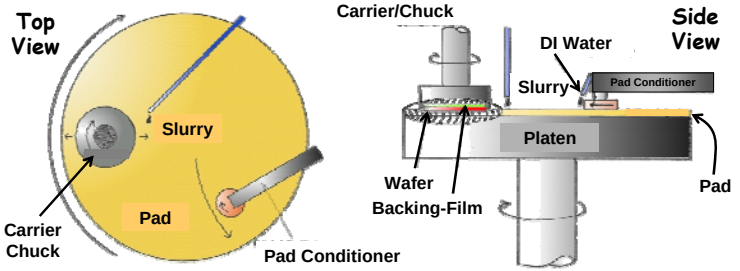
SUMMiT V Layer Stack



- Uses chemical mechanical polishing (CMP) to maintain planarity as more structural layers are realized

Chemical Mechanical Polishing (CMP)

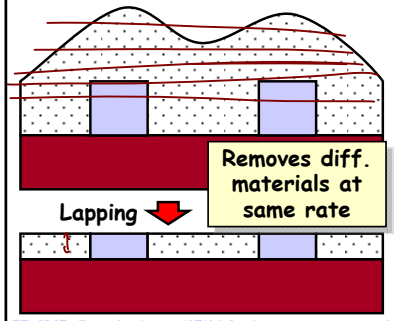
- Used to planarize the top surface of a semiconductor wafer or other substrate
- Uses an abrasive and corrosive chemical slurry (i.e., a colloid) in conjunction with a polishing pad
  - Wafer and pad are pressed together
  - Polishing head is rotated with different axes of rotation (i.e., non-concentric) to randomize the polishing



CMP: Not the Same as Lapping

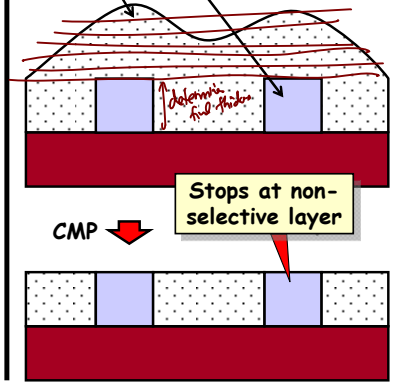
Lapping

- Lapping is merely the removal of material to flatten a surface without selectivity
- Everything is removed at approximately the same rate

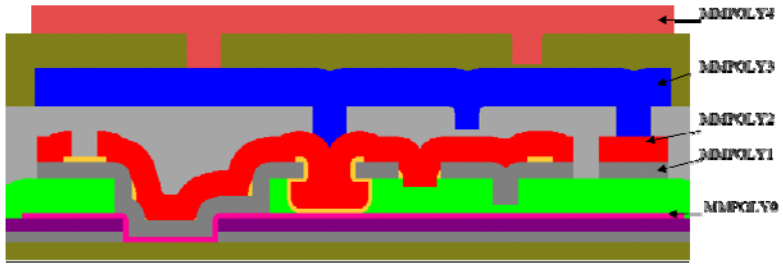


Chemical Mechanical Polishing

- CMP is selective to certain films, and not selective to others



Actual SUMMiT Cross-Section



- No CMP until after the first three polySi layers
- 1 μm mmpoly1 and 1.5 μm mmpoly2 can be combined to form a 2.5 μm polysilicon film
- Refer to the SUMMiT V manual (one of your handouts) for more detailed information on masks and layout instructions

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