PROBLEM SET #2

Issued: Tuesday, Sep. 11, 2012

Due (at 7 p.m.): Tuesday Sept. 25, 2012, in the EE C245 HW box near 125 Cory.

1. Most on-chip high frequency devices, be they purely electrical or electromechanical, prefer a thick layer of underlying insulator to reduce parasitic capacitance. One approach to making such a thick layer comprises etching very deep trenches into the silicon wafer, and then oxidizing the wafer in a thermal oxidation furnace, as shown in Figure PS2.1-1.

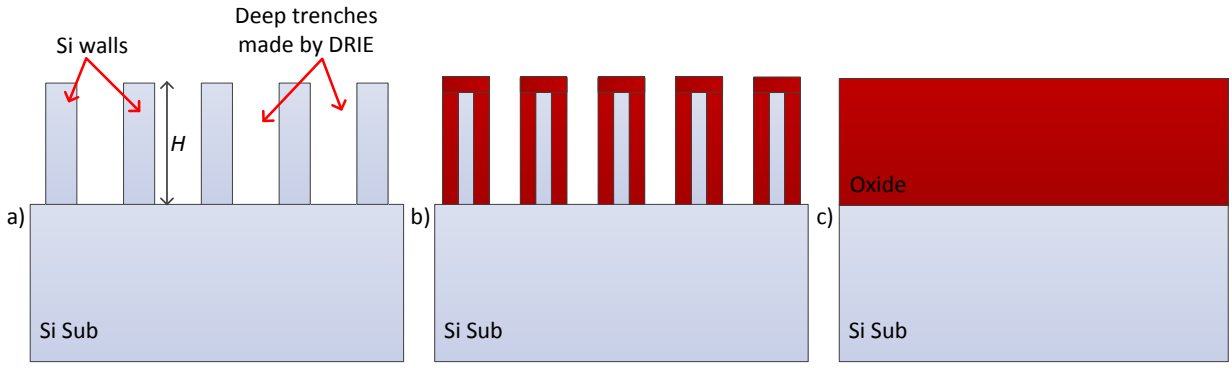

Figure PS2.1-1

(a) For best isolation, the oxidation process should consume the silicon walls entirely, with no empty space left between the walls. If the layout in Figure PS2.1-2 defines the pattern to be etched, where the dark regions indicate the silicon walls, find the needed d_1 if d_2 is 1μm and H is 5μm? If the trenches must be 20μm deep, what then is the required d_1?

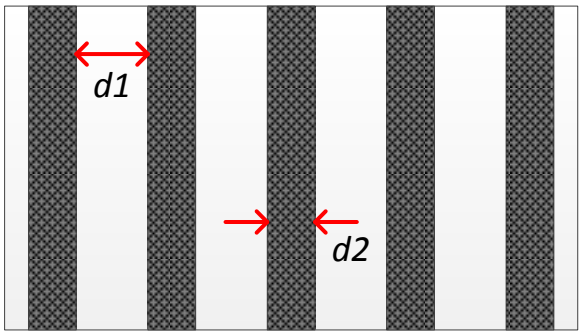

Figure PS2.1-2

(b) Derive an expression as a function of d_2, B and B/A for the time required to oxidize the silicon walls completely.

(c) If the trenches are 5μm deep, what is the entire thickness of the oxide layer when the oxidation process is complete? What will be the oxide thickness when trenches are 20μm deep? Neglect oxidation of the silicon surface at the bottom of trenches.

(d) Your colleague has proposed that if you use the layout in Figure PS2.1-3 for the etch mask, the oxidation time decreases. How do your answers to the previous parts change for this layout?

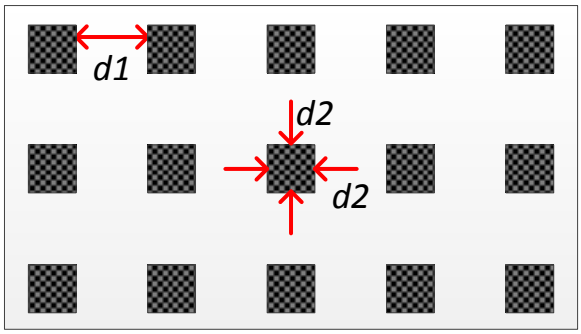

Figure PS2.1-3

2. Suppose you want to make a resistor by diffusing boron atoms into an n-type silicon wafer with a constant n-type doping concentration of $N_{sub} = 1 \times 10^{15} cm^{-3}$. To do so, you first place the wafer into a pre-deposition furnace alongside solid-source boron wafers for 30min at 900°C. You then drive in the dopants (with no boron source) for 60min at 1050°C.

(a) Derive an expression for the distribution of boron atoms after the pre-deposition step and plot it as a function of depth. What is the total number of dopant atoms per unit area?

(b) Derive an expression for the distribution of boron atoms after the drive-in step and plot it as a function of depth. As discussed in lecture, you can assume the pre-deposition step equates to a thin layer of highly doped silicon at the surface of the wafer and then use the total number of dopant atoms per unit area to find the Gaussian function.

(c) The depth at which the concentration of diffused dopant atoms is the same as the background concentration is defined to be the junction depth. What is the junction depth at the end of the process?

(d) Find the sheet resistance of the doped layer. Remember that the dopant concentration is a function of depth, so use the distribution function derived in (b) to find the exact sheet resistance. Assume the pn-junction depletion width is negligible in comparison to junction depth.

(e) What is the resistance of a resistor with $L = 100\mu m$ and $W = 10\mu m$ fabricated in this process?

(f) What constant doping level gives you the same sheet resistance with the same junction depth you derived in (c)?

(g) Suppose you further oxidize the wafer in a dry oxidation furnace for 2 hours at 900°C. What happens to the boron atoms at the Si-SiO_2 interface? Find the new value of the junction depth. Does the resistance you calculated in (i) change? [Hint: See pg.52 of Jaegar.]

3. This problem explores the anisotropic wet etching of silicon to create suspended structures that can be used for example in gas flow meter sensors. You are given a (100) silicon wafer with the hard mask layer deposited on it (c.f., Figure PS2.3-1) patterned with the layout given in Figure PS2.3-2. The etchant you use is 20% KOH solution at 80°C, which has an etch rate of 1.4μm/min in (100) direction.

(a) Draw the cross-section of the structure along A-A′ and B-B′ after 2 and 8 min. Assume the pattern is perfectly aligned with the wafer major flat, i.e., the (110) direction.

(b) What will happen if the wafer remains in the etchant for a very long time?

(c) Redraw the cross-sections and give all dimensions when the mask layout is 10° misaligned to the (110) plane.

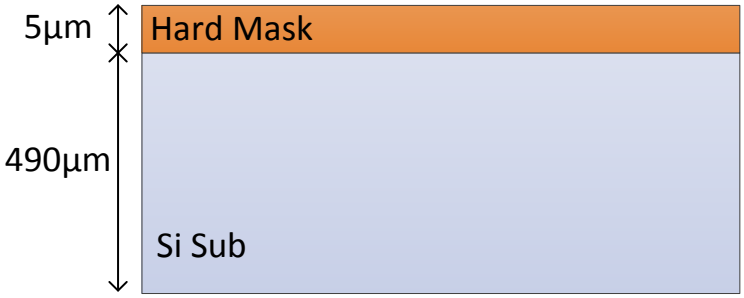

Figure PS2.3-1

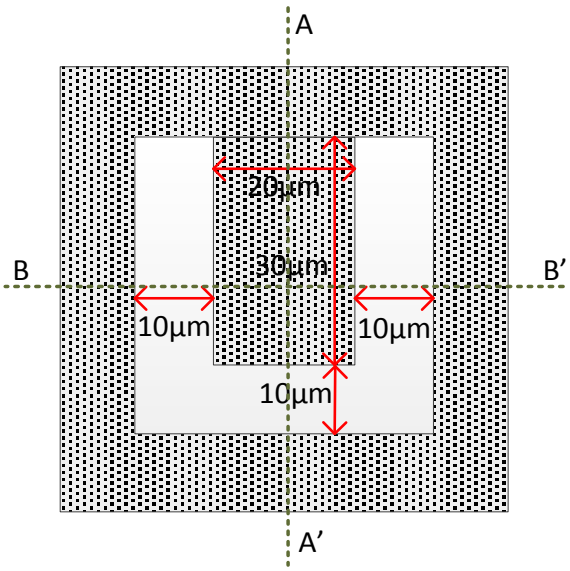

Figure PS2.3-2

4. This problem explores effect of finite lateral etch rate on the final etch profile. Assume you want to etch material A in the samples shown in Figure PS2.4-1 with etchant X. This etchant etches material A with $ER_{A,H}$ and $ER_{A,V}$ in the horizontal and vertical directions, respectively. The etchant is not completely selective and etches material B with vertical and lateral etch

rates of $ER_{B,V}$ and $ER_{B,H}$, respectively. Draw the cross-section of each structure when material A is completely gone. Clearly state the assumptions you make to get to final solution.

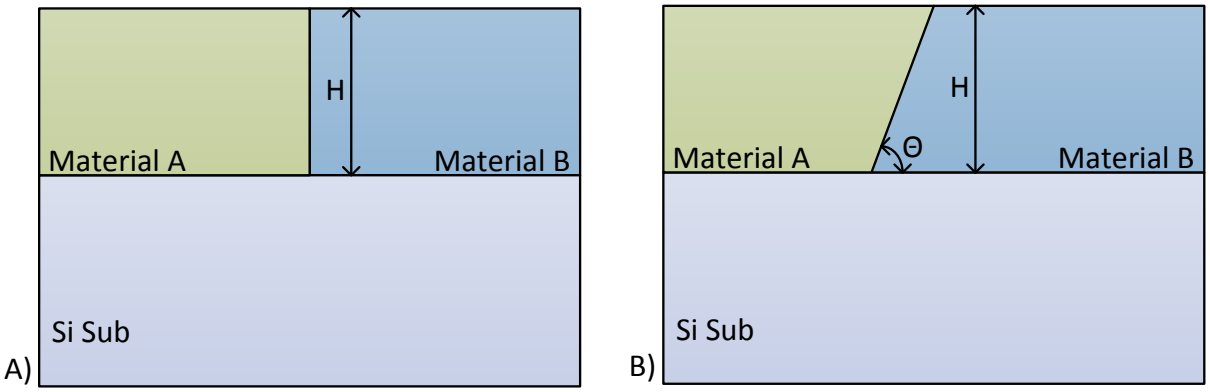

Figure PS2.4-1

5. You are given a wafer with the cross-section shown in Figure PS2.5-1 and intend to release etch the structure, i.e., to leave only the polysilicon structure atop the blanket nitride/oxide layer. To perform the release, you first dry etch the polysilicon in an RIE system with etch rate and selectivity given in Table 2.5-1. You then wet etch the oxide layer in a completely isotropic etchant with characteristics given in Table 2.5-2.

Since the deposition steps are not completely uniform, the layer thickness may not be the same over the entire wafer. So when you are etching a layer, you need to etch a bit longer than what you calculate from knowledge of thickness and etch rate to make sure all structures are etched completely. It is common practice to etch for 20% longer than the calculated time (i.e., do a 20% overetch). Include this overetch in your calculations for this problem.

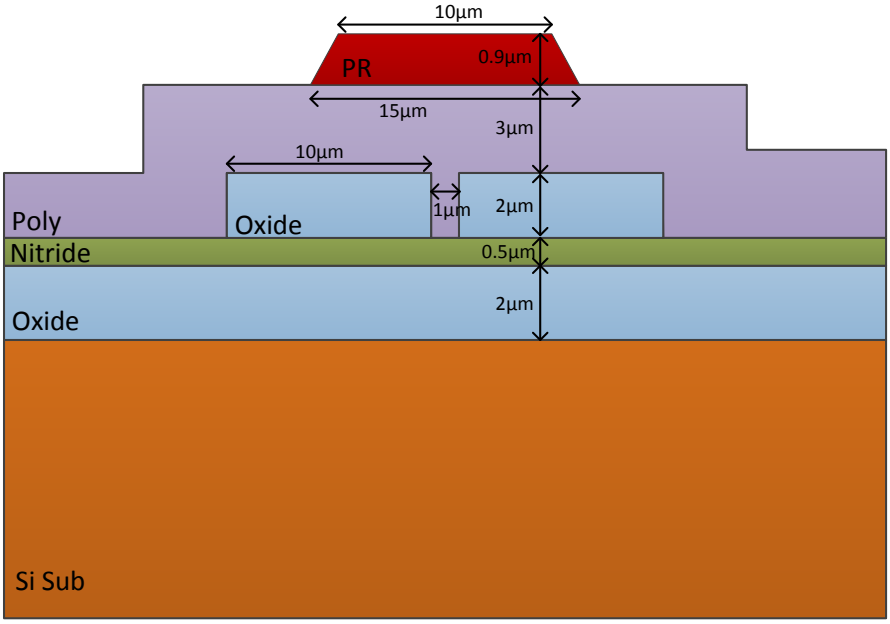

Figure PS2.5-1

Table 2.5-1

Polysilicon etch rate	0.5μm/min
Selectivity over Oxide	5:1
Selectivity over Nitride	10:1
Selectivity over Photoresist	2:1

Table 2.5-2

Oxide etch rate	0.2μm/min
Selectivity over Poly	10:1
Selectivity over Nitride	5:1
Selectivity over Photoresist	5:1

(a) How long should you etch the polysilicon layer? Draw the wafer cross-section immediately after the polysilicon etch step. You can assume the RIE etch is completely anisotropic.

(b) How long does it take to completely release the structure? Draw the wafer cross-section immediately after the release step. Assume the wet etch is completely isotropic.

(c) As you have seen, there are two major problems with this process. Explain what caused these problems and how one might fix them. Draw the final cross-section attained by your proposed fixes.