Effects of Defect Propagation/Growth on In-Line Defect-Based Yield Prediction

Wataru Shindo, Student Member, IEEE, Raman K. Nurani, and Andrzej J. Strojwas, Fellow, IEEE

Abstract—This paper presents the importance of understanding defect propagation/growth and its impact on in-line yield prediction. In order to improve the prediction accuracy, impact of defect propagation and growth phenomena needs to be modeled and incorporated into yield prediction system. We developed a new yield prediction model by taking into account defect carryover. The empirical results of interlayer and intralayer defect propagation analysis using actual fabline data are presented.

Index Terms—Critical area, defect propagation, defect growth, in-line inspection, yield model, yield prediction.

I. INTRODUCTION

REDICTING the yield value of the wafers before they reach the end-of-line is quite essential for successful yield management in semiconductor manufacturing. The advantages of early in-line yield prediction include detection and elimination of yield-limiting process excursions and adjustment of wafer starts to meet the demand schedule. In-line defect inspections are the key enablers in the functional yield prediction. We have previously presented a multiple-layer critical area based yield prediction system using in-line defect measurements [1]. The prediction accuracy of our model has been already quite high. However, it is required to improve the accuracy much more since even slight error in the prediction may result in unacceptable revenue loss in subquarter micron era and beyond. From the previous work, we found that defect propagation and growth can be a major source of yield prediction inaccuracy. This is because even a small defect that does not kill a die at a current layer may grow in size and possibly kill the die at subsequent layers. Such phenomena have not been considered in conventional yield prediction models at all. The purpose of this paper is to extend the yield model used in the multilayer in-line yield prediction system to include the defect propagation. We also present and discuss the results of intralayer and interlayer defect propagation analysis using real fabline data.

Manuscript received December 4, 1997; revised March 5, 1998.

W. Shindo is with the Department of Electronic Engineering, Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan (e-mail: shindo@sse.ecei.tohoku.ac.jp).

R. K. Nurani is with KLA-Tencor Corporation, Milpitas, CA 95035 USA (e-mail: raman.nurani@kla-tencor.com).

A. J. Strojwas is with the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA 15213-3890 USA (e-mail: ajs@gauss.ece.cmu.edu).

Publisher Item Identifier S 0894-6507(98)08364-X.

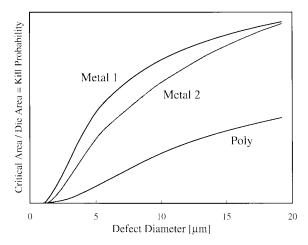


Fig. 1. Critical areas divided by the die area (kill probability) of three critical layers, i.e., Poly, Metal 1, and Metal 2 of a logic product.

II. IN-LINE YIELD PREDICTION METHODOLOGY

Critical area is a way of qualifying layout sensitivity to spot defects that cause pattern deformations. The critical area is defined as the area of a die on which if the center of a defect of a given size lands it will cause a pattern defect (e.g., short or open) [2]. Therefore, there is a unique critical area for a different defect size for each layer in the die. Critical area divided by the die area gives the probability that a defect of a given size cause a failure, so called kill probability or kill ratio. Fig. 1 shows critical area functions divided by the die area for three layers (Poly, Metal 1, and Metal 2) of a logic product. The critical area increases monotonically with the defect size, and different layers have different critical area functions.

Assuming the defects are randomly distributed across a wafer, a generalized Poisson-based functional yield model can be used as a yield predictor [2]:

$$Y = \prod_{i=1}^{N} \exp\left[-D_i \int_x A_i^{crit}(x) \cdot f_i(x) dx\right]$$
 (1)

where

i critical layer;

N number of critical layers;

x defect radius,
D defect density

defect density,

critical area and defect size probability density functions of defect radius, respectively.

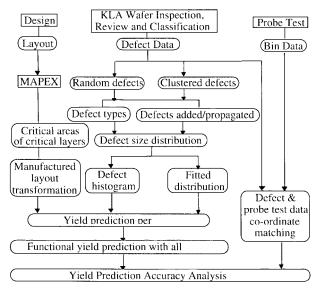


Fig. 2. Critical area-based multilayer in-line yield prediction system.

A flow chart of the multiple-layer in-line yield prediction system based on the critical area is shown in Fig. 2. Critical areas of all the critical layers are extracted from the design layout format using software called MAPEX [3]. Then the critical areas obtained from the drawn layouts are transformed to truly represent the manufactured dimensions because the drawn layouts are significantly different from the manufactured layouts due to design shrinks and shifts in critical dimensions [1]. The defect data obtained from KLA 213X inspection stations, which includes defect coordinates and sizes, is post-processed as follows.

- Random defects (randomly distributed defects) and clusters (spatially clustered defects) are separated using the de-clustering function of the KLA 255X data analysis station. Since clusters account for relatively small yield losses (especially for logic products), we focus only on the random defects for the purpose of this study (It is easy to extend this model to include defect clusters.).
- 2) Defect source analysis (DSA) is performed to determine which defect originated at a current layer and which got transferred from the previous layers. DSA module in KLA 255X enabled us to distinguish adder defects (that correspond to the newly added defects at the current layer) and common defects (that correspond to the defects propagated from prior layers) [1]. This determination is based on the defect coordinates. It should be noted that defect inspection equipment may report the same defect more than once at different layers if the defect is seen through transparent layers, or more importantly, the defect can actually propagate to higher layers and grow in size due to the "decoration" effect [4].
- 3) Then, defect density and defect size distribution of either only adder defects or adder+common defects are obtained.

By combining defect density and size distribution with the critical area function of multiple layers, we are now able to

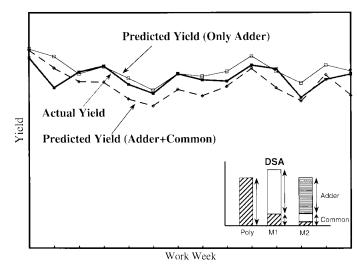


Fig. 3. Comparison of actual yield and predicted yield using only adder and adder+common defects.

predict yield impact of multiple layers using (1). In terms of defect density and size distribution, however, it is not certain whether we should use adder+common defects or only adder defects for better prediction accuracy. Fig. 3 presents the comparison between the predicted yield and the actual yield for four-month production at AMD-Austin fabline. The overall predicted yield is the product of the predicted yield of Poly, Metal 1, and Metal 2. (Contact holes are included in Poly-layer critical area calculation since a defect at the Poly layer can cause a short not only between Poly lines but also between a Poly line and a contact hole.) Yield prediction is based on either adder+common defects or adder defects only. It is apparent from this figure that the critical area methodology is successfully tracking the actual yield on a weekly basis. However, the yield prediction based on adder+common defects underestimates the actual yield. This is due to the fact that yield impacts of common defects are counted more than once independently at multiple layers although the common defects cannot kill a die twice. On the other hand, the predicted yield using only adder defects agrees very well with the actual yield for most weeks. The accuracy is well within 3% on the average. However, the predicted yield using only adder defects is slightly higher than the actual yield in most weeks. This is because defect propagation and growth phenomena are not considered at all in this case despite the fact that a harmless defect at a layer potentially causes a failure at subsequent layers. Therefore, the most accurate prediction is between these two methods, i.e., "adder+common" and "adder only." The yield model given by (1) assumes that the yield impact of each layer is independent, which is not true if defect carryover phenomenon is significant. This result clearly indicates that defect carryover has to properly handled and incorporated in the yield model in order to improve prediction accuracy.

III. YIELD MODEL INCORPORATING DFECT PROPAGATION

We have developed a yield model that takes into account the defect carryover effects. To simplify the problem, only

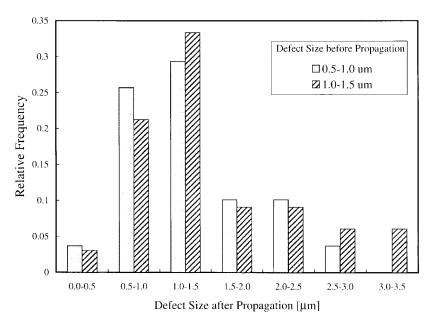


Fig. 4. The size distributions of propagated defects whose original sizes at the previous layer are $0.5-1.0~\mu m$ and $1.0-1.5~\mu m$.

two critical layers (denoted as layers 1 and 2) are considered. However, the model can be easily extended to more than three layers.

A defect generated at layer 1 can kill a die not only at layer 1, but also at layer 2 if the defects propagate to the subsequent layer. Let x_1 and x_2 denote the size of a defect at layers 1 and 2, respectively. The probability that a defect generated at layer 1 kills a die at any layer, p_1 , is given by the sum of the probability that a defect kills a die at layer 1, p_{11} , and the probability that the defect does not kill the die at layer 1 but kills the die at layer 2, p_{12} :

$$\begin{aligned} p_{11} &= P\{Kill @ layer1\} \\ &= \int_{x_1} f(x_1) K_1(x_1) \, dx_1 \\ p_{12} &= P\{NotKill @ Layer1 \& Kill @ layer2\} \\ &= \int_{x_1} f(x_1) \{1 - K_1(x_1)\} \\ &\cdot \left\{ \int_{x_2} f(x_2|x_1) K_2(x_2) \, dx_2 \right\} dx_1, \end{aligned}$$

where

 $f(x_1)$ probability density function (PDF) of the defect size at layer 1;

 $f(x_2|x_1)$ PDF of the defect size at layer 2 conditioned on the defect size at layer 1 (x_2 is zero if the defect does not propagate);

 $K_i(x_i)$ kill probability function of defect size x_i at layer i.

Hence, p_1 is given by

$$p_1 = p_{11} + p_{12}$$

$$= \int_{x_1} f(x_1) \left[K_1(x_1) + \{1 - K_1(x_1)\} \int_{x_2} \cdot f(x_2 | x_1) K_2(x_2) dx_2 \right] dx_1.$$

The kill ratio $K_i(x_i)$ is given by $A_i^{crit}(x_i)/A_d$, where $A_i^{crit}(x_i)$ is the critical area for the defect size x_i at layer i and A_d is the die area.

$$p_{1} = \int_{x_{1}} f(x_{1}) \left[\frac{A_{1}^{crit}(x_{1})}{A_{d}} + \left\{ 1 - \frac{A_{1}^{crit}(x_{1})}{A_{d}} \right\} \int_{x_{2}} \cdot f(x_{2}|x_{1}) \frac{A_{2}^{crit}(x_{2})}{A_{d}} dx_{2} \right] dx_{1}.$$
 (2)

Hence, by assuming defects are randomly distributed, the yield determined by the layer1-originated defects is as follows:

$$Y_{1} = \exp(-A_{d} \cdot D_{A1} \cdot p_{1})$$

$$= \exp\left[-D_{A1} \int_{x_{1}} f(x_{1}) A_{1}^{crit}(x_{1}) dx_{1}\right]$$

$$\cdot \exp\left[-D_{A1} \int_{x_{1}} f(x_{1}) \left\{1 - \frac{A_{1}^{crit}(x_{1})}{A_{d}}\right\}\right]$$

$$\cdot \left\{\int_{x_{2}} f(x_{2}|x_{1}) A_{2}^{crit}(x_{2}) dx_{2}\right\} dx_{1}$$
(3)

where D_{A1} is the adder defect density at layer 1. The first exponential term in the second equality of (3) is the same as the yield calculated by (1) using only adder defect. Therefore, this term indicates the yield loss caused by the layer-1 adders at layer 1. The second exponential term represents the yield loss caused by propagated common defects where the double-counting issue is eliminated. The conditional defect size distribution $f(x_1|x_2)$ is required in the new yield model. It can be obtained by generating the histogram of propagated defect size x_2 for given original defect size x_1 . Fig. 4 shows typical defect size distributions of propagated defects whose original sizes at the previous layer are 0.5-1.0 μ m and 1.0–1.5 μ m, respectively. When the defect propagation/growth characteristics vary from defect type to type, the conditional distribution $f(x_1|x_2)$ of each defect type may need to be calculated separately.

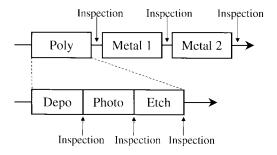
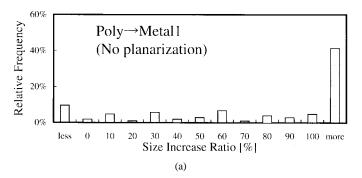


Fig. 5. Inter- and intralayer defect propagation analysis.



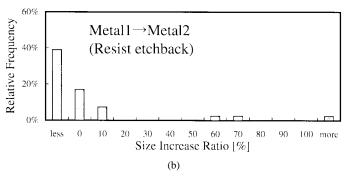


Fig. 6. Histograms of the defect size increase ratio. (a) Poly to Metal 1 and (b) Metal 1 to Metal 2.

IV. INTER- AND INTRALAYER DEFECT PROPAGATION

In order to compute the yield using (3), it is necessary to model the defect propagation/growth effects. Obviously interlayer defect carryover is quite important in dealing with multiple layer yield prediction. Intralayer analysis is also important in the following sense. 1) It provides better understanding of the mechanism of interlayer defect carryover and 2) as the complexity and number of process steps per layer increase, it is eventually required to monitor the yield losses even within one process module. Consequently intralayer inspections will play more important roles in yield prediction. Thus, we did extensive analyses on interlayer and intralayer defect propagation as illustrated in Fig. 5. Interlayer carryover was investigated by comparing the so-called final inspections of each layer, i.e., post Poly Etch inspection, post Metal 1 Etch inspection, and post Metal 2 Etch inspection, all of them after photoresist stripping. Intralayer analysis was done within the Poly module using post-Depo, post-Photo, and post-Etch and Clean inspections.

Fig. 6 shows the layer dependence of the interlayer defect growth (a) from Poly to Metal 1 and (b) from Metal 1 to Metal

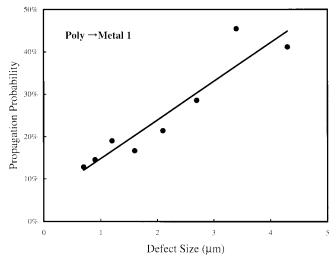


Fig. 7. Probability of defect propagation from Poly to Metal 1 as a function of the original defect size.

2. The horizontal axes indicate size increase ratio defined by the propagated defect size divided by the original defect size. 0% indicates that a defect does not change its size at all. 100% represents that a defect doubles its size. From Poly to Metal 1, over 40% of the propagated defect more than double their sizes. There was no planarization process between Poly to Metal 1 in this case, and thus the Poly defects can grow in size due to the decoration effect. On the other hand, most of the defects reduce the size from Metal 1 to Metal 2. This is because photoresist etchback was carried out between Metal 1 and 2 and the defects got planarized. It is demonstrated that defect growth strongly depends on planarization processes, such as resist etchback or chemical mechanical polishing (CMP). However we should note that even the planarized defects can cause functional or parametric failure especially if the top of the defect reaches the planarized surface.

Next we focus on the propagation form Poly to Metal 1, where no planarization process is performed. The probability of defect carryover from Poly to Metal 1 as a function of the original defect size is shown in Fig. 7. Average propagation probability is about 20%, but this probability strongly depends on the original size. As one can imagine, lager defects have higher chance of propagation. Since larger defects have high kill ratio and high propagation probability, it seems that larger defects are more important in yield impact analysis than smaller defects. However, yield impact of the larger defects after the propagation may not be so high because such larger defects might kill the dies already at the prior layer. On the other hand, kill probability and propagation probability of smaller defects may be low compared to larger defects. However, smaller defects are also important in yield prediction since the smaller defects are more frequent, and a small defect which does not cause any failure at current layer may kill the die at the following layer if the defect size growth is significant.

Fig. 8 shows interlayer defect propagation probabilities for several nonplanar defect types and planar defect types. It is clearly seen that defect type is also an essential factor

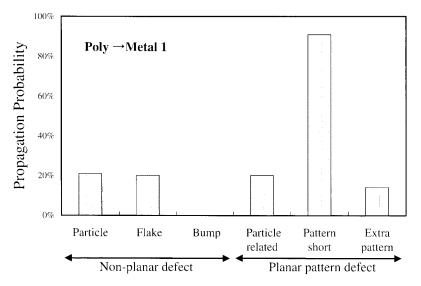
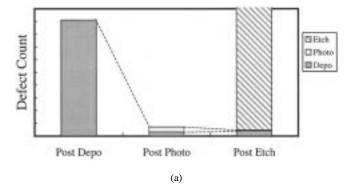


Fig. 8. Defect propagation probabilities from Poly to Metal 1 of nonplanar defects and Poly planar defects.

in the interlayer defect propagation. It should be noted that the propagation probabilities of Poly planar defects are not necessarily lower than that of nonplanar defects. Although yield impact prediction can be performed without classifying defects into various types (e.g., particles, planar defects, scratches), we can implement an option of predicting yield loss per defect type in our system. By using the defect density and defect size distribution per defect type, it is possible to predict yield impact of each defect type. This approach is essential especially when the defect carryover probability varies from defect type to type.

To study the intralayer propagation, defect source analysis (DSA) was carried out within the Poly module, which consists of 1) gate oxidation and polysilicon deposition (denoted as Depo), 2) photolithography for gate definition (denoted as Photo), and 3) dry etching and cleaning (denoted as Etch). Fig. 9 shows the results of intralayer carryover analysis of (a) random defects and (b) cluster defects. In this particular data set, carryover from Depo to Etch is more significant than from Photo. We assume the number of Photo-generated defects is relatively low because the environment for lithography process is strictly controlled while film deposition and etching process have structural defect sources, e.g., particle flakingoff from the chamber wall. (Note that the probability of Photo-to-Etch carryover is not necessarily lower than that of Depo-to-Etch.) Furthermore, propagation of cluster defects is more significant than for random defects. This is probably due to the interactions between the defects. Defects in a cluster can be considered as one huge defect since the distance between the defects is very close. However, it does not mean that clusters are more important than randoms in defect propagation analysis because random defects account for large portion of yield loss. Fig. 10 shows the sources of the defects detected at post-Etch inspection. For instance, ninety percent of type A defects are originated at Etch, a few percent are from Photo, and the rest are generated at Depo. Intralayer propagation also strongly depends on the defect type. Different defect types exhibit different profiles of defect source. (This indicates that



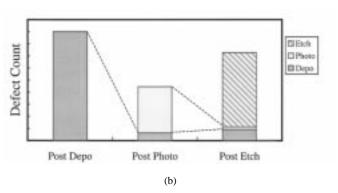


Fig. 9. Defect source analysis within Poly module. (a) Random defects and (b) Cluster defects.

understanding the defect propagation will not only help in reducing yield prediction error but also aid in identifying the problem source [5].) Thus the yield impact analysis should be performed based on the defect type as well as the defect size. The propagation probabilities required in our new yield model (3) can be derived from such experiments. However, it should be noted that defect propagation analysis based on both defect size and type may require a large sample size. If the sample size is not big enough in any case, simulations of defect propagation/growth [4] and the defect detection scheme (e.g., capture rate) [6] would be of great help in modeling the

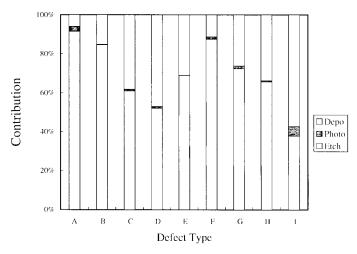


Fig. 10. Sources of the defects found at post Poly etch inspection.

propagation statistics and in making assumptions about the dominant propagation mechanisms.

V. CONCLUSION

In this paper, we discussed the role of defect propagation in yield prediction. It is found that yield prediction using adder+common defects underestimates the actual yield since the common defects are counted more than once, whereas yield prediction based on only adder defects overestimates the yield. Thus we proposed a new yield model by taking into account the propagation/growth phenomenon. Furthermore, we showed examples of inter and intralayer defect carryover obtained from real fabline.

ACKNOWLEDGMENT

The authors would like to thank M. McIntyre of AMD Austin, W. Tomlinson of IBM Burlington, D. Fletcher of KLA-Tencor, and Y. Mizokami of KLA-Tencor Japan for their various support of this research.

REFERENCES

- R. K. Nurani, A. J. Strojwas, W. P. Maly, C. Ouyang, W. Shindo, R. Akella, M. McIntyre, and J. Derrett, "In-line yield prediction methodologies using patterned wafer inspection information," *IEEE Trans. Semiconduct Manufact*, vol. 11, pp. 40–47. Feb. 1998.
- Semiconduct. Manufact., vol. 11, pp. 40–47, Feb. 1998.
 [2] W. Maly and J. Deszczka, "Yield estimation model for VLSI artwork evaluation," *Electron. Lett.*, vol. 19, pp. 226–227, Mar. 1983.
- [3] H. T. Heineken and W. Maly, "Manufacturing analysis environment—MAPEX," in *Proc. 1994 Custom Integrated Circuit Conf.*, 1994, pp. 309–312.
- [4] X. Li, A. J. Strojwas, M. Reddy, L. Milor, and Y. T. Lin, "Modeling of defect propagation/growth for early impact prediction in VLSI

- fabrication," in *Proc. Advanced Semiconductor Manufacturing Conf.*, 1997, pp. 263–268.
- [5] W. Shindo, E. H. Wang, R. Akella, and A. J. Strojwas, "Effective excursion detection and source isolation with defect inspection and classification," in *Proc. Advanced Semiconductor Manufacturing Conf.*, 1997, pp. 146–149.
- [6] A. L. Swecker, A. J. Strojwas, A. Levy, and B. Bell, "Evaluation of defect detection schemes for CMP process monitoring using rigorous 3-D EM simulations," in *Proc. Advanced Semiconductor Manufacturing* Conf., 1997, pp. 283–288.



Wataru Shindo (S'98) received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1993 and 1995, respectively. He studied low-temperature silicon epitaxy using low-energy ion bombardment process. Currently, he is pursuing the Ph.D. degree at the graduate school of Tohoku University.

From 1996 to 1997, he visited Stanford University, Stanford, CA, to work on yield management of semiconductor manufacturing.



Raman K. Nurani received the B.S. degree in mechanical engineering from the Indian Institute of Technology, Madras, in 1984, the M.B.A. degree from the Loyola Institute of Business Administration, Madras, in 1990, the M.S. degree in management of manufacturing and automation from Carnegie Mellon University, Pittsburgh, PA, in 1992, and the Ph.D. degree in management of manufacturing and automation from Carnegie Mellon University in 1995. He was a Visiting Student in the Department of Industrial Engineering and

Operations Research, University of California, Berkeley, during 1993–1994. At UC Berkeley, he was actively involved in the Sloan Focus study on Yield Management and the SRC funded project on Production Logistics Techniques Incorporating Yield Analysis.

He is currently a Senior Research Scientist at KLA-Tencor Corporation, Milpitas, CA. He has been interacting with many leading semiconductor companies such as AMD, TI, Digital, and HP to develop, validate, and implement his research work. His work has been instrumental in setting up the research program at KLA Instruments Corporation along with several universities and fab partners. His current research focuses on the development of models and methodologies in the area of yield management and automated wafer inspection. His other research interests include production logistics and systems design, production planning under yield and demand uncertainty, and process control in manufacturing.

Dr. Nurani received the Honorable Mention in the 1995 George B. Dantzig Award from INFORMS (Institute for Operations Research (OR) and Management Science (MS)) for the best Ph.D. dissertation that is innovative and relevant to the practice of OR and MS.

Andrzej J. Strojwas (F'90), for a photograph and biography, see this issue, p. 544.