Process Integration of Single-Wafer Technology in a 300-mm Fab, Realizing Drastic Cycle Time Reduction With High Yield and Excellent Reliability

Shuji Ikeda, *Senior Member, IEEE*, Kazunori Nemoto, *Member, IEEE*, Michimasa Funabashi, Toshiyuki Uchino, Hirohiko Yamamoto, Noriyuki Yabuoshi, Yasushi Sasaki, Kazuhiro Komori, Norio Suzuki, Shinji Nishihara, Shunji Sasabe, and Atsuyoshi Koike, *Member, IEEE*

Invited Paper

***Abstract*—In this paper, we discuss a new technology implemented with all, single-wafer processing for a 300-mm fab. Newly developed equipment and chemicals reduce the process time and provide cost savings. The combination of fully automated systems and single-wafer processing significantly reduces queuing time. The process has been re-integrated to eliminate long time processes and make it suitable for single-wafer technologies. As a result, a very aggressive cycle time (0.25 days/layer) with high yield, in double-polysilicon, sextuple-metal, 0.18-μm LOGIC process has been demonstrated. High-performance devices with excellent reliability are also obtained. A new methodology for detecting parametric errors effectively in the early stages of production is implemented for quick yield ramp up.**

***Index Terms*—Cycle time reduction, failure analysis, manufacturing automation, single-wafer process, yield optimization.**

I. Introduction

SCALING is one of the main streams to achieve higher performance/higher density. Yield improvement is the key to reducing costs. To keep up with the strong requirements for cost reduction, the semiconductor industry is in the process of increasing wafer size from 200 to 300 mm. However, this transition is complicated because the process flow in semiconductor manufacturing continues to increase and become more sophisticated. The increase in the number of process steps and number of lots in work-in-process (WIP) increase cycle time and raise inventory asset costs. In order to avoid inventory waste due to changing market requirements (such as customer's orders/design changes), to enable the fast ramp up of new lines/new products, or to quickly recover from unexpected problems, quick turn around time is essential in the integrated circuit (IC) industry today [1]–[4]. We proposed a new scheme integrating an all single-wafer process (SWP) in a 300-mm fab to achieve short cycle time manufacturing [5]. In the early stages of production, the main yield killer is systematic defects caused by parametric problems. Engineering Data Analysis (EDA) supported by commercial yield analysis systems is widely used for detecting these kinds of defects. However, the smaller number of data points makes early detection of parametric errors difficult. An advanced EDA is proposed to improve the yield in a short time during the early stages of production. In this paper, we describe new technologies integrated with SWP to achieve drastic cycle time reduction with high performance devices having excellent reliability.

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The authors are with the Trecenti-Technologies, Inc., Hitachinaka, Ibaraki, 312-0034, Japan.

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TABLE I
COMPARISON OF THE CONVENTIONAL BATCH PROCESS AND SWP IN THIS WORK

Module	Step	Conventional process	This work
Diffusion	STI SiN deposition	Furnace batch	RT single wafer
	STI oxide densification		
	Oxidation, gate and others		
	Nitridation for gate oxide		
	Poly gate		
	Spacer SiN, Oxide		
Wet	SiN stripe	wet station batch	single wafer dry etch
	Photo Resist strip	wet station batch	single wafer
	pre-clean		
	solvent clean		
Implant	High energy well imp	Batch	Batch-chain imp.
	Medium current imp	single wafer	single wafer
Photo	Photo scanner/tracker	single wafer	single wafer
Etch	Etcher/ PR ash	single wafer	single wafer
Thin film	CVD/ PVD metal dep.	single wafer	single wafer
	PE/HDP CVD oxide film		
	CMP		

II. Single-Wafer Processing

The comparison of conventional process and SWP in this work is shown in Table I. All steps have been changed to SWP including wet clean, CVD, and anneal/oxidation—major cycle time bottlenecks in conventional batch lines. Cycle time killers in batch processing are process time and queuing time. One of the advantages of SWP is that it does not require queuing time to facilitate batch processing. Thus, process time has a greater impact on cycle time than on the batch process [6], [7]. The key to reduced process time is process optimization and development of new equipment capabilities. As a result of these newly devel-

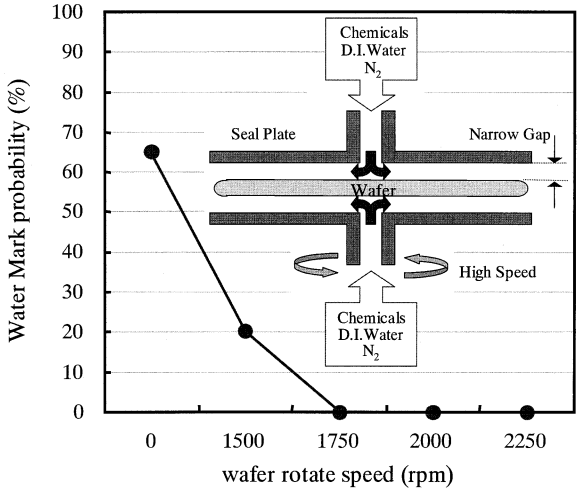


Fig. 1. Watermark probability dependence on wafer rotation speed and chamber design of newly developed single-wafer cleaning system.

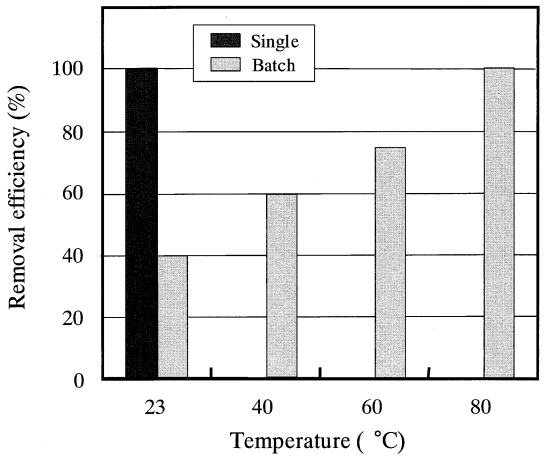


Fig. 2. Particle removal efficiency dependence on the cleaning temperature compared with batch and single wet clean processes.

oped equipment and processes, SWPs have better productivity and process capability than equivalent batch processes.

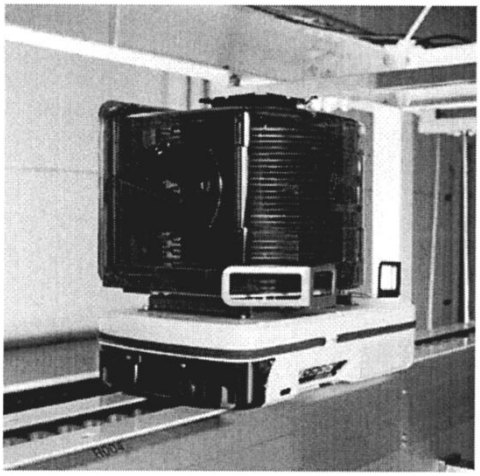
One of the examples we developed for this concept is an innovative single-wafer wet cleaning system that is used to replace the conventional batch cleaning system. Chamber structure is shown in Fig. 1. Newly developed cleaning chemicals remove particles and contamination effectively even at room temperature and shorten process time [8]. It is well known that higher temperature gives higher efficiency of particle reduction in cleaning because of higher etching ratios, but the required preheat time results in longer process time. Room temperature operation is essential because maintaining cleaning solutions at high temperature on the wafer is very difficult for SWP without wafer preheat prior to cleaning. Inorganic materials are added into conventional RCA solutions to reduce activation energy and increase etching rates at room temperature and to realize shorter cleaning time as shown in Fig. 2. Another key point, controlling Z potential by pH control [9], is essential to eliminate re-attachment of particles. Metal contamination is effectively removed by chemical redox potential control [10]. The new system achieves a 100% cleaning efficiency within 15 s/wafer at room temperature compared to the conventional RCA batch cleaning requiring 10 min/cassette in 80 °C to achieve the same efficiency. Since nitrogen flows in the narrow gap between the wafer and seal plate, and the wafer rotates at high speed during the drying sequence, seal-plate design is the key to eliminating watermarks. Moreover, we found that the number of watermarks strongly depends on the rotation speed during the dry process. A rotation speed of over 1750 rpm during the dry spin step eliminates watermarks effectively, as shown in Fig. 1. As a result, the new cleaning system, with single-wafer treatment at room temperature, makes easier to remove particles and contamination than batch processes at 80 °C. Because no preheat time is required, we are able to achieve a suitable process in one-tenth of the time used for conventional batch RCA cleaning at 80 °C. This accomplishment helps us achieve both cycle time reduction and chemical and waste disposal savings.

Throughout our 300-mm process development work, we were aware that a reduction in the process time sometimes results in a loss of film uniformity in CVD processes. So, one of our priorities was to achieve good film uniformity simultaneously with shorter process times. One of the most sensitive CVD processes to device performance is spacer film deposition. Thickness variation causes spacer width differences that affect both device performance and reliability. We found that the thickness variation of RT Si_3N_4 strongly depends on the concentration of SiH_2 formed during an intermediate reaction, which could be reduced by optimizing pressure, gas flow ratio, and deposition temperature. With the optimized process, good step coverage and good uniformity were achieved with the RT spacer film deposition system.

III. Fab Automation

As decreasing transfer time becomes more important for shorter processing times, we have addressed lot transfer with a newly developed high-speed run and transfer rail guided vehicle (RGV) used for intra-bay transportation. Interbay lot transfer is handled with an overhead shuttle (OHS) system combined with fast-access bay stations. Bay stations are conceptually different from stockers because they have been designed to minimize lot stay time between interbay and intrabay transport and are not used to stock lots. The combined effects of these newly developed transportation systems yield a total transfer time one-third that available with current commercial-based systems. The key to achieving this high-speed transportation is the use of the front opening unified pod (FOUP), which has been standardized by collaboration work in the international community. Wafers are fixed firmly inside the FOUP and do not vibrate under rapid acceleration. Therefore, wafers are not damaged and particles are not generated by high-speed transportation. In the conventional carrier case, the wafers might be subject to cracks due to this high-speed transfer. RGV itself has the advantage of reduced vibration during high-speed operation compared with automated guided vehicle (AGV) making it easier to increase the speed of the RGV. In order to fully utilize the RGV's high-speed performance, flexible and quick access to bay stations is indispensable. High-speed RGV areas are completely segregated by partitions for safety reasons. Images of RGV and OHS are shown in Fig. 3.

(a)



(b)

Fig. 3. Images of (a) RGV and (b) OHS used for quick wafer transportation.

Lot size in SWP is flexible, but with careful calculation we found that thirteen wafers per lot achieves the highest productivity while maintaining quick turn around time. Total process time including program load, wafer load/unload, wafer processing is 10.85 days and total wafer transfer time is 1.40 days for 13 wafers, 35 masks with sextuple metal 0.18-μm LOGIC. Total time without queuing time is 12.25 days (0.35 days per layer). Queuing time increases with WIP and unscheduled down time of equipment and other unexpected trouble, however, total cycle time of the SWP is much shorter than that of conventional batch process. Since the process time of SWP is proportional to the number of wafers in a lot, we use a smaller lot size (three wafers a lot, for example) for super cycle time reduction. We demonstrated 0.25 days per layer (6 h per layer) in a 0.18 μm LOGIC product in a three-wafer lot. This quick turn around time is very effective for development, device tuning for sophisticated LSI products, and yield enhancement

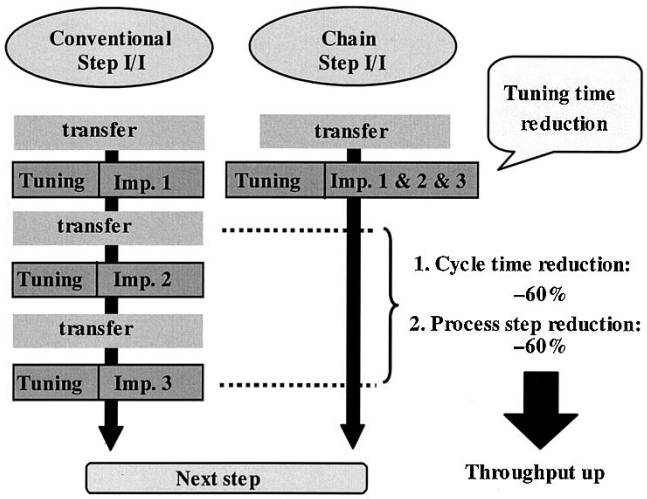


Fig. 4. Cycle time and process step reduction of well formation. Chain ion implantation is used instead of conventional three-step ion implantation.

efforts. Other large volume products, DRAM, flash also gain advantage from the SWP in the reduction of investment and elimination of risk.

IV. Process Integration

All process conditions were modified to fit SWP [11]. Moreover, we addressed cycle time reductions eliminating or modifying some process steps. One of the examples for process time reduction is well chain ion implantation, as shown in Fig. 4. We were successful in replacing conventional multistep high energy ion implantation, which required at least three lot transfers on a batch implanter, with a multi-step ion chain implantation process that required only one transfer step. Chain ion implantation, which is the only process that uses batch equipment in our fab, realizes triple well structure without high temperature and long-time anneal. All of the long time anneal processes are eliminated or replaced by RTA. One of the critical process steps is densification anneal of the STI filling oxide at around 1000 °C for 10 to 20 min in a conventional batch fab. Longer anneal gives us better film quality, better tolerance for HF, and less recess. We combined single-wafer HDP CVD oxide and RT anneal at 1000 °C for 20 s. The liner oxide condition is the key to eliminating damage from HDP CVD on gate oxide. This process change resulted in very good STI profiles without recesses or voids as shown in Fig. 5.

One potential drawback to a SWP is higher sensitivity to plasma damage. Backside films electrically float the wafer during plasma processing and reduce plasma damage. However, no films are deposited on the backside of the wafers in SWPs. Fig. 6 shows the gate leakage current dependence on HDP CVD film deposition temperature. We found that plasma damage is drastically reduced by using a lower deposition temperature, resulting in higher Q_{bd} (charge to breakdown) of the gate oxide film. All plasma processes—dry etching, other plasma CVD, sputter, and ashing—are carefully optimized to eliminate plasma damage. As a result, highly reliable gate oxide quality is obtained.

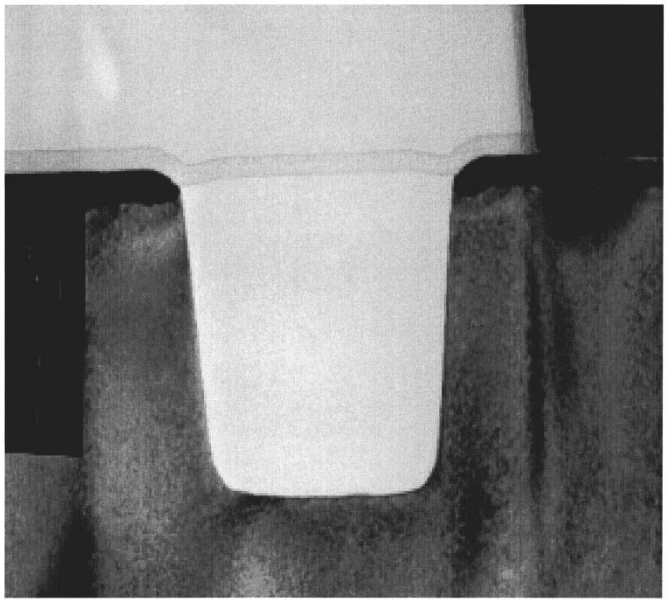


Fig. 5. Cross-sectional view of STI.

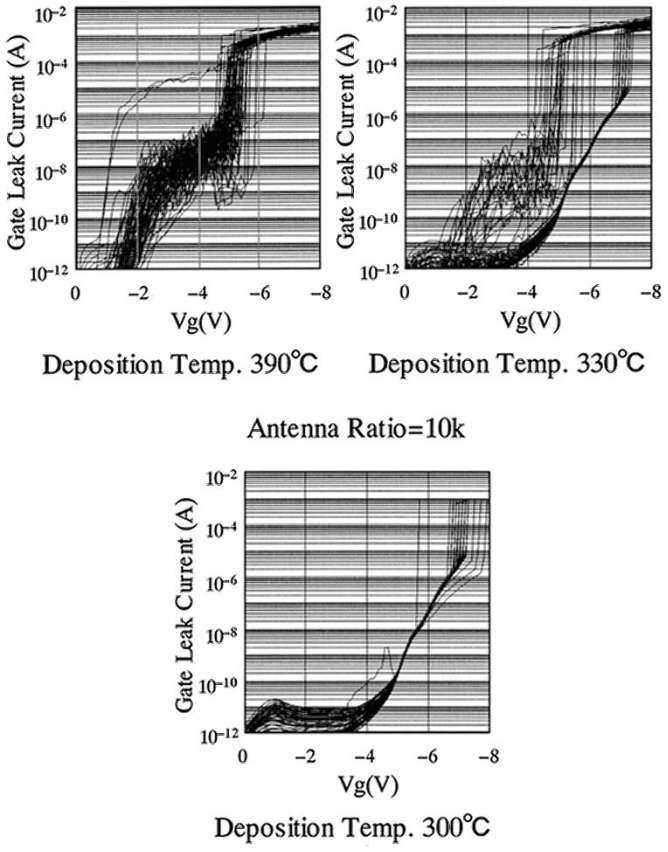


Fig. 6. Gate leakage current dependence on HDP deposition temperature measured on TEG with 10 k antenna ratio.

The absence of backside films makes mechanical stress control easier. Residual stress in backside films causes wafer warpage—a bigger problem in larger diameter wafers. Fig. 7 shows wafer warpage at each process step in this work. One of the most problematic types of film is CVD-W, which is subject to large compressive stresses. Mechanical stress is controlled

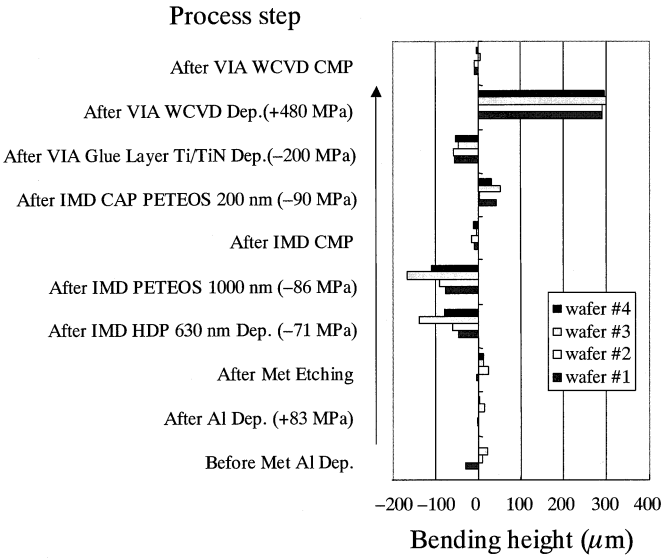


Fig. 7. Bending height of product wafer in each process step. Mechanical stress of each film is controlled to minimize wafer bending.

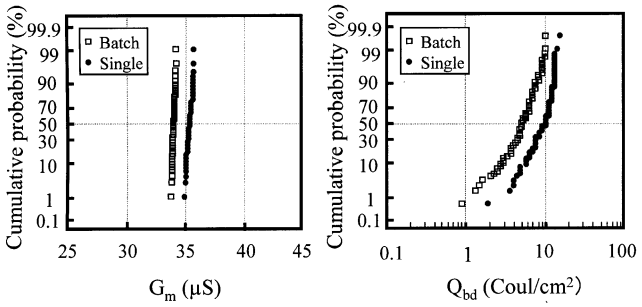


Fig. 8. Transconductance (left) and charge to breakdown (right) improvement by RT gate oxide compared with conventional furnace oxide.

by designing film deposition conditions so as to ensure mutual stress compensation and minimize wafer warpage. A combination of tensile and compressive films solved wafer warpage easily because of the absence of stress from backside films.

V. Device Characteristics

We used various rapid thermal processes to replace conventional furnace steps. A high-temperature single-wafer oxide system was introduced to replace the conventional batch type oxidation for gate oxide. Higher temperature oxidation is known to provide higher activation energy, which makes shorter process times possible and results in defect-free oxidation and a smoother surface finish. We combined higher temperature RT oxide and H_2 bake to get higher trans-conductance and better oxide integrity. As shown in Fig. 8, RT oxide showed better Gm and Q_{bd} characteristics compared with furnace oxidation. As N–Si bonding is stronger for higher temperature nitridation, our process improves hot carrier lifetime about one order of magnitude compared to lower temperature furnace process, as shown in Fig. 9. We use RT-polysilicon as a gate electrode since this film has fine and uniform grain, which is essential in order to suppress threshold voltage variation, especially in small size MOSFETs [12], [13]. RT-nitride spacers with a much

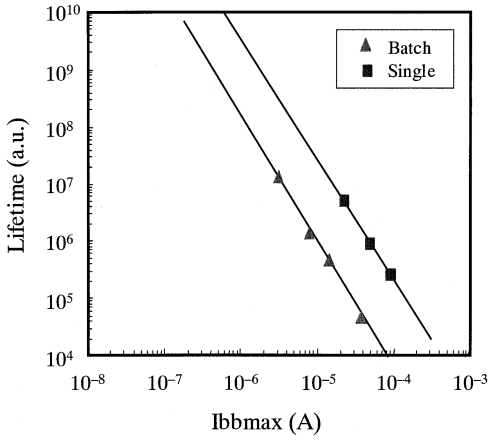


Fig. 9. Hot carrier lifetime comparison between RT gate oxide and conventional furnace oxide.

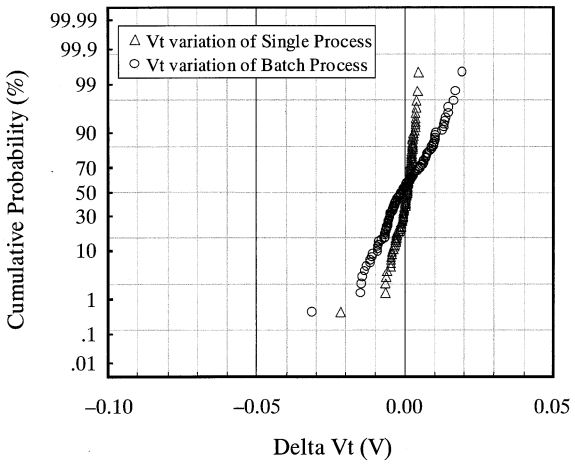


Fig. 10. Threshold voltage variation of SWP and batch process.

shorter deposition time gives shallower junction extensions and improves $V_{\rm th}$ rolloff, resulting in better uniformity of threshold voltage, as shown in Fig. 10. Better process control is achievable in SWPs because SWP enables process control feedback on a wafer by wafer basis. Overall, we demonstrated that our all SWP provided better device performance because of lower thermal budget and better control of device parameters. As we described, we obtained smaller variation in device performance with higher reliability, compared with the device obtained in a conventional fab.

VI. Yield Management

A. Quick Ramp Up With Systematic Defect Analysis

Defects that cause yield loss (at die-functionality testing) can be categorized as either systematic or random. Systematic defects are usually induced by conflict between product-design requirements and wafer-processing accuracy (usually the result of setting inadequate process windows), whereas random defects are often induced by particles and pattern defects. Since a process is not mature at the beginning of production, systematic defects can greatly influence yield improvement. The most important activity for shortening the time required for yield ramping is to quickly optimize "inline process parameters" (for

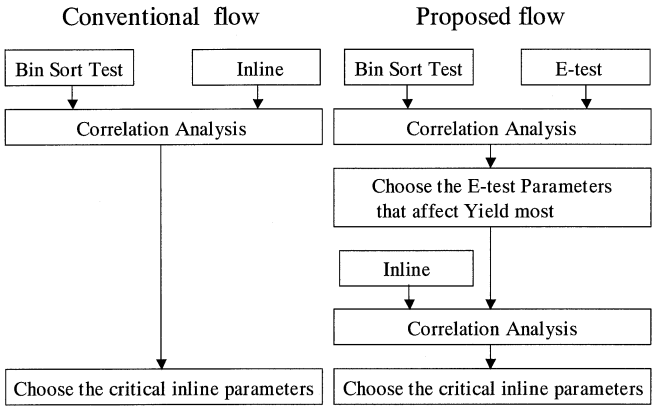


Fig. 11. Flow for detecting causes of yield loss related to marginal problems.

example, lithography critical-dimensions and film thickness). Conventionally, the relationship between "bin-data" (measured during die-functionality or die-yield testing) and inline process parameters is directly studied using statistical correlation analysis to identify the most critical inline process parameters for optimization, as shown on the left in Fig. 11. However, the volume of products in the early stages of production is limited, and inline process parameters usually are monitored with relatively low sampling frequency. This situation makes effective statistical analysis extremely difficult due to insufficient data.

To solve this problem, we applied the method illustrated in Fig. 11 (right side) and Fig. 12 [14]. The systematic yield is affected by several "e-test parameters" (basic electrical test-structure measurements taken at the end of the wafer fabrication process). To find the root cause of yield loss induced by systematic problems, we must first identify the yield impact of altering each e-test parameter. The first step in our method is to perform correlation analysis between bin data and e-test parameters to calculate the yield impact of each e-test parameter. We used "zone analysis," illustrated in Fig. 12, so as to effectively obtain more bin data from each wafer. In this analysis, the bin data is categorized into zones that correspond to the measurement points of the e-test. Bin data for each zone, rather than the average value of a wafer, is used for correlation analysis. This method enables us to obtain many more data points from a wafer, resulting in effective statistical analysis. As a 300-mm wafer has more die than a 200-mm wafer, zone analysis is much more effective for 300-mm wafers. Moreover, since the e-test is performed at several points on each wafer, the correlation between these two data types provides us with sufficient data points. Once critical e-test parameters are identified, correlation analysis between those e-test parameters and inline process parameters is performed to identify the inline process parameters to be modified.

B. Validation of Proposed Methodology

To evaluate the efficiency of our proposed systematic defect reduction method, we applied it to actual 300-mm wafer fabrication. In the pilot run of 0.18 μm Low-power SRAM, the main failure was large stand-by current. It is one of the typical systematic problems of SRAM and was observed in the wafer edge area. A composite map of standby current failure of one lot (13

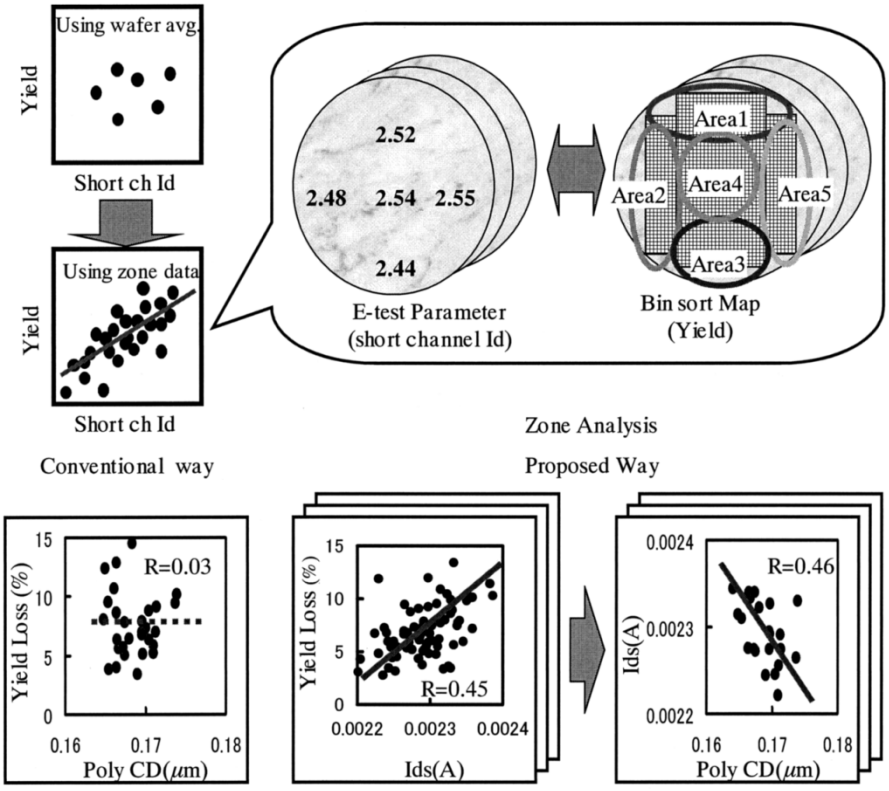


Fig. 12. Proposed Approach: Upper: Zone analysis; Lower: Results of implementing the proposed method.

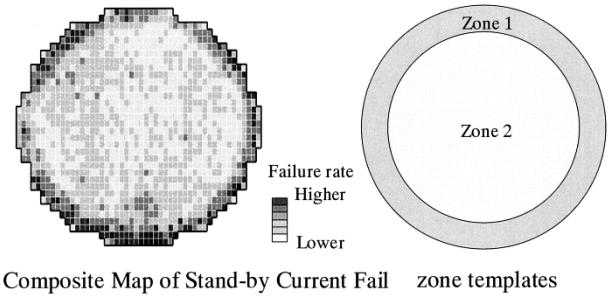
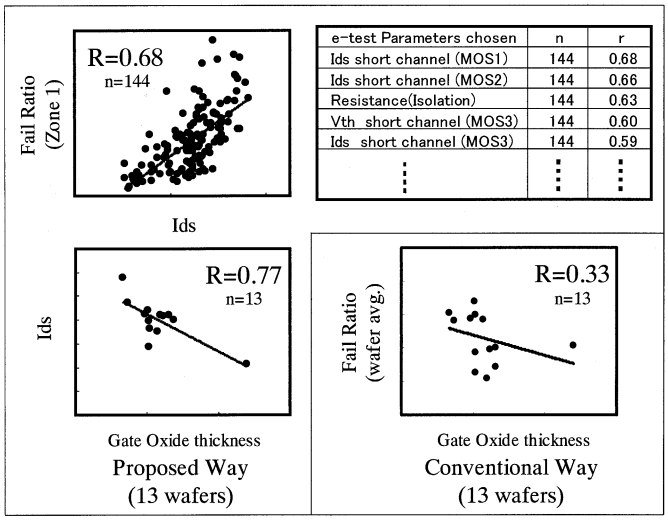


Fig. 13. Composite map of standby current failures (left) and templates used for zone analysis (right).



e-test Parameters chosen	n	r
Ids short channel (MOS1)	144	0.68
Ids short channel (MOS2)	144	0.66
Resistance(Isolation)	144	0.63
Vth short channel (MOS3)	144	0.60
Ids short channel (MOS3)	144	0.59

Fig. 14. Correlations between ratio of standby current failure and gate oxide thickness obtained by newly proposed method and conventional method. Top right: Table of Correlation coefficient (r) between failure mode and e-test parameter. Top left: Correlation between ratio of standby current failure and Ids, that has the highest correlation coefficient with the failure. Bottom left: Correlation between Ids and gate oxide thickness. Bottom right: Correlation between ratio of standby current failure and gate oxide thickness.

wafers) is illustrated in Fig. 13. We applied the zone templates shown in the figure. Then we examined the correlation analysis between the failure ratio and all of the e-test parameters. Ids of short channel MOSFET was identified as the most critical e-test parameter affecting standby current failure ratio. We then examined the relationship between this e-test parameter, short-channel Ids, and all of the inline parameters. The most significant inline parameter was found to be the gate oxide film thickness as shown in Fig. 14. These data points are obtained in the first lot containing 13 wafers. We can take quick action to improve the yield. Correlation between gate oxide thickness and standby current failure, obtained by the conventional approach, is also shown at the right-hand side of Fig. 14. The correlation coefficient is 0.33, which is much smaller than that with the proposed method. The conventional approach cannot detect the gate oxide film thickness as a significant parameter. We successfully found the root cause of the systematic error, reduced yield significantly in pilot lot, only in one lot containing 13 wafers. As a result of actually applying this method to 300-mm wafer fabrication, we reduced the systematic defects in the early stages of production resulting in improved yield ramp up. The method

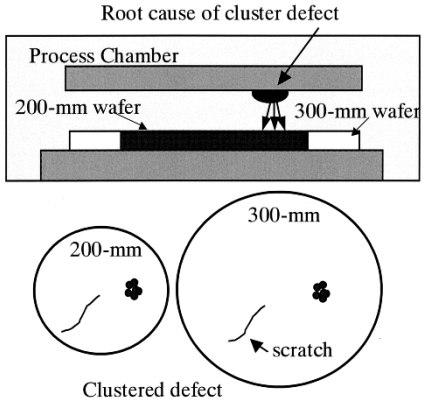


Fig. 15. Possible defect maps on 200- and 300-mm wafers.

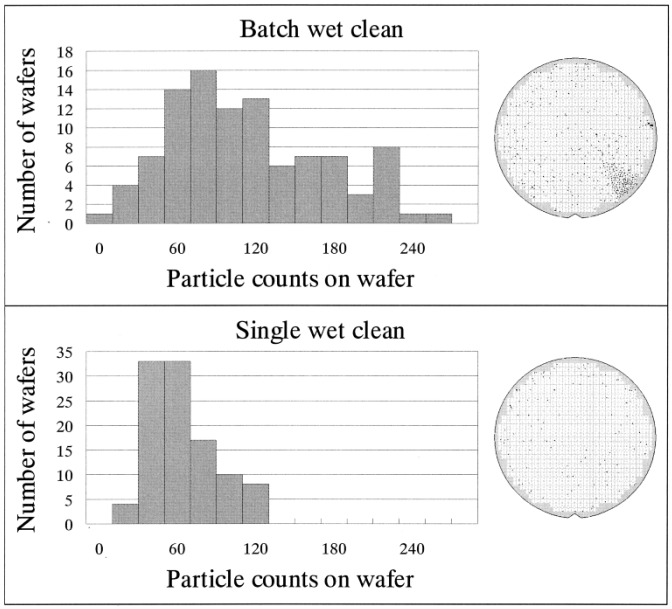


Fig. 16. Particle inspection results after wet clean. Batch wet clean (top). Single wet clean (bottom).

was proven to be useful for reducing yield loss due to systematic defects even in small-volume production.

C. Advantage of Yield Improvement on 300-mm SWP

We found out that a larger wafer size has the advantage with respect random defects. Some random defects might be proportional to the area, however, other defects, like scratch and clustered defects, have smaller impact for yield loss in larger diameter wafers as easily understood in the example depicted in Fig. 15. Thus, lower average defect density and higher yield are achieved in mass production.

SWP also has advantages in lower defect density. One of the well-known particle sources is the backside of the wafers. In CVD film deposition, oxidation, wet clean and other batch processes, wafers may be subject to contamination from the backside of adjacent wafers. However, SWP is not affected by the other wafers and has the benefit of particle or contamination reduction. Fig. 16 shows particle inspection results just after cleaning compared with batch and single wet process. Particles are inspected on one wafer per lot. Typical particle maps are also shown in Fig. 16. The average number of particles in the batch wet-process is higher than that of the single wet process with one of the sources being backside particles. The particles on the backside of the wafer are easily removed during the cleaning process but are re-attached on the surface of the adjacent wafer. On the other hand, in single wet processing there are no particles from the backside. In the particle map of the batch process, we can see a large number of particles from bottom left of the wafer. That is a typical example of the particles from the boat coming into contact with the edge of the wafer. These abnormal particles are suppressed in SWP. As the result, the number of particles on the wafer after cleaning is much smaller than that for the batch process. Thus, the SWP with 300-mm wafers provide a big advantage with respect to particle reduction.

VII. Conclusion

Production volume enhancement has been achieved through device scaling and increased wafer size. A new approach to cycle time reduction with SWP has been demonstrated, to develop a new strategy for future semiconductor manufacturing operations. A new EDA approach, increasing data points and detecting parametric error easily in early stage of production, has been implemented for a quicker yield ramp up. Fully integrated 0.18-μm technology with an all SWP in a 300-mm wafer fab provides drastic cycle time reduction. It also provides higher performance, higher reliability devices and lower defect density.

References

[1] R. R. Doering, "Trends in single-wafer processing," in *Dig. Tech. Papers, Symp. VLSI Technology*, 1992, pp. 2–5.

[2] A. Bowling, "Single-wafer processing and real-time process control for semiconductor integrated circuit manufacturing," in *Proc. Int. Symp. Semiconductor Manufacturing*, 1994, pp. 31–33.

[3] A. Koike, S. Shimoyashiro, K. Kubota, N. Suzuki, Y. Kiguchi, A. Fujisawa, A. Takamatsu, and T. Okabe, "A new LSI manufacturing scheme in the large-diameter wafer era for super-quick TAT development and volume production," in *Proc. Int. Symp. Semiconductor Manufacturing*, 1995, pp. 239–242.

[4] A. Koike, "A new fab concept in the 300 mm wafer era," in *Proc. Int. Symp. Semiconductor Manufacturing*, 2000, pp. 44–47.

[5] A. Koike, "Manufacturing in the 21st century," in *VLSI Symp.*, 2001, pp. 1–4.

[6] R. R. Doering and D. W. Reed, "Exploring the limits of cycle time for VLSI processing," in *Dig. Tech. Papers, Symp. VLSI Technology*, 1994, pp. 31–32.

[7] S. C. Wood, "Cost and cycle time performance of fabs based on integrated single-wafer processing," *IEEE Trans. Semiconduct. Manufact.*, vol. 10, pp. 98–111, Feb. 1997.

[8] M. Funabashi, S. Ikeda, M. Kuwabara, Y. Takeshima, N. Suzuki, S.Shunji Sasabe, and A. Koike, "Realization os single wafer wet cleaning in the 300 mm mass production line," in *Conf. Proc. Int. Symp. Semiconductor Manufacturing*, 2002, pp. 69–72.

[9] M. Itano, F. W. Kern Jr., M. Miyashita, and T. Ohmi, "Particle removal from silicon wafer surface in wet cleaning process," *IEEE Trans. Semiconduct. Manufact.*, vol. 6, pp. 258–267, Aug. 1993.

[10] T. Ohmi, T. Imaoka, J. Takano, and M. Kogure, "Segregation and removal of metallic impurity at interface of silicon and fluorine etchant," *J. Electrochem. Soc.*, vol. 140, pp. 811–817, 1993.

[11] C. Chen, T. Lin, J. Jung, N. Yabuoshi, Y. Sasaki, K. Komori, H. H. Shih, C. M. Liao, M. Funabashi, N. Suzuki, Y. Ishii, T. Uchino, K. Nemoto, H. Ymamoto, S. Nishihara, S. Sasabe, A. Koike, S. Ikeda, and J. Tsao, "Innovation of 300 mm fab manufacturing with single wafer technology," in *Tech. Dig. IEDM*, 2001, pp. 607–610.

[12] S. Ikeda, Y. Yoshida, K. Shoji, K. Kuroda, K. Komori, N. Suzuki, K. Okuyama, S. Kamohara, N. Ishitsuka, H. Miura, E. Murakami, and T. Yamanaka, "A highly manufacturable 0.18 sum generation LOGIC technology," in *Tech. Dig. IEDM*, 1999, pp. 675–678.

[13] H. P. Tuinhout, A. M. Montree, J. Schmitz, and P. A. Stolk, "Effect of gate depletion and boron penetration on matching of deep submicron CMOS transistors," in *Tech. Dig. IEDM*, 1997, pp. 631–634.

[14] K. Nemoto, S. Ikeda, O. Yoshida, S. Sasabe, and H. Su, "A statistical method for reducing systematic defects in the initial stages of production," in *Proc. Int. Advanced Semiconductor Manufacturing Conf.*, 2002, pp. 77–81.

Shuji Ikeda (M'91–SM'02) was born in Tokyo, Japan, in 1956. He received the B.S. degree in physics from Tokyo Institute of Technology, Tokyo, Japan, in 1978, and the M.S. degree in electrical engineering from Princeton University, Princeton, NJ, in 1987.

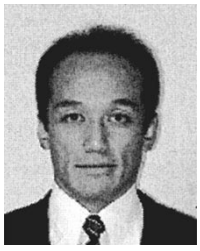
He joined Semiconductor and Integrated Circuit Group, Hitachi ltd., Tokyo, Japan, in 1978, where he was engaged in research and development of state of the art SRAM process and devices, including high resistive poly load / thin film transistors for SRAM application and high performance MOS devices. He was also working on developing process technology for LOGIC, embedded memories, and CMOS power RF devices and transferring the technology to mass production line. In October 2000, he joined Trecenti Technologies Inc, established in March 2000 as a first 300-mm single-wafer fab, where he is a General Manager of Products Technology Division. His interests are on process integration/yield improvement of high-performance microprocessors, LOGIC, embedded memories, Flash and SRAM. He has authored over thirty technical papers on device technology, process integration and manufacturing including several invited papers. He has served on the committee of IEEE International Electron Devices Meeting (IEDM) since 1993. He was a General Chairman of 2002 IEDM.

Dr. Ikeda received R & D 100 award in 1999 for the contribution on development of SH Risk-microprocessor.

Kazunori Nemoto (M'95) received B.S. and M.S. degrees in management science from the Science University of Tokyo, Tokyo, Japan, in 1984 and 1986, respectively.

He joined the Semiconductor and Integrated Circuit Division of Hitachi, Ltd., Japan, in 1986. He has been in charge of manufacturing technology for wafer fabrication. From 1995 to 1996, he was a visiting scholar at Purdue University, West Lafayette, IN, working on TAT reduction for semiconductor manufacturing. He is currently a senior manager in manufacturing technology department of Trecenti Technologies, Inc., joint venture UMC and Hitachi. His research interests include process control methods and yield improvement methodology.

Mr. Nemoto is a member of the IEEE Components, Packaging and Manufacturing Technology Society.



Michimasa Funabashi received the B.S. and M.S. degrees in image science from Chiba University, Japan, in 1984 and 1986, respectively.

He joined the Semiconductor and Integrated Circuit Division of Hitachi Ltd., Japan, in 1986. He has been in charge of process development of semiconductor manufacturing. From 1994 to 1996, he was a visiting researcher at Stanford University working on development of new chemicals for wet cleaning. He is currently a senior manager of Trecenti-technologies, Inc., and a member of the Electrochemical society.

Toshiyuki Uchino (M'01) received the B.S. degree in mechanical engineering from the University of Tokyo, Tokyo, Japan, in 1984 and the M.S. degree in manufacturing systems engineering from the University of Wisconsin, Madison, in 1990.

He is a senior manager of Manufacturing Technology B Department of Trecenti Technologies, Inc. He worked at Hitachi for 15 years as an equipment engineer of thermal process. He had contributed to development of vertical diffusion furnace. Since he joined Trecenti in 2000, he played a major role in start-up of the first 300-mm volume production fab. He is one of the key members in the Factory Integration section of the International Technology Roadmap for Semiconductors (ITRS).

Hirohiko Yamamoto was born in Fukuoka, Japan in 1956. He received the B.S. degree in Industrial chemistry from Kumamoto University, Kumamoto, Japan in 1981.

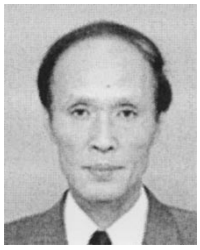
He joined HITACHI Microcomputer Engineering Inc.(present HITACH ULSI systems Inc.), Tokyo, Japan, 1981, where he has been working on development and improvement of CVD technology for mass production. He is presently CVD technology section manager of Manufacturing Technology Department of Trecenti Technologies Inc.

Noriyuki Yabuoshi was born in Aichi, Japan in 1964. He received the B.S. and M.S. degrees in electronic engineering from Nagoya University, Aichi, Japan, in 1987 and 1989, respectively.

He joined Semiconductor and Integrated Circuit Group, Hitachi ltd., Tokyo, Japan, in 1989, where he has been working on development of the Logic/SRAM process technologies. He is presently a manager of Logic/SRAM Process Integration group of Trecenti Technologies Inc. His responsibility includes process integration/yield improvement of high-performance microprocessors, logic, and SRAMs.

Yasushi Sasaki was born in Tokyo, Japan in 1969. He received the B.S. degree in physics from Toho University, Chiba, Japan in 1992.

He joined Semiconductor and Integrated Circuit Group, Hitachi ltd., Tokyo, Japan in 1992, where he has been working on development of the Logic process technologies. He is presently a manager of Logic/SRAM Process Integration group of Trecenti Technologies Inc. His responsibility includes process integration/yield improvement of high-performance microprocessors, logic and SRAMs.



Kazuhiro Komori was born in Tochigi Prefecture, Japan in 1951. He graduated Tochigi Prefectural Motegi High School, and joined Semiconductor Division, Hitachi Ltd, Tokyo, Japan in 1970.Then he studied electronics engineering at Hitachi Keihin Technical College in 1975, and semiconductor engineering in Tokyo University in1976.

He joined Process Engineering Development Department of Semiconductor and Integrated Circuit Group, Hitachi Ltd., in 1977, where he had been working on research and development of state of the art nonvolatile memory process and devices including yield enhancement in mass production line. He joined Trecenty Technologies Inc. in 2000, where he had working on process Integration for SRAM,logic, and nonvolatile memory products. He joined BBK Electronics Corp. Ltd, Guangdong, China, in 2002, and he is working on research and development of electronic educational products.

Norio Suzuki received the B.S. and M.S.degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1977 and 1979,respectively.

He joined Semiconductor and Integrated Circuit Group, Hitachi Ltd., Tokyo, Japan, in 1979, and has been engaged in the developments of process integration for SRAM and state-of-the-art oxidation. He is presently a manager of Manufacturing Technology B Department of Trecenti Technologies Inc. His responsibility includes the improvement of diffusion process, wet cleaning process and the analysis of process data.

Shinji Nishihara was born in Hyogo, Japan in 1956. He received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1981, and M.S. degree from Osaka University, Osaka, Japan, in 1983.

He joined Semiconductor and Integrated Circuit Group, Hitachi Ltd., Tokyo, Japan, in 1983, where he has been working on research and development of metallization process, sputtering equipment and yield enhancement in mass production line. He has been the leader of Interconnect Working Group in STRJ from 1998 to 2000. He is presently a manager of Manufacturing Technology Department of Trecenti Technologies Inc. His responsibility includes module process and equipment; Lithograph, Dry Etching, CVD, PVD and CMP. He is a committee member of SEMI Technology Symposium since 1999.

Shunji Sasabe received B.S. degree in applied physics from Osaka City University, Osaka, Japan, in 1975 and M.S. degree in applied physics from Nagoya University, Aichi, Japan, in 1977.

He joined Device Development Center of Hitachi, Ltd., Japan in 1977. He has worked for Trecenti Technologies Inc. since 2000 as a department manager of manufacturing technology department. He is currently a general manager of Dainippon Screen MFG. Co. Ltd. His research activities include the module process technology of semiconductor manufacturing.

Atsuyoshi Koike (M'02) received the B.S. and M.S. degrees in engineering from Waseda University, Japan, in 1976 and 1978. respectively, and the Ph.D. degree in electrical engineering from Tohoku University, Japan, in 2002.

He is currently President and CEO of Trecenti Technologies, Inc. He has more than 20 years of experience in development of process and manufacturing technology in Hitachi, Ltd. Before joining Trecenti, he was the General Manager of Semiconductor Manufacturing Technology Division, Semiconductor & Integrated Circuits of Hitachi, Ltd. In Hitachi, he had long studied highly efficient manufacturing technology, especially single-wafer processing for cycle time reduction over ten years. He was also served as Chairman of J300E and played a key role of collaboration work with I300I in order to build solid foundation of 300-mm standards.