

The Impact of Tolerance on Kill Ratio Estimation for Memory

Oliver D. Patterson, *Member, IEEE* and Mark H. Hansen

Abstract—Spatially correlating in-line inspection data and post-process electrical test data is an effective approach for estimating the yield impact of different defect types and/or process steps. An estimator for the probability that a particular type of defect kills an electrically testable structure, the kill ratio, has been described in the literature. This estimator may be used to predict the yield impact immediately after inspection, providing a number of benefits. It may also be used to generate a yield loss pareto by defect type. This paper introduces a new estimator for the kill ratio, which takes into account the impact of tolerance, a parameter setting the maximum distance between a defect and structure under which they are considered spatially correlated. This estimator was developed for memory (bitmap) data, where the tolerance is very large relative to the size of the structure. The tolerance is often increased to accommodate for misalignment between inspection tool sets and the electrical data. The problem with increasing the tolerance is that the chance of coincidental correlation between failed bits and defects increases as the square of tolerance. Analytical and simulation results are presented to illustrate the danger of using the existing kill ratio estimator with too large a tolerance or overly sensitive inspection tool recipes. These same results illustrate the improved performance of the new estimator. Because the number of falsely attributed defects adds up over a number of inspections, a small error in the kill ratio estimator can have a major impact on the yield loss pareto.

Index Terms—Bitmap, kill ratio, overlay of electrical and defect data, yield loss pareto, yield modeling.

I. INTRODUCTION

Spatial correlation of in-line inspection data and end-of-line electrical test data, also known as overlay analysis, may be used to identify killer defects and their process step of origination. This information is useful for prioritizing yield improvement efforts, tracking yield loss contributions by process step or defect type, and predicting yield [1]–[4]. Overlay analysis may be applied to any type of electrically testable structure, including whole product die, comb test structures [5] and individual bits in an array of memory [4], [6], [7]. Application to memory is useful for a number of reasons. First, the chance of defects from different inspections correlating with the same electrical failure is small even for very high defect densities due to the small size of a bit of memory. Second, memory is a part of many products and therefore fabrication of nonrevenue generating test structures is not necessary.

Two useful metrics typically used in analyzing overlay analysis data are the kill ratio, which is defined as the increased chance of a structure being rejected when a defect of type i is present relative to the baseline yield, and the defect limited yield, which is defined as the upper limit for circuit yield which would be obtained if a particular visual defect type were the only factor limiting the overall yield [3]. Defect types are often broken down by inspection step but may also be broken down by defect characteristics. The following estimators for the kill ratio, KR_i^{lit} , and defect limited yield, LY_i^{lit} , for a defect of type i , denoted d_i , are defined in the literature [3]

$$KR_i^{\text{lit}} = 1 - \frac{1 - u^{\text{lit}}}{1 - b^{\text{lit}}} \quad (1)$$

$$LY_i^{\text{lit}} = 1 - P(i)KR_i^{\text{lit}} \quad (2)$$

where

$$u^{\text{lit}} = 1 - \frac{\text{total good structures with } d_i \text{ observed}}{\text{total structures with } d_i \text{ observed}} \quad (3)$$

$$b^{\text{lit}} = 1 - \frac{\text{total good structures where } d_i \text{ is not observed}}{\text{total structures where } d_i \text{ is not observed}} \quad (4)$$

and

$$P(i) = \frac{\text{total structures with } d_i \text{ observed}}{\text{total structures}}. \quad (5)$$

The kill rate u^{lit} is an estimate of the conditional probability that a structure will fail given that defect i is present on the structure; the kill rate b^{lit} is an estimate of the conditional probability that a structure will fail given that defect i is not present on the structure, and $P(i)$ is an estimate of the probability that a defect of type i occurs on a structure. The superscript *lit* stands for literature. For convenience, (3) and (4) are presented in a simplified form, where the inspection tools are perfect, i.e., the probability that an existing defect is missed is 0, and the probability that a defect is detected although it really does not exist is 0.

This theory assumes a one-to-one correspondence between defects and electrical structures (i.e., an observed defect will only impact the electrical structure that it appears to lie on). This will be the case for large test structures, but not for memory. The size of a bit of memory for 0.16- μm technology is roughly 5 μm^2 , whereas the positional inaccuracy of state-of-the-art optical inspection tools is much worse. Based on a set of tool accuracy experiments conducted at Agere Systems, defect wafer maps for the same wafer can be as far as 25 μm offset for two different KLA 2138s. The offset between wafer maps

Manuscript received January 22, 2001; revised January 26, 2002.

O. D. Patterson is with Agere Systems, Orlando, FL 32819 USA (e-mail: odp@agere.com).

M. H. Hansen is with Bell Laboratories, Murray Hill, NJ 07974-0636 USA. Digital Object Identifier 10.1109/TSM.2002.804875

from a KLA 2138 and a Surfscan AIT may be as much as $75 \mu\text{m}$. These values assume the inspection tool recipes are set up analogously. If different locations for the die origin are selected (e.g., the middle of the intersection of the two scribe lines for one tool and the bottom left corner of the die for the other tool), the positional inaccuracy will be much worse. Therefore, even if a defect does in fact cause an electrical failure, the position on the defect wafer map may be $75 \mu\text{m}$ or greater from the location of the failed bit on the electrical wafer map. Also, the same defect may be identified at multiple inspections but may similarly be offset from wafer map to wafer map. Therefore, a new theory is needed to address the situation where each observed defect can correspond to one out of a large number of electrical structures.

To address the issue of positional inaccuracy between inspection tools and the electrical wafer map, overlay analysis packages include a parameter called tolerance, t [8]. The tolerance is the maximum distance between two events (defect to defect or defect to electrical failure) to be considered spatially correlated. When a nonzero t is used, an error is introduced into KR_i^{lit} and LY_i^{lit} . This error is the chance of coincidental correlation (i.e., the chance that an unrelated defect is within the t of a failed bit). The error in KR_i^{lit} will be shown to be approximately equal to the total area within t of any electrical failure divided by the total inspected wafer area. This error increases with the square of t and linearly with the number of electrical failures.

A new estimator for kill ratio, which takes into account the impact of t , is derived in this paper. This estimator is compared to KR_i^{lit} for different t and electrical and physical defect densities analytically and through simulation. The impact of these variables on the yield loss pareto is also quantified.

II. KILL RATIO

Hall *et al.* [2] shows how contingency table analysis may be used to determine whether two variables of classification, the existence of a defect of type i on a die and the functionality of the die, are correlated. For memory, different class variables as shown in Fig. 1 are appropriate. Let A be defined as all area within t of a defect of type i . This area is shaded in the example wafer map in Fig. 2. The remaining inspected area, \bar{A} , is shaded in Fig. 3 for the same example wafer map. For now, assume that no two defects are within t of each other. We will look at the impact of violating this assumption in a Section VI. Let fail_area be the number of electrical failures multiplied by the area in a circle of radius t , a tolerance ball. The OK_area is the remaining area. In A , the fail_area is equivalent to the number of hits (defects within t of a failure) multiplied by the area in a tolerance ball, while the OK_area is the number of misses (defects not within t of a failure) multiplied by the area in a tolerance ball. In \bar{A} , the fail_area is the area where a hypothetical defect could land and be within t of an electrical failure, whereas the OK_area is the area where a hypothetical defect could land without being within t of an electrical failure.

The independence of A versus fail_area may be determined by comparing

$$u = \frac{\text{hit_area}}{A} \quad (6)$$

	A	\bar{A}	total
fail_area	hit_area	area_for_a_hit	
ok_area	miss_area	area_for_a_miss	
total	A	\bar{A}	total_area

Fig. 1. Contingency table for determining whether a defect of type i impacts yield.

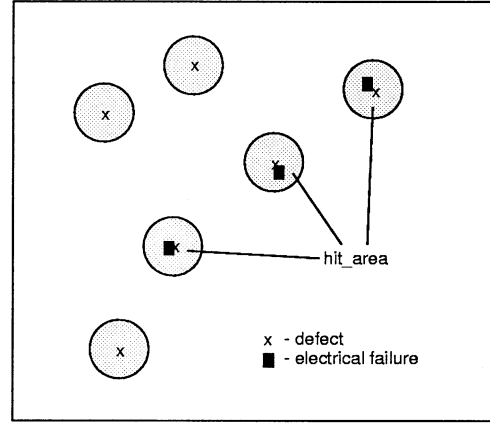


Fig. 2. Example of A . The area, A , is shaded. The hit_area is indicated. The remaining shaded area is the miss_area.

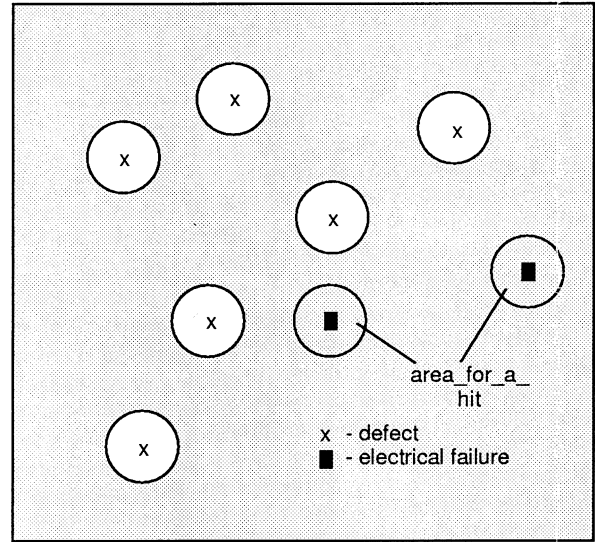


Fig. 3. Example of \bar{A} . The area, \bar{A} , is shaded. The area_for_a_hit is indicated. The remaining shaded area is the area_for_a_miss.

and

$$b = \frac{\text{area_for_a_hit}}{\bar{A}} \quad (7)$$

using a Chi-squared statistic. The kill rate u is an estimate of the probability that a bit within t of a defect will be dead at electrical test. The background kill rate b is an estimate of the probability

that a bit will be dead given it is not within t of a defect. (Similar notation to reference [3] is adopted to facilitate comparison to the existing theory. For ease of notation, estimators are not notated with hats, since the symbols in this paper are predominantly estimators.) Dependency of these variables indicates that the presence of a defect changes the likelihood that the structure upon which it lies will be rejected. In this paper, we will assume that the inspection tools are perfect. If the classification variables A and fail_area are dependent, then u and b will have significantly different values.

The kill ratio KR_i can be derived using u and b

$$KR_i = 1 - \frac{1 - u}{1 - b}. \quad (8)$$

This new estimator is similar to (1) but is a function of u and b rather than u^{lit} and b^{lit} . The kill rate u simplifies to u^{lit} , so the only difference between kill ratio estimators is the b term. Note that the estimator KR_i^{lit} was developed for the more general case where the inspection tools are imperfect in reference [3]. The estimator KR_i can be similarly generalized.

It is not necessary to determine the actual regions for A , \bar{A} , hit_area , and area_for_a_hit to determine u , b , and KR_i . Instead, these regions may be quantified by an approximation of their area. First A and \bar{A} are calculated

$$A = \max(N\pi t^2, N * \text{bit_area}) \quad (9)$$

$$\bar{A} = \text{total_area} - A \quad (10)$$

where N is the number of defects, total_area is the total inspected area, and bit_area is the area of a single bit. Equation (9) is an approximation for A ; for small values of t the tolerance balls approach the form and size of a bit of memory. This approximation makes it possible to span from one estimator to another. Generally, t^2 will be large compared to the area of a bit.

Next the defect wafer map is overlaid with the electrical wafer map to obtain the number of hits h , missed defects m_d , and missed electrical failures m_E

$$m_d = N - h \quad (11)$$

$$m_E = E - h \quad (12)$$

where E is the total number of bit failures. From these variables, u and area_for_a_hit are calculated

$$u = \frac{h}{N} \quad (13)$$

$$\text{area_for_a_hit} = \max(m_E \pi t^2, m_E \text{bit_area}). \quad (14)$$

Equation (14) is an approximation since tolerance balls around electrical failures could intersect with each other or A . The background hit rate b , is calculated using (7).

Both u and b are bound by 0 and 1. Although in practice u will occasionally be smaller than b , resulting in a negative value for KR_i , it does not make sense that the presence of a defect should decrease the chance of failure. Therefore, KR_i should also be bound by 0 and 1. Negative values of KR_i will routinely occur when the true KR_i is 0 or very small and are not reason for concern. When t is 0, b becomes b^{lit} and the expression for KR_i exactly matches KR_i^{lit} .

In order to demonstrate this estimator, a model is necessary. The underlying probabilistic model, which describes the true process, will be represented by u^{model} , b^{model} and KR_i^{model} . This model will be used in both the simulation and analytical sections.

III. YIELD LOSS PARETO

In order to prioritize yield improvement opportunities, the yield impact of the different defect types must be compared. A standard way is through the use of the defect limited yield which may be expressed similarly to (2) but as a function of KR_i

$$LY_i = 1 - P(i)KR_i. \quad (15)$$

The term $P(i)$ may be expressed as the ratio of N to the total number of bits total_bits , resulting in the following estimate for LY_i :

$$LY_i = 1 - \frac{NKR_i}{\text{total_bits}} = 1 - \frac{E_{ai}}{\text{total_bits}} \quad (16)$$

where E_{ai} is the number of electrical failures attributed to defect i . Rather than generating a pareto of LY_i for all defect types, it may be more useful to generate a pareto of E_{ai} since LY_i is dependent upon the test structure size. From E_{ai} , LY_i for any test structure or chip size may easily be determined. The attributed failures E_{ai} may be calculated in a number of ways

$$E_{ai} = NKR_i = N - \frac{m_d}{1 - b}. \quad (17)$$

IV. ANALYTICAL COMPARISON TO EXISTING FORMULAS

The new estimator KR_i is analytically compared to KR_i^{lit} in this section. The error in the kill ratio estimate is defined as

$$KR_i^{\text{error}} = KR_i^{\text{lit}} - KR_i \quad (18)$$

and is expressed as a percentage of 1, the maximum possible value for a kill ratio. The error in E_{ai} is defined as a percentage of the total number of electrical failures

$$E_{ai}^{\text{error}} = \frac{NKR_i^{\text{lit}} - NKR_i}{E}. \quad (19)$$

In the simulation results that follow, we show that the difference between KR_i and KR_i^{model} , the true kill rate for defect i used in the model, is much, much smaller than the difference between KR_i^{lit} and KR_i^{model} . Therefore, KR_i^{error} and E_{ai}^{error} are representative of the true error in KR_i^{lit} and E_{ai}^{lit} .

Since a bit covers an extremely small area, even for very high levels of random yield loss, $b^{\text{lit}} \cong 0$ and

$$KR_i^{\text{lit}} \cong u. \quad (20)$$

An expression for KR_i^{error} may be obtained using (8), (18), and (20):

$$KR_i^{\text{error}} \cong \frac{b(1 - u)}{1 - b}. \quad (21)$$

TABLE I
 ERRORS IN KR_i^{lit} AND E_{ai}^{lit} FOR A RANGE OF VALUES FOR \bar{N} , \bar{E} , t , total_area AND KR_i^{model} .
 ALL VALUES ARE NORMALIZED TO COUNTS OR AREA PER WAFER

case	\bar{N}	\bar{E}	t cm	total_area cm ²	KR_i^{model}	h	u	\bar{A} cm ²	area_for_a hit cm ²	b	KR_i	KR_i^{error}	E_{ai}^{error}
1	4000	2000	0.015	300	0.0	19	0.005	297	1.4	0.005	0.0	0.5%	0.9%
2	8000	2000	0.015	300	0.0	38	0.005	294	1.4	0.005	0.0	0.5%	1.9%
3	4000	4000	0.015	300	0.0	38	0.009	297	2.8	0.009	0.0	0.9%	0.9%
4	4000	2000	0.030	300	0.0	75	0.019	289	5.4	0.019	0.0	1.9%	3.8%
5	4000	2000	0.015	150	0.0	38	0.009	147	1.4	0.009	0.0	0.9%	1.9%
6	4000	2000	0.015	300	0.1	414	0.103	297	1.1	0.004	0.1	0.3%	0.7%
7	4000	2000	0.015	300	0.2	809	0.202	297	0.8	0.003	0.2	0.2%	0.5%
8	4000	2000	0.015	300	0.3	1205	0.301	297	0.6	0.002	0.3	0.1%	0.3%
9	4000	2000	0.015	300	0.5	2000	0.500	297	0.0	0.000	0.5	0.0%	0.0%
10	8000	2000	0.015	300	0.1	820	0.103	294	0.8	0.003	0.1	0.3%	1.0%
11	4000	4000	0.015	300	0.1	431	0.108	297	2.5	0.01	0.1	0.8%	0.8%
12	4000	2000	0.030	300	0.1	454	0.114	289	4.4	0.02	0.1	1.4%	2.7%
13	4000	2000	0.015	150	0.1	427	0.107	147	1.1	0.01	0.1	0.7%	1.4%
14	3000	1200	0.016	300	0.0	10	0.003	298	1.0	0.0032	0.0	0.3%	0.8%
15	3000	1200	0.016	300	0.1	307	0.102	298	0.7	0.0024	0.1	0.2%	0.5%
16	3000	1200	0.016	300	0.2	604	0.201	298	0.5	0.0016	0.2	0.1%	0.3%
17	6000	2400	0.016	300	0.0	39	0.006	295	1.9	0.0064	0.0	0.6%	1.6%
18	6000	2400	0.016	300	0.1	626	0.104	295	1.4	0.0048	0.1	0.4%	1.1%
19	6000	2400	0.016	300	0.2	1215	0.203	295	1.0	0.0032	0.2	0.3%	0.6%

In the case where defect i does not affect yield, u and b will be identically distributed. For large total_area, u and b will approach their population quantities, u^{model} and b^{model} . Therefore, large sample approximations for KR_i^{error} and E_{ai}^{error} when defect i does not affect yield are

$$KR_i^{\text{error}} \cong b = \frac{E\pi t^2}{\bar{A}} \cong \frac{E\pi t^2}{\text{total_area}} \quad (22)$$

and

$$E_{ai}^{\text{error}} \cong \frac{N\pi t^2}{\bar{A}} \cong \frac{N\pi t^2}{\text{total_area}}. \quad (23)$$

Equation (23) was obtained from (17) and (22). It could just as easily be derived intuitively; it is the percentage of area on the wafer an unrelated electrical failure could fall and be within t of a defect (i.e., coincidentally correlate with a defect). Equations (22) and (23) show that: KR_i^{error} is proportional to the electrical defect density, $E/\text{total_area}$, and t^2 , but is independent of N ; also E_{ai}^{error} is proportional to the physical defect density, $N/\text{total_area}$, and t^2 , but is independent of E . Equations (22) and (23) may be used to approximate the significance of using KR_i versus KR_i^{lit} .

Table I compares KR_i and E_{ai} to KR_i^{lit} and E_{ai}^{lit} for different values of N , E , t , and KR_i^{model} . Similar to (22) and (23), these results represent what would be observed for very large sample sizes where the variance in the estimators is approximately 0. The values in Table I are expressed on a per wafer basis. The purpose of this table is to give the reader an idea of the size of the error in KR_i^{lit} and E_{ai}^{lit} for a set of possible values.

The number of hits, h , is calculated by summing the hits due to defect i with the random hits

$$h = NKR_i^{\text{model}} + (E - NKR_i^{\text{model}}) \frac{(A - NKR_i^{\text{model}}\pi t^2)}{\text{total_area}}. \quad (24)$$

The hits due to defect i are approximated using NKR_i^{model} . The kill rates u and b are calculated using (7) and (13). The estimator KR_i and KR_i^{error} are calculated using (8) and (21). Lastly, E_{ai}^{error} is calculated using (23).

Nineteen different cases are included in Table I. The values used are at the upper limits of the normal range to depict the worst case. Use of a t of 150 μm is not uncommon to cover for all possible sources of misalignment as discussed in Section I. For all 19 cases, KR_i exactly predicts KR_i^{model} . Therefore, KR_i^{error} and E_{ai}^{error} represent the error in KR_i^{lit} and E_{ai}^{lit} .

The first case is the baseline case, which is used for comparison with the other cases to show the effect of varying the different variables. The variable KR_i^{model} is 0; the defects do not impact yield. The estimator, KR_i equals KR_i^{model} whereas KR_i^{lit} equals 0.005, a 0.5% error. The corresponding error in E_{ai}^{lit} is 0.9%.

As in case 1, KR_i^{model} is also 0 for cases 2–5. In these cases, the variables N , E , t , and total_area are changed in turn. The effects are as expected based on (22) and (23).

Cases 6–13 show the inaccuracy of KR_i^{lit} and E_{ai}^{lit} when KR_i^{model} is not equal to zero. Cases 6–9 show that the errors decrease as KR_i^{model} is increased. In the extreme case, case 9, all the electrical failures are caused by defect i . Therefore,

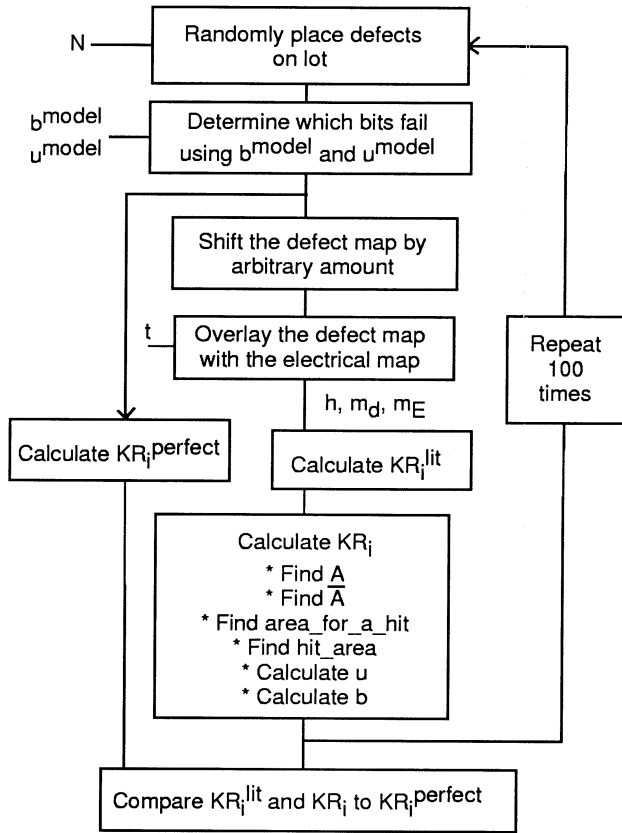


Fig. 4. Simulation.

area_for_a_hit is 0, b is 0, and KR_i^{error} is 0. Cases 10–13 show the effects of varying variables N , E , t , and totalArea when KR_{model} is nonzero. The errors are attenuated from the corresponding cases when KR_{model} is zero. Cases 14–19 are included to compare with the simulation results described in the next section.

Among all the cases in Table I, the largest errors in KR_i^{lit} and E_{ai}^{lit} occurred for $N = 4000$, $E = 2000$, $t = 300 \mu\text{m}$ and $A = 300 \text{ cm}^2$, the fourth case. The values for N , E , and t are on the high extreme of what might be used or observed in industry. The error in KR_i^{lit} for this case is 1.9%. This indicates that although KR_i is a more precise estimator for the kill ratio, in many cases, KR_i^{lit} is adequate. The effect on E_{ai}^{lit} is more detrimental. For this case, the error in E_{ai}^{lit} is 3.8%. A total of 75 of the 2000 electrical failures were falsely attributed to this defect. Alone possibly this is not so bad, however this error compounds with the number of inspections. For instance, consider the extreme case of ten inspections similar to this one (i.e., possessing comparable values for N and KR_{model}) and no two defects lying within $2t$ of each other (i.e., no overlapping tolerance balls). For each inspection, on average 3.8% of the failures would be erroneously attributed. In total, approximately 38% of the failures would be erroneously attributed. Most likely, the tolerance balls of some of these defects would overlap and therefore the percentage of electrical failures erroneously attributed would be somewhat smaller than 38%. Still, the yield loss pareto would contain close to 38% of the electrical failures and their relative magnitudes would be fully a function of noise, when in reality none of the captured defects caused a failure. The new

estimator E_{ai} accurately estimates the true number of killer defects by level and may be used to interpret the yield loss pareto.

V. SIMULATION

A simulation was developed to test the performance of KR_i . This simulation is described in the box diagram in Fig. 4. For this simulation, N , E , and KR_i^{model} are specified. A tolerance of $160 \mu\text{m}$ was used for all the simulation experiments reported in this paper. First, defects were randomly placed on a lot of 25 wafers, with each wafer consisting of $600 \times 3000 \times 4000$ bit memory arrays. This product is a hypothetical example. We assume each bit is $2 \times 2 \mu\text{m}^2$ so that the entire array is 0.48 cm^2 . A total of $25 \times N$ defects are randomly placed throughout the lot. With 4000 defects, very few landed within $2 \times t$ of each other, although this is allowed in the simulation. Which bits fail is determined using the modeled kill rates, u^{model} and b^{model} , which can be calculated from KR_i^{model} , E , and N using Eqn. (8) and the following expression for the probability of a failure:

$$P(\text{fail}) = P(\text{fail}|\text{defect})P(\text{defect}) + P(\text{fail}|\text{no defect})P(\text{no defect}). \quad (25)$$

In the simulation, we set

$$P(\text{defect}) = \frac{N}{\text{bits_per_wafer}} \quad (26)$$

and

$$P(\text{fail}) = \frac{E}{\text{bits_per_wafer}}. \quad (27)$$

Thus, (25) can be expressed in terms of E , u^{model} , b^{model} , and N

$$E = u^{\text{model}}N + b^{\text{model}}(\text{bits_per_wafer} - N). \quad (28)$$

For each bit with a defect, the chance of failure is determined with an electronic coin flip with the chance of failure being u^{model} . For each bit without a defect, the chance of failure is determined with an electronic coin flip with the chance of failure being b^{model} . Next, KR_i^{perfect} , which represents the kill ratio with perfect knowledge (i.e., the exact bit each defect sits upon is known), is calculated using (8) and a t of 0, which is equivalent to (1).

The defect map is then shifted by an arbitrary amount to represent natural offset between an inspection tool data and the electrical wafer map. Finally, KR_i^{lit} and KR_i are calculated. This simulation was run 100 times to generate distributions for KR_i^{lit} , KR_i , and KR_i^{perfect} including both the mean and the standard error. The mean and standard error values for KR_i^{lit} , KR_i , and KR_i^{perfect} are listed in Table II for different values of E and N . The percent differences between KR_i^{lit} and KR_i^{perfect} and KR_i and KR_i^{perfect} are also listed.

The average difference between KR_i^{perfect} and KR_i^{model} is very small, indicating a sufficiently large sample size to evaluate the estimators was used in the simulation. The standard errors for KR_i^{lit} , KR_i , and KR_i^{perfect} are very similar for each case and measure the natural variation in the number of killer defects per lot.

TABLE II
SIMULATION RESULTS. A TOLERANCE OF 160 μm WAS USED FOR ALL CASES. VALUES FOR N AND E ARE NORMALIZED TO COUNTS PER WAFER

\bar{N}	\bar{E}	KR_i^{model}	KR_i^{perfect}	SE	KR_i^{lit}	SE	KR_i	SE	KR_i^{lit} - KR_i^{perfect}	KR_i - KR_i^{perfect}
3000	1200	0	0.0000	0.0000	0.00325	0.0002	0.00004	0.0001	0.325%	0.004%
3000	1200	0.1	0.1000	0.0011	0.10249	0.0011	0.10023	0.0011	0.245%	0.019%
3000	1200	0.2	0.1999	0.0015	0.20153	0.0014	0.20020	0.0014	0.165%	0.031%
6000	2400	0	0.0000	0.0000	0.00649	0.0002	0.00002	0.0001	0.649%	0.002%
6000	2400	0.1	0.0998	0.0007	0.10470	0.0007	0.10018	0.0007	0.487%	0.035%
6000	2400	0.2	0.1999	0.0012	0.20317	0.0011	0.20050	0.0012	0.323%	0.055%
mean									0.366%	0.024%

The average difference between each of the estimators and KR_i^{perfect} is included on the bottom of the table. The average difference between KR_i^{lit} and KR_i^{perfect} is over ten times greater than the average difference between KR_i and KR_i^{perfect} , indicating that KR_i is much more accurate than KR_i^{lit} . The error in KR_i^{lit} is consistent with the values predicted in cases 13–19 of Table I and by (22). The observed error in KR_i^{lit} appears proportional to E and decreases as KR_i^{model} increases, also consistent with the previous results.

VI. OTHER FACTORS

In this section, some of the complicating factors that were temporarily set aside during the development of KR_i will be briefly discussed. A detailed discussion of these factors is beyond the scope of this paper.

In reality, many different classes of electrical failures commonly occur in addition to single bit failures, including column, row, cross, and double bit failures. For the purpose of overlay analysis, these failures should be considered a single failure since they are usually due to a single defect.

Clustering is prevalent in both cosmetic and electrical defect data and will affect the results of the kill ratio estimators discussed in this paper. Simulated experiments to quantify the impact of clustering on these estimators would be an interesting extension to this work. Neither KR_i nor KR_i^{lit} was designed to take advantage of clustering when present. Through these experiments potentially a modification to KR_i could be identified which would take advantage of the presence of clustering.

For now, when KR_i is used, we recommend treating clusters of defects as single defects. In some cases, unrelated defects that are within t of each other will both cause electrical failures. By clustering these defects, KR_i will be lower than it should be. In the case where two unrelated defects are within t of each other but do not cause electrical failures, KR_i will be higher than it should be. If numerous clusters occur, they should be investigated and the method of handling them should be based on this investigation. If numerous clusters occur due to very high defect densities, more accurate values for u and b could be generated by actually calculating the regions, A , \bar{A} , hit_area , and area_for_a_hit to take into account the overlap between events. This route is much more computationally intensive.

VII. CONCLUSION

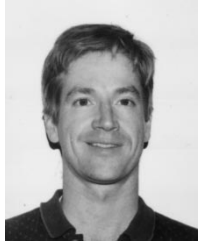
A new estimator for the kill ratio KR_i , which is appropriate for bitmap data, was introduced. The improvement in accuracy this estimator provides over the existing estimator KR_i^{lit} was demonstrated. The existing estimator becomes less accurate as t and the electrical defect density increase. At the same time, the number of falsely attributed electrical failures increases with t and the physical defect density. The estimator KR_i^{lit} will typically error on the high side because the estimate for b^{lit} does not take into account t . This error is approximately equal to the total area within t of any electrical failure divided by the total inspected wafer area. Equations are provided to approximate these errors for particular values of t , E , and total area when KR_i^{model} is 0. These serve as an upper bound for all values of KR_i^{model} , since when KR_i^{model} is nonzero, the error will be less. This paper demonstrates that small errors in KR_i^{lit} can have a major impact on the yield loss pareto. The total number of falsely attributed electrical failures is the sum of the error components over all defect types and inspection levels. For instance, in the extreme example presented, 38% of the defects were erroneously attributed. Therefore, t and N should be kept to reasonable sizes, and KR_i should be used instead of KR_i^{lit} for bitmap data.

ACKNOWLEDGMENT

The authors would like to thank K. Berstein, T. Karpowicz, L. LaBua, and R. Campbell of KLA-Tencor for their assistance in the experimental work which triggered some of these ideas.

REFERENCES

- [1] A. Fernandez, A. Lorenzo, S. Cruceta, and D. Oter, "A mathematical model for defect impact based on in-line vs test data correlations," in *Proc. ASMC*, 1999, pp. 92–96.
- [2] S. W. Hall, "Analysis of defectivity of semiconductor wafers by contingency table," in *Proc. Inst. Environmental Sciences*, 1994, pp. 177–183.
- [3] P. Mullenix, J. Zalniski, and A. J. Kasten, "Limited yield estimation for visual defect sources," *IEEE Trans. Semiconduct. Manuf.*, vol. 10, pp. 17–23, Feb. 1997.
- [4] R. Ott, H. Ollendorf, H. Lammering, T. Hladschik, and W. Haensch, "An effective method to estimate defect limited yield impact on memory devices," in *Proc. ASMC*, 1999, pp. 87–91.
- [5] T. Henry, "Use of a short loop zone tester for baseline D0 improvement in the metal 1 zone," in *Yield Management Solutions Sem. Proc.*: KLA Tencor, July 1998.
- [6] KLA-Tencor, *BitPower Analysis System User Manual*, 2.1 ed., 1999.
- [7] M. Merino, "SmartBit: Bitmap to defect correlation software for yield improvement," in *Proc. ASMC*, 2000.
- [8] KLA-Tencor, *Klarity Operations Manual*, 1.1 beta ed., 1999.



Oliver D. Patterson (S'94–M'98) received the S.B. degree from the Massachusetts Institute of Technology, Cambridge, in 1985, the M.S. degree from the University of Wisconsin, Madison, in 1987, and the Ph.D. degree from the University of Michigan, Ann Arbor, in 1998, all in electrical engineering.

He is a member of the defect reduction engineering group at Agere Systems in Orlando, FL. He both develops software tools and methodologies for yield improvement and applies these tools to the many technologies produced at Agere Systems. His current research interests include the development of methods for using an inspection SEM for in-line detection of yield limiting defects; he played a key role in the development of KLA-Tencor's μ Loop methodology. He also is active in yield modeling using critical area analysis.

Mark H. Hansen received the Ph.D. degree in statistics from the University of California, Berkeley, in 1994.

He is a Member of the Technical Staff, Statistics and Data Mining Research Department, Bell Laboratories. His research interests include methods for data-rich applications, especially those arising in telecommunications networks. His work is interdisciplinary, finding inspiration in analysis, signal processing, and information theory.

Dr. Hansen is an Associate Editor for the *Journal of the Statistical Association* and is currently Chair of Computing Section of the American Statistical Association.