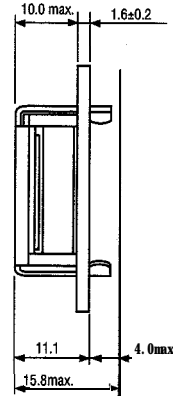| L1682B1J000	L1642B1J000	2x16	STN	80.0x36.0x15.8	35	64.5x13.8	2.95 x 3.80	0.50 x 0.55	0.05	420
L1682B1P000	L1642B1L000	2x16	WTSTN	80.0x36.0x15.8	35	64.5x13.8	2.95 x 3.80	0.50 x 0.55	0.05	420

L1682 (2x16) Unit: mm General Tolerance f0.5 mm

Reflective/EL Backlight   LED Backlight
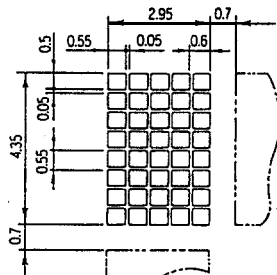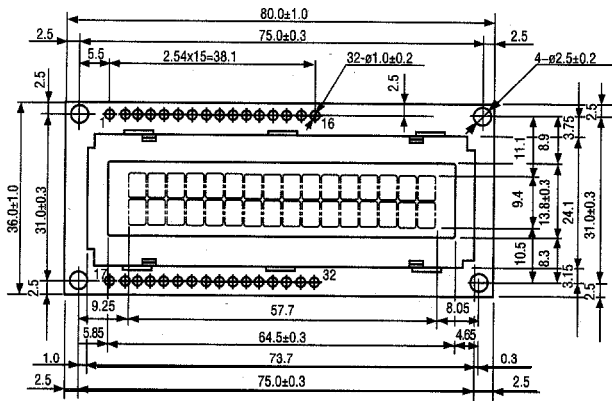
*LED Powered through pins 15 & 16 or 31 & 32
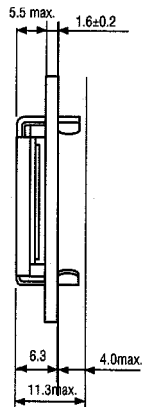
No.	No.	Name	Function
1	17	V_{SS}	GND
2	18	V_{DD}	Power supply voltage + 5 V
3	19	V_{LC}	Liquid crystal driving voltage
4	20	RS	L: Instruction code input. H: Data input
5	21	R/W	L: Data write from MPU to LCM. H: Data read from LCM to MPU
6	22	E	Enable
7	23	DB0	Data bus line
8	24	DB1	Data bus line
9	25	DB2	Data bus line
10	26	DB3	Data bus line
11	27	DB4	Data bus line
12	28	DB5	Data bus line
13	29	DB6	Data bus line
14	30	DB7	Data bus line
15	31	V_A*	Anode
16	32	V_K*	Cathode

PIN FUNCTIONS

OPTIMUM VIEWING ANGLE / CONTRAST ADJUSTMENT CIRCUIT

All Supertwist Character Modules Except
L1681 & L1692 Series

+55°

+15°

-15°

-55°

6 O'CLOCK

12 O'CLOCK
(Optional)
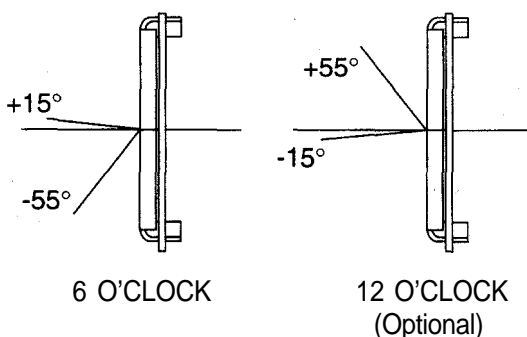
L1681 & L1692
Series (only)

+35°

-35°
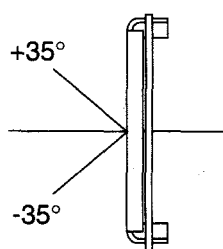
Side Viewing Angles on
Supertwist Character Modules

40°   40°

STANDARD STN & 12022

V_{DD}

V_{LC} 1K-10K

V_{SS}

(+5V)

(+)

(-)

(OV)

WIDE TEMPERATURE STN

V_{DD}

$* V_{LC}$ 10K

V_{SS}

1K

(+5V)

(+)

(-)

(OV)

(+)

(-)

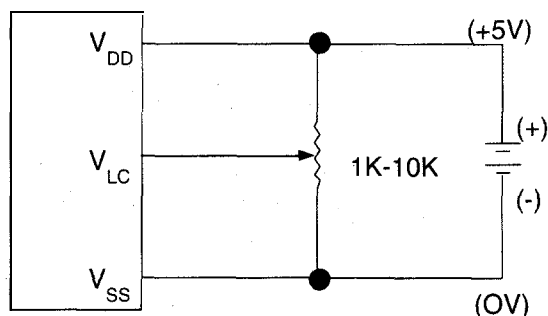(-5V)

• V_{LC} should not exceed -2V.
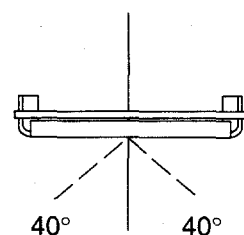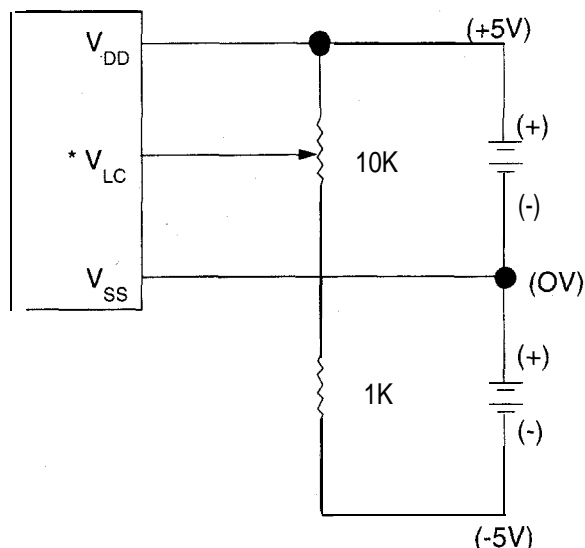
▶ The above schematic applies to all **Seiko Instruments** standard temperature supertwist character modules except L2022. A variable or fixed resistor must be used on any LCD module as it appears in the above schematic.

▶ A variable resistor is advisable, especially for stationary equipment. The variable resistor allows the user to adjust the voltage, to get maximum contrast in relationship to whatever angle the user is viewing the LCD (within the optimum viewing range). A variable also allows the user to adjust the voltage for any temperature fluctuations between 0" and 50°C.

▶ A fixed resistor limits the LCD to a finite voltage and therefore a very limited viewing angle. Fixed resistors should be used in those applications where the display can be adjusted to the particular user (i.e., hand-held products).

▶ The above schematic applies to all **Seiko Instruments** supertwist character modules with Wide Temperature Fluid. A variable or fixed resistor must be used on any LCD module as it appears in the above schematic.

▶ A variable resistor is advisable, especially for stationary equipment. The variable resistor allows the user to adjust the voltage, to get maximum contrast in relationship to whatever angle the user is viewing the LCD (within the optimum viewing range). A variable also allows the user to adjust the voltage for any temperature fluctuations between -20° and 70%.

▶ A fixed resistor limits the LCD to a finite voltage and therefore a very limited viewing angle. Fixed resistors should be used in those applications where the display can be adjusted to the particular user (i.e., hand-held products).

OPERATING INSTRUCTIONS

INTRODUCTION

Seiko Instruments intelligent dot matrix liquid crystal display modules have on-board controller and LSI drivers, which display alpha numerics, Japanese KATA KANA characters and a wide variety of other symbols in either 5 x 7 dot matrix.

The internal operation in the KS0006 controller chip is determined by signals sent from the MPU. The signals include: 1) Register select RS input consisting of instruction register (IR) when RS = 0 and data register (DR) when RS = 1; 2) Read/write (R/W); 3) Data bus (DB7~ DBO); and 4) Enable strobe (E) depending on the MPU or through an external parallel I/O port. Details on instructions data entry, execution times, etc. are explained in the following sections.

READ AND WRITE TIMING DIAGRAMS AND TABLES

The following timing characteristics are applicable for all of Seiko's LCD dot matrix character modules.

READ TIMING CHARACTERISTICS
$V_{DD}=5.0V\pm5\%$, $V_{SS}=OV$, $T_A=0^\circ C$ TO $50^\circ C$

item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W—E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	—	160	ns
Data hold time	t_H	5	—	ns

WRITE TIMING CHARACTERISTICS
$V_{DD}=5.0V\pm5\%$, $V_{SS}=OV$, $T_A=0^\circ C$ TO $50^\circ C$

Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W-E	t_{AS}	140		— ns.
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	80	—	ns
Data hold time	t_H	10	—	ns

READ OPERATION
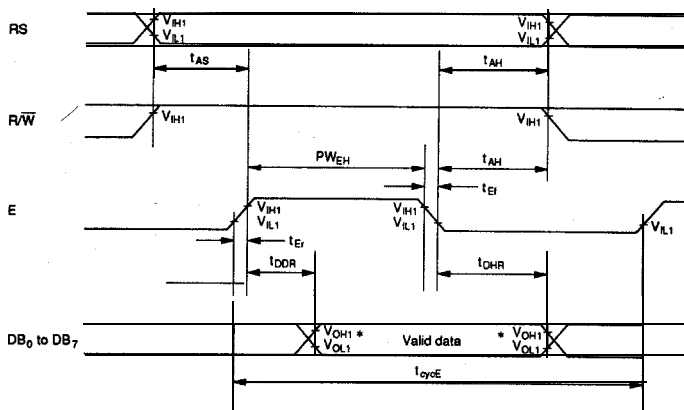
Note: • VOLI is assumed to be 0.8 V at 2 MHz operation.

DATA READ FROM MODULE TO MPU

WRITE OPERATION

DATA WRITE FROM MPU TO MODULE

INSTRUCTION CODES

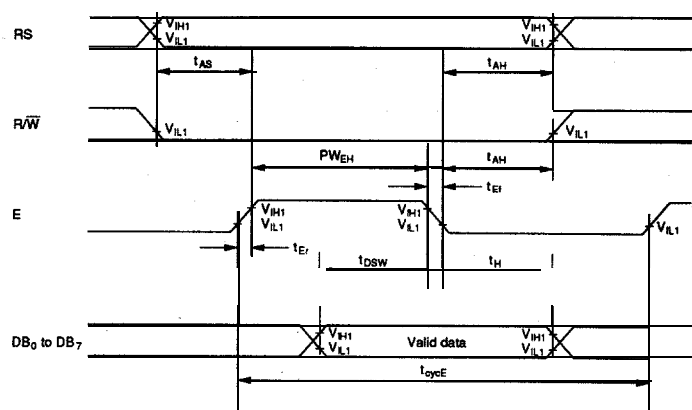| Instruction	Set RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (when f_{cp} or f_{osc} is 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μs - 1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μs ~ 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font(F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or to DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs

* Doesn't matter

DD RAM:	Display data RAM	I/D = 1: increment	C=1: Cursor ON	R/L=1: Right shift
CG RAM:	Character generator RAM	I/D = 0: Decrement	c = 0: Cursor OFF	R/L = 0: Left shift
A_{CG}:	CG RAM address	S=1: Display shift	B = I: Blink ON	DL = I: 6 bits
A_{DD}:	DD RAM address corresponds to cursor address	S=0: No display shift	B=O: Blink OFF	DL=O: 4 bits
AC:	Address counter used for both DD RAM and CG RAM address	D - I: Display ON D = 0: Display OFF S/C = 1: Display shift S/C = 0: Cursor movement	BF=1: Internal operation in progress BF=0: instruction can be accepted	N=1: 2 lines (L1671) F = 0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{osc} is 270 kHz: 40μs x 250/250 = 37μs

INSTRUCTION CODE EXPLANATIONS

The two registers 1) Instruction Register (IR) and the 2) Data Register (DR) in the KS0066 controller chip are directly controlled by the MPU. Control information is temporarily stored in these registers prior to internal operation start. This allows interface to various types of MPUs which operate at different speeds from that of the KS0066, and allows interface from peripheral control ICs. Internal operations of the KS0066 are determined from the signals sent from the MPU. These signals, including register selection signals (RS), Read/Write (R/W) and data bus signals (DBO - DB7) are polled instructions.

REGISTER SELECTION		
RS	**R/W**	**Operation**
0	**0**	IR selection, IR write. Internal operation: Display clear
0	1	**Busy** flag (DB7) and address counter (DBO to DB6) read
1	0	DR selection, DR write. Internal operation: DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation: DD RAM or CG RAM to DR

ADDRESS COUNTER (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DBO to DB6; refer to above "Register Selection Table" when RS = 0 and R/W= 1.

CLEAR DISPLAY

	RS	R/W	D B 7						DBO
Code	0	0	0	0	0	0	0	0	0	1

Clear all display memory and return the cursor to the home position. In other words, the cursor returns to the first character block on the first line on all 1, 2, and 4 line character modules except L4044. If the above is entered on E2 (the second controller for lines 3 and 4), the cursor will return to the first character on the third line.

CURSOR HOME

	RS	R/W	D B 7							DBO
Code	0	0	0	0	0	0	0	0	1	*

*Doesn't matter

Returns cursor to home position. First line first character blocks on all 1, 2 and 4 line display; except L4044 refer "clear display": (Address 0; A,, "80"). The contents of DD RAM remain unchanged.

RESTRICTIONS ON EXECUTION OF DISPLAY CLEAR AND CURSOR HOME INSTRUCTIONS	
Conditions of use	**Restrictions**
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction).	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. • L4052: f_{osc} = 250 kHz • The other modules: f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction.	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

	RS	R/W	DB7						I/D	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one block when writing or reading a character code from DD RAM or CG RAM. The cursor automatically moves to the right when incremented by one or to the left if decremented by one.

S: Shifts the entire display to either the right or left when S = 1 (high). When S = 1 and I/D = 1 the display shifts one position to the left. When S = 1 and I/D = 0 the display shifts one position to the right. This right or left shift occurs after each data write to DD RAM. Display is not shifted when reading from DD RAM. Display is not shifted when S = 0.

DISPLAY AND CURSOR ON/OFF CONTROL

	RS	R/W	DB7						DC	DB0
Code	0	0	0	0	0	0	1	DC	B	

D: Display is turned ON when D = 1 and OFF when D = 0. When display is OFF, display data in DD RAM remains unchanged. Information comes back immediately when D = 1 is entered.

C: Cursor is displayed when C = 1 and not displayed when C = 0. If the cursor disappears, function of I/D etc.

does not change during display data write. In a 5 x 7 dot matrix there is an eighth line which functions as the cursor.

B: When B = 1, the character at the cursor position starts blinking. When B = 0 the cursor does not blink. The blink is done by stiching between the all black dot matrix and displayed character at 0.4 second intervals. The cursor and the blink can be set at the same time (fosc = 250 kHz).

5 X 7 DOT MATRIX
C = 1 (cursor display)   B = 1 (blinking)
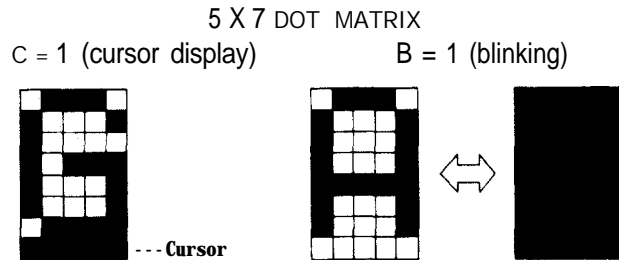
--- Cursor

	RS	R/W	DB7					S/C	R/L	DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Doesn't Matter

Cursor/Display Shift moves the cursor or shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. In case of a 2-line display, the

cursor is shifted from character block 40 of line 1 to character block 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. In case of a 4-line display, the cursor does not move continuously from line 2 to line 3. The cursor is shifted from character block 40 of line 3 to character block 1 of line 4. Displays of lines 3 and 4 are shifted at the same time. The display pattern of line 2 or 4 is not shifted to line 1 or 3.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

FUNCTION SET

	RS	R/W	DB7							DB0
Code	0	0	0	0	1	DL	N	F	*	*

* Doesn't Matter

Function Set sets the interface data length, the number of display lines and the character font.

DL: Interface data length

When DL = 1, the data length is set at 8 bits (DB7 to DB0).

When DL = 0, the data length is set at 4 bits (DB7 to DB4).

The upper 4 bits are transferred first, then the lower 4 bits follow.

N: Number of display lines
F: Sets character font

1	0	2	5 x 7 dot matrix	I/16	L1671, L1681, L1672, L1682 L1692, L1634, L2032, L2022 L2034, L2462, L4052, L4044

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

CG RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit   Lower bit →

CG RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit   Lower bit →

DD RAM addresses expressed as binary AAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU.

BUSY FLAG/ADDRESS READ

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit   Lower bit →

The BF signal can be read to verify if the controller is indicating that the module is working on a current instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

DATA WRITE TO CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	0	D	D	D	.D	D	D	D	D

← Upper bit   Lower bit →

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

DATA READ FROM CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

← Upper bit   Lower bit →

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. In addition, either instruction is executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note: The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

5 x 7 + CURSOR

Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data), (5 x 7 dot matrix).

Character code (DD RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	CG RAM address 5 4 3 2 10 ←Upper bit Lower bit+	Character pattern (CG RAM data) 7 6 5 4 3 2 1 0 -Upper bit Lower bit→	
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0 0 1 0 10 0 11 1 0 0 1 0 1 11 0 1 1 1	* * * 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * 0 0 0 0 0	Example of character pattern (R)
			← Cursor position
0 0 0 0 * 0 0 1	0 0 1 0 0 0 0 0 1 0 10 0 11 1 0 0 1 0 1 11 0 1 1 1	* * * 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * 0 0 0 0 0	Example of character pattern (Y)
0 0 0 0 * 1 1 1	1 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * * * * * * *	

NOTES: ▶ In CG RAM data, **1** corresponds to Selection and 0 to Non-selection on the display.

▶ Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).

▶ CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is charged to 1, one bit lights, regardless of the cursor.

▶ The character pattern column position corresponds to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

▶ When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

PROGRAMMING THE CHARACTER GENERATOR RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to create up to eight custom 5 x 7 characters + cursor (5 x 8). Once programmed, the custom characters or symbols are accessed exactly as if they were in ROM. However since the RAM is a volatile memory, power must be continually maintained. Otherwise, the custom characters/symbols must be programmed into non-volatile external ROM and sent to the display after each display initialization. All dots in the 5 x 8 dot matrix can be programmed, which includes the cursor position.

The modules RAM are divided into two parts: data display RAM (DD RAM) and custom character generator RAM (CG RAM). This is not to be confused programming the custom character generator RAM with the 192 character generator ROM. The CG RAM is located between hex 40 and 7F and is contiguous. Locations 40 thru 47 hold the first custom character (5 x 8), 48 thru 4F hold the second custom character, 50 thru 57 hold the third CG, and so forth to 78 thru 7F for the eighth CG character/symbol.

If during initialization the display was programmed to automatically increment, then only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the completed character is formed. All eight custom CG characters can be programmed in 64 consecutive "writes" after sending the single initial 40 address.

The CG RAM is 8 bits wide, although only the right-most 5-bits are used for a custom CG character row. The left-most dot of programming the CG RAM character corresponds to D4 in the most significant nibble (XXXD4) of the data bus code, with the remaining 4 dots in the row corresponding to the least significant nibble (D3 thru DO), DO being the right-most dot. Thus, hex 1 F equals all dots on and hex 00 equals all dots off. Examples include hex 15 (10101) equal to 3 dots on the hex OA (01010) equal 2 dots on. In each case the key 5-bits of the 8-bit code program one row of a custom CG character. When all 7 or 8 rows are programmed, the character is complete. A graphic example is shown below:

RS	R/W	Data	Display	Description
0	0	40	—	addresses 1st row, 1st CG character
1	0	11	* *	result of 11, 1 st row
1	0	OA	**	result of OA, 2nd row
1	0	1F	*****	result of 1 F, 3rd row
1	0	04	*	result of 04, 4th row
1	0	1F	*****	result of 1 F, 5th row
1	0	04	*	result of 04, 6th row
1	**0**	04	*	result of 04, 7th row
1	0	00	—	result of 00, 8th row (cursor position)
1	0	15	***	1st row, 2nd CG character. **Note:** Addressing not now required; hex 48 is next in the sequence.

2) L1672-Series (16 characters x 2 lines)
   L1682-Series
   L1692-Series

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF