Diode Problem:

Using ideal model,

Using large signal model,

Using small-signal model,
Diode is always reverse biased. At least 2 V with polarity shown is maintained over diode and resistor.

Assume capacitor discharged. Initially, when input is 1 V, diode is reverse biased. With this open circuit, capacitor will not charge or discharge. $V_{out} = V_c + 1$.

When input is $-1$ V, diode will be forward biased. Capacitor will charge.

Ideal model - forward bias

Large signal model - forward bias

Capacitor charges to 1 V quickly. Capacitor charges to 0.3 V.
Small-signal model forward bias

Capacitor will charge to 0.4 V quickly
\[ T = 2 \text{ ns} \]

Because of initial gap voltage

Ideal

Steady State. Flipped upside down for next circuit.
Create a truth table for the following circuit:

\[ A = 0 \]
\[ B = 0 \]

\[ F = 0 \]
Create a truth table for the following circuit:

\[ A = 0 \]
\[ B = 1 \]
\[ F = 1 \]
Create a truth table for the following circuit:

A = 1
B = 0
F = 1
Create a truth table for the following circuit:

A = 1
B = 1

F = 1

Conclude: OR gate
Guessing modes:

Transistor ② is cutoff: \( V_{GS} = 0 \) \( \rightarrow \) No current \( I_D \).

Transistor ④ has \( V_{GS} = V_T + \varepsilon \), so \( I_D/\overline{VDS} \) curve is shallow \( \Rightarrow \) low \( I_{D4} \) in saturation mode.

Transistor ① has \( V_{GS1} = -V_{DD} + V_T + \varepsilon \), so \( I_D/\overline{VDS} \) curve is steep, with low \( I_D \) from transistor ④,

\[ \Rightarrow \overline{VDS1} \text{ is small and transistor in triode} \]

Transistor ③ has \( V_{GS3} > \overline{VDS3} \).

\( \overline{VDS3} \) must be small, otherwise \( \overline{VDS3} + \overline{VGS3} \) substantial

\[ \Rightarrow \text{substantial } \overline{VDS} \]

\( \overline{VDS3} \) small \( \& \) \( \overline{VDS1} \) small \( \Rightarrow \overline{VDS4} \) large \( \Rightarrow \overline{VGS3} \) small

So "probably" transistor ③ in saturation (shallow curve).
Transistor ② is cutoff, no $I_D$.

Transistor ① has $V_{GS} = -V_T - \varepsilon$, so $I_D$/$V_{DS}$ curve is shallow $\Rightarrow$ low $I_{D1}$, likely saturation.

Transistor ④ has $V_{GS} = V_{DD} - V_T - \varepsilon$, so $I_D$/$V_{DS}$ curve is steep, with low $I_{D4} = I_{D1}$

$\Rightarrow$ $V_{DS4}$ small and triode mode.

Transistor ③ has substantial $V_{GS3}$ since $V_{G3} = V_{DD}$ and $V_{S3} = V_{DS4}$ is small, steep $I_D$/$V_{DS}$ curve and small $I_{D3} = I_{D1} \Rightarrow$ triode mode.
2 Transistors:

\[ \begin{align*}
N\text{MOS} & \quad P\text{MOS} \\
\chi &= 0 & \chi &= 0 \\
V_T &= 1 & V_{TP} &= -1 \\
I_{DSATN} &= & I_{DSATP} = & \\
10^{-4}(V_{GS}-V_T)^2 & & 10^{-4}(V_{GS}-V_T)^2 & \\
\end{align*} \]

Relate \( I_{DP}, I_{DN}, V_{DSP}, V_{DSN} \) with KVL + KCL:

\[ 5 = V_{DSN} - V_{DSP} \quad I_{DN} + I_{DP} = 0 \]

Guess that N\text{MOS} is in saturation, P\text{MOS} in triode:

\[ I_{DN} = I_{DSATN}(1 + \chi V_{DSN}) = 10^{-4}(1.2 - 1)^2 = 4 \times 10^{-6} \]

\[ I_{DP} = \frac{2 I_{DSATP}}{(V_{GS} - V_{TP})^2} \left( V_{GS} - V_{TP} - \frac{V_{DSP}}{2} \right) V_{DSP} \]

\[ = 2 \times 10^{-4} \left( 1.2 - 5 - -1 - \frac{V_{DSP}}{2} \right) V_{DSP} \]

\[ = 2 \times 10^{-4} \left( 2.8 - \frac{V_{DSP}}{2} \right) V_{DSP} \]

Substitute \( I_{DP} = -I_{DN} \) and solve for \( V_{DSP} \):
\[-4 \times 10^{-4} = 2 \times 10^{-4} (2.8 - \frac{V_{DS_P}}{2}) V_{DS_P}\]

\[0 = -V_{DS_P}^2 + 5.6V_{DS_P} + 0.04\]

\[V_{DS_P} = -0.0071 \quad \text{or} \quad 5.6071\]

- \underline{agrees with triode}\n- \underline{impossible}\n
\[V_{DS_N} = 5 + V_{DS_P} = 4.993\, V\]

- \underline{agrees with Sat}
Transistor in linear circuit:

\[ V_T = 1.0 \text{ V} \]
\[ V_{GS} = 3 \text{ V} \]
\[ R = 2 \text{ M} \Omega \]
\[ 10 \text{ k}\Omega \]

\[ \chi = 0 \]

\[ I_{DSAT} = 10^{-4} (V_{GS} - V_T)^2 \]

By voltage division, \( V_{GS} = 4 \text{ V} \)

Write linear part:

KVL gives us \( 5 = I_D \cdot 10\text{k} + V_{DS} \)

Write transistor equation:

Guess a mode - saturation is easiest to solve

\[ I_D = I_{DSAT} (1 + \chi V_{DS}) \]
\[ = 10^{-4} (4 - 1)^2 (1 + 0 V_{DS}) = 9 \cdot 10^{-4} \]

Check to see if really in sat mode:

is \( V_{DS} > V_{GS} - V_T \) (true for sat mode)

\[ V_{DS} = 5 - 10\text{k} I_D = 5 - 10\text{k} \cdot 9 \cdot 10^{-4} = -4 \]

not sat mode.
So try triode mode (it should be right, since sat & cutoff are impossible):

\[ I_D = 2 IT_{DSAT} \frac{(V_{GS} - V_T - \frac{V_{DS}}{2})}{(V_{GS} - V_T)^2} V_{DS} \]

\[ = 2 \cdot 10^{-4} (4 - 1 - \frac{V_{DS}}{2}) V_{DS} \]

From linear equation, \( I_D = \frac{5 - V_{DS}}{10k} \)

\[ \frac{5 - V_{DS}}{10k} = 2 \cdot 10^{-4} (3 - \frac{V_{DS}}{2}) V_{DS} \]

\[ 0 = 2(3 - \frac{V_{DS}}{2}) V_{DS} - 5 + V_{DS} \]

\[ = -V_{DS}^2 + 7V_{DS} - 5 \]

\[ V_{DS} = 6.19 V \text{ or } 0.80 V \]

\[ \text{impossible!} \]

\[ V_{DS} = 0.90 V \text{ (confirms triode) } \]

\[ I_D = \frac{5 - V_{DS}}{10k} = 420 \mu V \]