Homework #1

Due Tuesday, September 10

Problem 1:

Create a truth table and draw a logical circuit (gates) for the following Boolean function:

$S_0 = A \bullet \overline{B} \bullet \overline{C} + \overline{A} \bullet \overline{B} \bullet C + \overline{A} \bullet B \bullet \overline{C} + A \bullet B \bullet C$

Problem 2:

Simplify the circuit from Problem 1 to use the minimum number of gates. You can use any of the gates from the class notes.

Problem 3:

Write a Boolean function in the variables A, B and C, and draw a logical circuit for the following truth table:

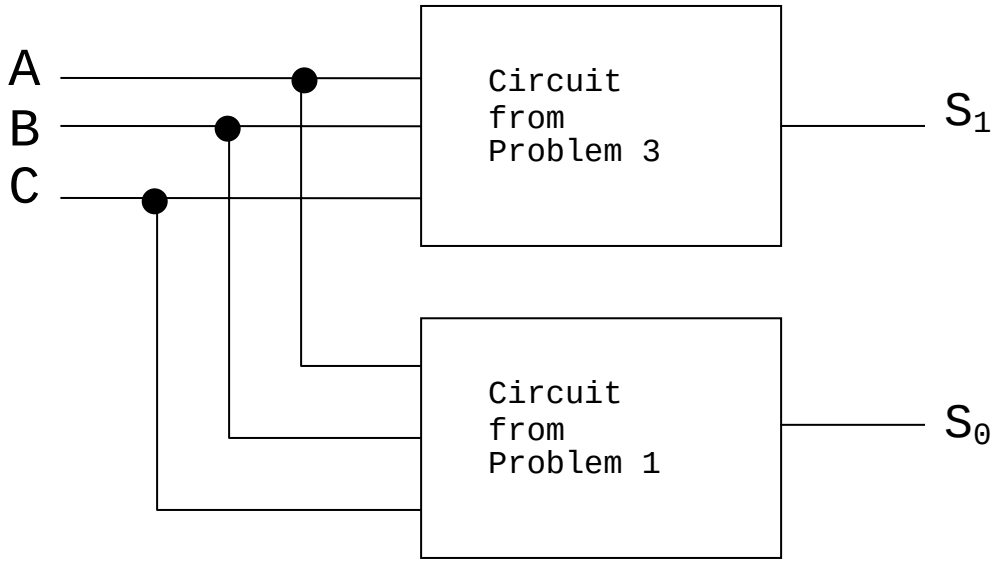
Inputs			Output
A	B	C	S_1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Problem 4:

Simplify the Boolean function from Problem 3 as much as possible.

Problem 5:

Combine the circuits from Problem 1 and Problem 3 as follows, to make a function with 3 inputs and two outputs:



Describe, *with one word*, what the above circuit does.

Problem 6:

Draw a timing diagram of the signal at the final output F of the following circuit. Assume each gate has a delay of T, and that A, B, and C have been at logic zero for a long time, until they are all turned on at time t = 0.