EE 40

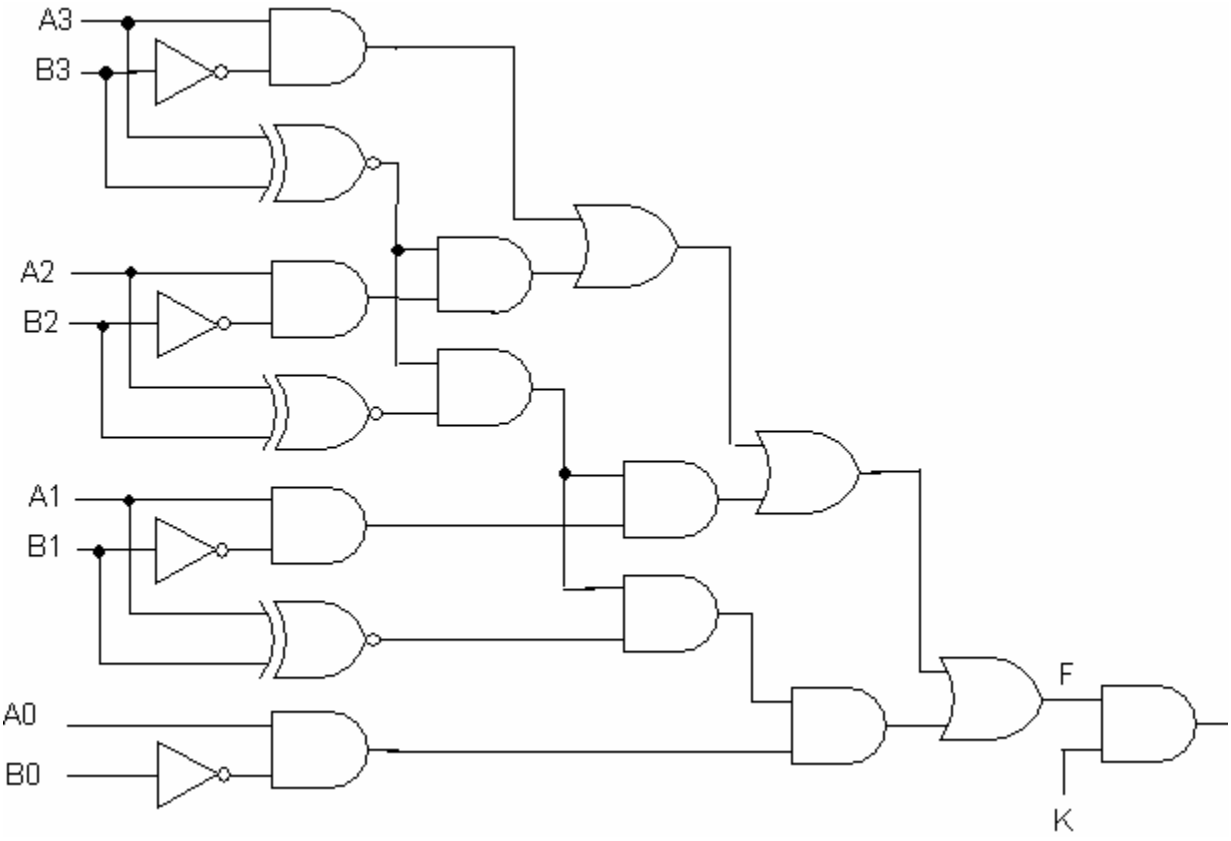
Homework #2

Due September 12, 2002

Problem 1:

An engineer with too much time on his/her hands has assembled the complicated circuit below using simple logic gates. Because the circuit contains paths with different propagation delays, false outputs may appear at the point F after the inputs are changed. Hence, the output F is ANDed with a clock signal K, which will be turned on to let F through only when enough time has passed for all signals to propagate through.

Each gate that this engineer used has a propagation delay of 20 ns. What is the corresponding maximum clock frequency?

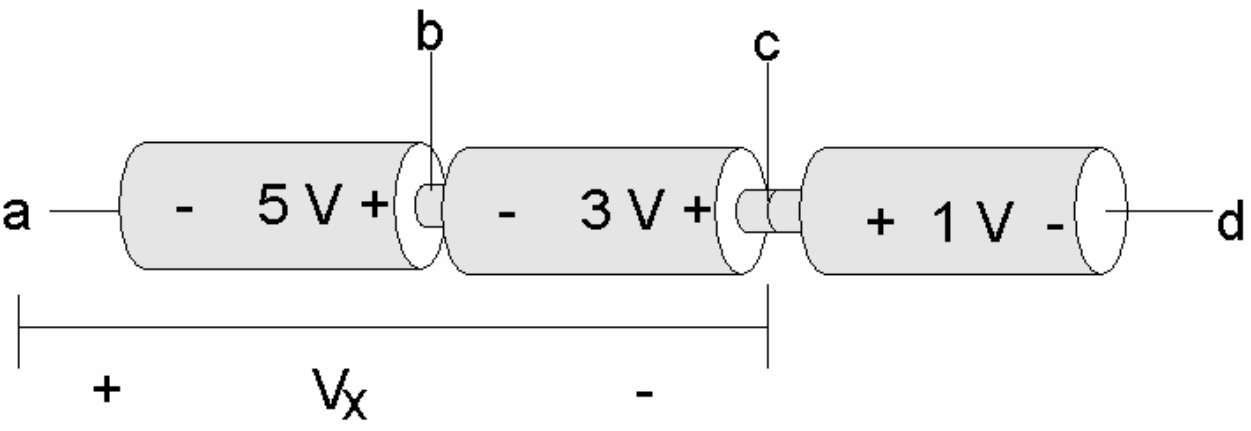


Problem 2:

The circuit above is a 4-bit magnitude comparator. It takes two 4-bit binary numbers, A and B, as input and outputs 1 if and only if A > B. Is there a different circuit which does this job faster? If so, what is the maximum clock frequency for the faster circuit?
Major Hint: Finding existing solutions is easier than creating new ones.

Problem 3:

Consider the following series of batteries:

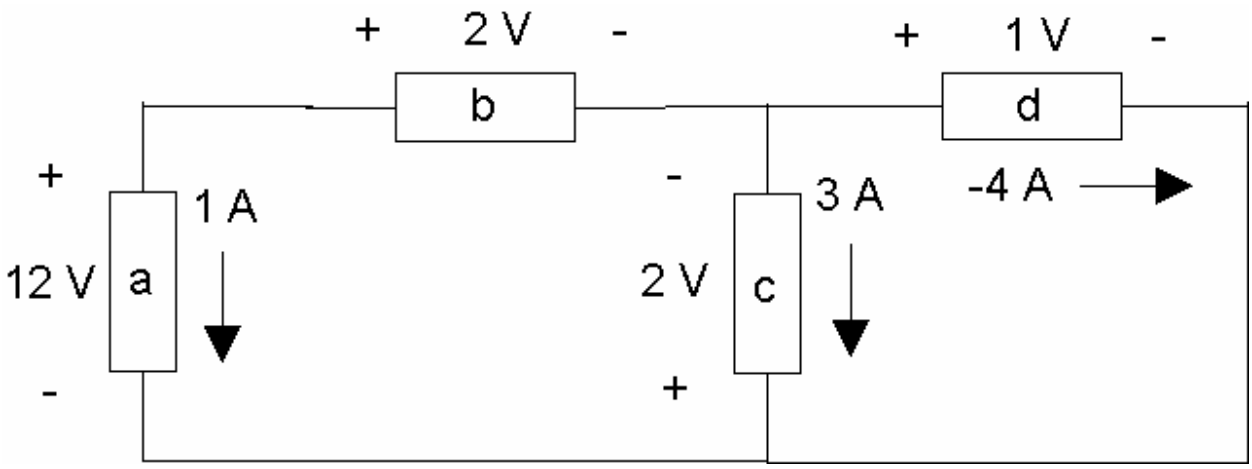


Find

i) V_{ad}
ii) V_{cb}
iii) V_x

Problem 4:

Consider the following circuit:



Find the power for each element, using the “associated reference directions” relationship between voltage and current (Lecture 4). State whether each element is absorbing or releasing power.