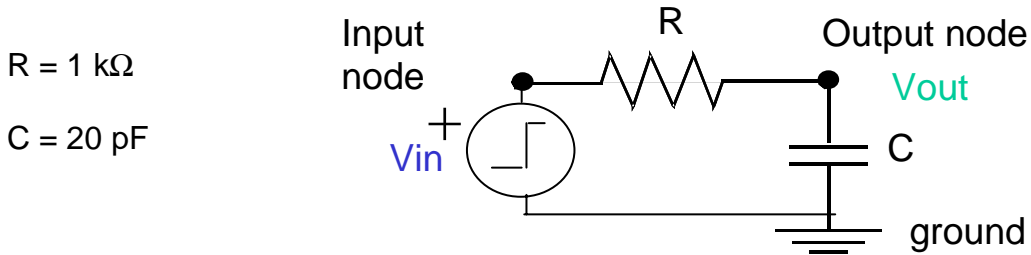


Homework #3

Due Thursday, September 19

Problem 1:

Consider the following circuit:



Assume that V_{in} has been at zero voltage for a long time, and rises immediately to 3 V at time $t = 0$.

- Sketch the output voltage V_{out} , over a time range of five time constants. Indicate the voltage level that V_{out} has reached after each time constant.
- Write the equation for V_{out} as a function of time, for $t \geq 0$.
- Write an equation for the power absorbed in the resistor R as a function of time.
- Find the total energy dissipated by the resistor over the entire duration of the transient period, from $t = 0$ to $t \rightarrow \infty$.

Problem 2:

Consider the same circuit from Problem 1, this time subjected to a pulse input voltage V_{in} , of duration 40 ns and amplitude 3 V, starting at $t = 0$ (V_{in} at 0 V for all $t < 0$).

- Sketch the output voltage V_{out} , over a time range of 100 ns. Indicate the peak voltage reached by V_{out} and the time at which the peak occurs.
- Write the equation for V_{out} as a function of time, for $t \geq 0$.

Problem 3:

Now suppose we are again working with the circuit from Problem 1, but we want to design a pulse long enough so that the output of our gate is at least V_{IH} . V_{IH} is the minimum recommended input voltage to be recognized as logic 1, so we are finding the minimum pulse length that sends the right message through to the next gate.

Suppose that the amplitude of the V_{in} pulse will be 3 V, and that $V_{in} = 0$ for all $t < 0$. The V_{IH} we want to reach is 2.1 V. How long should the pulse be?