EE 40

Homework #8

Due Friday, December 6, 2002 at 2 PM

Problem 1:

Consider the CMOS inverter circuit. Let V_M be the input voltage which makes V_{OUT} equal to V_{IN}. For this input voltage, both the PMOS and NMOS transistors will be in saturation mode.

Let λ equal zero for both transistors, so $I_D = I_{DSAT}$ for each transistor. With

$$I_{DSAT(N)} = \frac{W_N}{2L_N}\mu_N C_{ox}\left(V_{GS(N)} - V_{T(N)}\right)^2 \qquad I_{DSAT(P)} = -\frac{W_P}{2L_P}\mu_P C_{ox}\left(V_{GS(P)} - V_{T(P)}\right)^2$$

$V_{T(N)} = -V_{T(P)} = 1$ V | $C_{OX} = 5$ fF/μm^2 | $L_N = L_P = 1.5$ μm

$\mu_N = 500$ $cm^2/(Vs)$ | $\mu_p = 250$ $cm^2/(Vs)$ | $W_P = 10$ μm

find the value of W_N that will lead to $V_M = 1.5$ V.

Problem 2:

Suppose we have connected the output of CMOS inverter 1 to the input of CMOS inverter 2, where both of the inverters have the following characteristics:

$V_{T(N)} = -V_{T(P)} = 1$ V | $L_N = L_P = 2$ μm | $W_N = 6$ μm

$\mu_N = 500$ $cm^2/(Vs)$ | $\mu_p = 250$ $cm^2/(Vs)$ | $W_P = 12$ μm

$t_{OX} = 10$ nm (oxide thickness) | $k_{OX} = 4$ (oxide dielectric constant) | $V_{DD} = 5$ V

$L_I = 30$ μm (interconnect length) | $W_I = 1$ μm (interconnect width) | $C_{DB(P)} = C_{DB(N)} = 50$ fF

Find the propagation delay from the input of inverter 1 to the output of inverter 1 for a perfect high to low input transition.

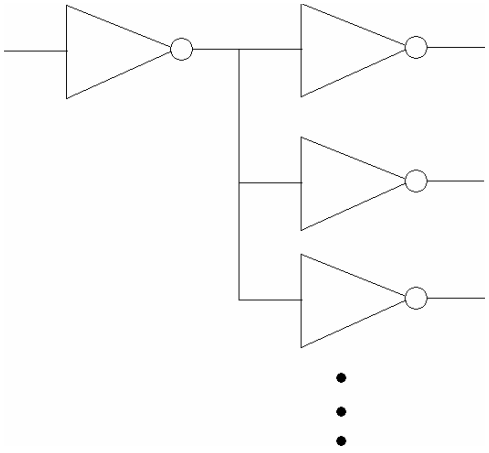
Use W_N, L_N, W_P, L_P as the channel dimensions (for calculating I_{DSAT}) as well as the gate dimensions (for calculating C_{GB}). Let λ equal zero for all transistors.

Problem 3:

Consider a CMOS inverter with

R_N = 3 kΩ $C_{DB(P)} = C_{DB(N)} = C_{GB(P)}$ = 50 fF

R_P = 2 kΩ $C_{GB(N)}$ = 75 fF

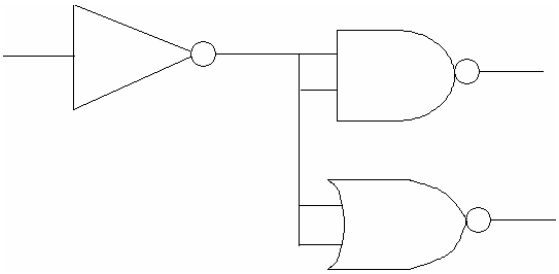


The output of this inverter is connected to the input of several other identical inverters, as shown at right.

Each inverter connected at the output adds an interconnect capacitance C_I of 100 fF.

Determine the number of inverters that can be connected (the "fan-out") if the propagation delay from the input to output of the first inverter may not exceed 20 ns.

Problem 4:



Consider a CMOS inverter with output connected to both inputs of a NAND gate and both inputs of a NOR gate as shown.

Using the resistance and capacitance values given in Problem 3 for the transistors, determine the propagation delay from the inverter input to inverter output for both low to high and high to low (perfect) input transitions.