EE 40

Homework #8 Solutions and Grading

For each problem, deduct 5 points for each "reasonable" error. If the solution method is completely wrong, award 0 points (the minimum score for each problem).

Problem 1 Answer: 25 Total Points

When $V_{IN} = 1.5$ V, $V_{OUT} = 1.5$ V.

$V_{GS(N)} = V_{IN} = 1.5$ V

$V_{DS(N)} = V_{OUT} = 1.5$ V

$V_{GS(P)} = V_{IN} - V_{DD} = 1.5$ V – 5 V = -3.5 V

$V_{DS(P)} = V_{OUT} - V_{DD} = 1.5$ V – 5 V = -3.5 V

$I_{D(N)} + I_{D(P)} = 0 \quad \Rightarrow \quad I_{D(N)} = -I_{D(P)}$

Both transistors are in saturation, so $I_D = I_{DSAT}$ for each transistor. Substitute into $I_{D(N)} = -I_{D(P)}$:

$$I_{DSAT(N)} = -I_{DSAT(P)} = \frac{W_N}{2L_N}\mu_N C_{ox}\left(V_{GS(N)} - V_{T(N)}\right)^2 = \frac{W_P}{2L_P}\mu_P C_{ox}\left(V_{GS(P)} - V_{T(P)}\right)^2$$

$$\frac{W_N}{2x1.5x10^{-6}m}500x10^{-4}m^2/(Vs)\frac{5x10^{-15}F}{10^{-12}m^2}(1.5\text{ V} - 1\text{ V})^2$$

$$= \frac{10x10^{-6}}{2x1.5x10^{-6}m}250x10^{-4}m^2/(Vs)\frac{5x10^{-15}F}{10^{-12}m^2}(-3.5\text{ V} - -1\text{ V})^2$$

$W_N = 125\ \mu m$

Problem 2 Answer: 25 Total Points

Propagation delay from high to low involves R_{P1}, $C_{DB(N1)}$, $C_{DB(P1)}$, $C_{GB(N2)}$, $C_{GB(P2)}$, and C_l.

To find R_{P1}, take the average of $V_{DS(P1)}/I_{D(P1)}$ when $V_{DS(P1)}$ is at full voltage and when it has transitioned halfway. That is:

$$R_{P1} = \frac{1}{2}\left(\frac{-V_{DD}}{I_{DSAT(P1)}} + \frac{-V_{DD}/2}{I_{DSAT(P1)}}\right) = .\frac{-0.75V_{DD}}{-\frac{W_{P1}}{2L_{P1}}\mu_{P1}\frac{k_{ox}\varepsilon_0}{t_{ox}}\left(V_{GS(P1)} - V_{T(P1)}\right)^2}$$

$$= \frac{-0.75x5\text{ V}}{-\frac{12x10^{-6}m}{2x2x10^{-6}m}250x10^{-4}m^2/(Vs)\frac{4x8.85x10^{-12}F/m}{10x10^{-9}m}(-5\text{ V} - (-1\text{ V}))^2} = 883\ \Omega$$

Note that we do the calculation for $V_{GS(P1)}$ *after* the transition has taken place, so:

$V_{GS(P1)} = V_{IN} - V_{DD} = 0 - 5$ V = -5 V

Compute $C_{GB(P2)}$ and $C_{GB(N2)}$ using parallel place capacitance:

$$C_{GB(P2)} = \frac{k_{ox}\varepsilon_0}{t_{ox}} W_P L_P = \frac{4x8.85x10^{-12} F/m}{10x10^{-9} m}(12x10^{-6} m)(2x10^{-6} m) = 85 \text{ fF}$$

$$C_{GB(N2)} = \frac{k_{ox}\varepsilon_0}{t_{ox}} W_N L_N = \frac{4x8.85x10^{-12} F/m}{10x10^{-9} m}(6x10^{-6} m)(2x10^{-6} m) = 42.5 \text{ fF}$$

Compute C_I using parallel plate capacitance:

$$C_I = \frac{k_{ox}\varepsilon_0}{t_{ox}} W_I L_I = \frac{4x8.85x10^{-12} F/m}{10x10^{-9} m}(30x10^{-6} m)(1x10^{-6} m) = 106 \text{ fF}$$

With $C_{DB(P1)} = C_{DB(N1)} =$ 50 fF, we can now compute the time constant (all the capacitances are in parallel):

$\tau = R_{P1}(C_{DB(P1)} + C_{DB(N1)} + C_{GB(P2)} + C_{GB(N2)} + C_I) = 883\ \Omega\ (50 + 50 + 85 + 42.5 + 106)$ fF = 295 ps

The propagation delay is 0.69 τ : **t_p = 207 ps**

<u>Problem 3 Answer</u>: 25 Total Points

Low to high transition:

$t_p = 0.69\ \tau = 0.69\ R_{N1}[C_{DB(P1)} + C_{DB(N1)} + n(C_{GB(P2)} + C_{GB(N2)} + C_I)] \leq 20$ ns

$0.69 \times 3000\ \Omega\ [50 + 50 + n(50 + 75 + 100)]$ fF ≤ 20 ns

$n \leq 42$

High to low transition:

$t_p = 0.69\ \tau = 0.69\ R_{P1}[C_{DB(P1)} + C_{DB(N1)} + n(C_{GB(P2)} + C_{GB(N2)} + C_I)] \leq 20$ ns

$0.69 \times 2000\ \Omega\ [50 + 50 + n(50 + 75 + 100)]$ fF ≤ 20 ns

$n \leq 63$

Conclusion: Fan-out is **42 gates**.

Deduct 5 points unless both transition directions are considered (high to low and low to high) or an argument is given as to why low to high has longer propagation delay.

Problem 4 Answer: 25 Total Points

Draw the circuits for the attached NAND and NOR gates. Note that the output of the inverter splits into four lines, and each line is attached to a PMOS and an NMOS transistor—just like an inverter input. Therefore, we can model these two gates, in terms of capacitance contributed to propagation delay, as four inverters (each gate is 2 inverters).

I did not specify whether to allow one interconnect capacitance per gate or per input, so:

One Possible Answer:

Using one interconnect capacitance per gate:

Low to high transition:

$t_p = 0.69\ \tau = 0.69\ R_{N1}[C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2\ C_I]$

$= 0.69 \times 3000\ \Omega\ [50 + 50 + 4(50 + 75) + 2(100)]$ fF = **1.66 ns**

High to low transition:

$t_p = 0.69\ \tau = 0.69\ R_{P1}[C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2\ C_I]$

$= 0.69 \times 2000\ \Omega\ [50 + 50 + 4(50 + 75) + 2(100)]$ fF = **1.10 ns**

The Other Possible Answer:

Using one interconnect capacitance per input:

Low to high transition:

$t_p = 0.69\ \tau = 0.69\ R_{N1}[C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2\ C_I]$

$= 0.69 \times 3000\ \Omega\ [50 + 50 + 4(50 + 75) + 4(100)]$ fF = **2.07 ns**

High to low transition:

$t_p = 0.69\ \tau = 0.69\ R_{P1}[C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2\ C_I]$

$= 0.69 \times 2000\ \Omega\ [50 + 50 + 4(50 + 75) + 4(100)]$ fF = **1.38 ns**