Problem 1 Answer: 25 Total Points

When \( V_{IN} = 1.5 \) V, \( V_{OUT} = 1.5 \) V.

\[ V_{GS(N)} = V_{IN} = 1.5 \text{ V} \quad V_{DS(N)} = V_{OUT} = 1.5 \text{ V} \]

\[ V_{GS(P)} = V_{IN} - V_{DD} = 1.5 \text{ V} - 5 \text{ V} = -3.5 \text{ V} \quad V_{DS(P)} = V_{OUT} - V_{DD} = 1.5 \text{ V} - 5 \text{ V} = -3.5 \text{ V} \]

\[ I_{D(N)} + I_{D(P)} = 0 \quad \Rightarrow \quad I_{D(N)} = -I_{D(P)} \]

Both transistors are in saturation, so \( I_D = I_{DSAT} \) for each transistor. Substitute into \( I_{D(N)} = -I_{D(P)} \):

\[
I_{DSAT(N)} = -I_{DSAT(P)} = \frac{W_N}{2L_N} \mu N C_{ox} (V_{GS(N)} - V_T(N))^2 = \frac{W_P}{2L_P} \mu P C_{ox} (V_{GS(P)} - V_T(P))^2
\]

\[
W_N = \frac{10^{-6}}{2x1.5x10^{-6}} \frac{500x10^{-4} \text{ m}^2}{(Vs)} \frac{5x10^{-15} \text{ F}}{10^{-12} \text{ m}^2} (1.5 \text{ V} - 1 \text{ V})^2
\]

\[
= \frac{10^{-6}}{2x1.5x10^{-6}} \frac{250x10^{-4} \text{ m}^2}{(Vs)} \frac{5x10^{-15} \text{ F}}{10^{-12} \text{ m}^2} (-3.5 \text{ V} - 1 \text{ V})^2
\]

\[ W_N = 125 \mu \text{m} \]

Problem 2 Answer: 25 Total Points

Propagation delay from high to low involves \( R_{P1}, C_{DB(N1)}, C_{DB(P1)}, C_{GB(N2)}, C_{GB(P2)}, \) and \( C_t \).

To find \( R_{P1} \), take the average of \( V_{DS(P1)/I_{D(P1)}} \) when \( V_{DS(P1)} \) is at full voltage and when it has transitioned halfway. That is:

\[
R_{P1} = \frac{1}{2} \left( \frac{-V_{DD}}{I_{DSAT(P1)}} + \frac{-V_{DD}/2}{I_{DSAT(P1)}} \right) = \frac{-0.75V_{DD}}{\frac{W_P}{2L_P} \mu P C_{ox} \frac{t_{ox}}{\epsilon_0} (V_{GS(P1)} - V_T(P1))^2}
\]

\[
= \frac{-0.75 \times 5 \text{ V}}{12x10^{-6} \text{ m} - 250x10^{-4} \text{ m}^2 / (Vs) 4 \times 8.85x10^{-12} \text{ F/m} \times 10^{-9} \text{ m} (-5 \text{ V} - (-1 \text{ V}))^2}
\]

\[ R_{P1} = 883 \Omega \]

Note that we do the calculation for \( V_{GS(P1)} \) after the transition has taken place, so:

\[ V_{GS(P1)} = V_{IN} - V_{DD} = 0 - 5 \text{ V} = -5 \text{ V} \]
Compute \( C_{GB(P2)} \) and \( C_{GB(N2)} \) using parallel place capacitance:

\[
C_{GB(P2)} = \frac{k_{ox} \varepsilon_0}{t_{ox}} W_{PLP} = \frac{4 \times 8.85 \times 10^{-12} F / m}{10 \times 10^{-9} m} (12 \times 10^{-6} m) (2 \times 10^{-6} m) = 85 \text{ fF}
\]

\[
C_{GB(N2)} = \frac{k_{ox} \varepsilon_0}{t_{ox}} W_{NLN} = \frac{4 \times 8.85 \times 10^{-12} F / m}{10 \times 10^{-9} m} (6 \times 10^{-6} m) (2 \times 10^{-6} m) = 42.5 \text{ fF}
\]

Compute \( C_{I} \) using parallel plate capacitance:

\[
C_{I} = \frac{k_{ox} \varepsilon_0}{t_{ox}} W_{LI} = \frac{4 \times 8.85 \times 10^{-12} F / m}{10 \times 10^{-9} m} (30 \times 10^{-6} m) (1 \times 10^{-6} m) = 106 \text{ fF}
\]

With \( C_{DB(P1)} = C_{DB(N1)} = 50 \text{ fF} \), we can now compute the time constant (all the capacitances are in parallel):

\[
\tau = R_{P1} (C_{DB(P1)} + C_{DB(N1)} + n(C_{GB(P2)} + C_{GB(N2)} + C_{I})) = 883 \Omega \ (50 + 50 + 85 + 42.5 + 106) \text{ fF} = 295 \text{ ps}
\]

The propagation delay is 0.69 \( \tau \) :

\[ t_p = 207 \text{ ps} \]

**Problem 3 Answer:** 25 Total Points

Low to high transition:

\[ t_p = 0.69 \tau = 0.69 R_{N1}[C_{DB(P1)} + C_{DB(N1)} + n(C_{GB(P2)} + C_{GB(N2)} + C_{I})] \leq 20 \text{ ns} \]

\[ 0.69 \times 3000 \Omega \ [50 + 50 + n(50 + 75 + 100)] \text{ fF} \leq 20 \text{ ns} \]

\[ n \leq 42 \]

High to low transition:

\[ t_p = 0.69 \tau = 0.69 R_{P1}[C_{DB(P1)} + C_{DB(N1)} + n(C_{GB(P2)} + C_{GB(N2)} + C_{I})] \leq 20 \text{ ns} \]

\[ 0.69 \times 2000 \Omega \ [50 + 50 + n(50 + 75 + 100)] \text{ fF} \leq 20 \text{ ns} \]

\[ n \leq 63 \]

Conclusion: Fan-out is 42 gates.

Deduct 5 points unless both transition directions are considered (high to low and low to high) or an argument is given as to why low to high has longer propagation delay.
**Problem 4 Answer**: 25 Total Points

Draw the circuits for the attached NAND and NOR gates. Note that the output of the inverter splits into four lines, and each line is attached to a PMOS and an NMOS transistor—just like an inverter input. Therefore, we can model these two gates, in terms of capacitance contributed to propagation delay, as four inverters (each gate is 2 inverters).

I did not specify whether to allow one interconnect capacitance per gate or per input, so:

**One Possible Answer:**

Using one interconnect capacitance per gate:

Low to high transition:

\[ t_p = 0.69 \tau = 0.69 \, R_{N1} \left[ C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2 \, C_i \right] \]

\[ = 0.69 \times 3000 \, \Omega \left[ 50 + 50 + 4(50 + 75) + 2(100) \right] \text{fF} = 1.66 \text{ ns} \]

High to low transition:

\[ t_p = 0.69 \tau = 0.69 \, R_{P1} \left[ C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2 \, C_i \right] \]

\[ = 0.69 \times 2000 \, \Omega \left[ 50 + 50 + 4(50 + 75) + 2(100) \right] \text{fF} = 1.10 \text{ ns} \]

**The Other Possible Answer:**

Using one interconnect capacitance per input:

Low to high transition:

\[ t_p = 0.69 \tau = 0.69 \, R_{N1} \left[ C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2 \, C_i \right] \]

\[ = 0.69 \times 3000 \, \Omega \left[ 50 + 50 + 4(50 + 75) + 4(100) \right] \text{fF} = 2.07 \text{ ns} \]

High to low transition:

\[ t_p = 0.69 \tau = 0.69 \, R_{P1} \left[ C_{DB(P1)} + C_{DB(N1)} + 4(C_{GB(P2)} + C_{GB(N2)}) + 2 \, C_i \right] \]

\[ = 0.69 \times 2000 \, \Omega \left[ 50 + 50 + 4(50 + 75) + 4(100) \right] \text{fF} = 1.38 \text{ ns} \]