Problem 1: MOSFET subthreshold leakage

For a MOSFET operating in the subthreshold regime (\( V_{GS} < V_T \)), the reduction in gate voltage needed to reduce the drain current by one decade is defined as the “subthreshold swing”:

\[
S = n \left( \frac{kT}{q} \right) (\ln 10)
\]

The units of \( S \) are mV/decade. A small value of \( S \) is desirable, because it allows a low OFF current (\( I_{DS} \) at \( V_{GS} = 0 \) V) to be achieved with a low threshold voltage (desirable for high ON current \( I_{DSAT} \)). Note that the smallest value of \( S \) attainable at room temperature (300K) is 60 mV/decade.

Consider an n-channel MOSFET for which the factor \( n = 1.15 \). The threshold voltage for this device is defined to \( V_{GS} \) at which the normalized drain current \( I_D/(W/L) \) reaches 100 nA, with \( V_{DS} = 100 \) mV.

a) Find \( S \)

b) Suppose the leakage current must be less than 100 pA when \( V_{GS} = 0 \) V and \( V_{DS} = 100 \) mV, for \( W = L \). What is the minimum threshold voltage this device can have?

c) For ultralow-power technology (such as that used for memory chips used in portable electronic devices, e.g. cell phones) the leakage current requirement is much more stringent, typically less than 0.1 pA. Qualitatively, how would the transistor drive current (\( I_{DSAT} \)) for such a technology compare with that of the technology described in part (b)?

Problem 2: The MOSFET as a resistive switch

For digital circuit applications, the MOSFET can be modeled simply as a resistor in the ON state (\( V_{GS} = V_{DD} \), the power-supply voltage). Its equivalent resistance in the ON state is

\[
R_{eq} \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)
\]

where \( I_{DSAT} \) is the drain saturation current and \( \lambda \) is the channel-length modulation parameter.

a) Consider a long n-channel MOSFET (refer to Slide 8 of Lecture 25 for the appropriate \( I_{DSAT} \) equation) of dimensions \( W = 100 \) µm and \( L = 10 \) µm, for which \( k_n' = 50 \) µA/V², \( V_T = 0.7 \) V, and \( \lambda = 0 \). Calculate its equivalent resistance in the ON state, for \( V_{DD} = 5 \) V.

b) In general, a lower ON-state resistance (\( R_{eq} \)) is desirable for achieving faster circuit speed (i.e. lower propagation delay). Describe at least two approaches to lowering \( R_{eq} \).

c) Consider a very-short n-channel MOSFET (refer to Slide 11 of Lecture 25 for the appropriate \( I_{DSAT} \) equation) of dimensions \( W = 1 \) µm and \( L = 0.1 \) µm, for which \( C_{ox} = 2 \) µF/cm², \( V_T = 0.4 \) V, and \( \lambda = 0.1 \). Calculate its equivalent resistance in the ON state, for \( V_{DD} = 1 \) V. Assume that the saturation velocity \( v_{sat} = 10^7 \) cm/s, and that the electron mobility \( \mu_n = 300 \) cm²/Vs.
Problem 3: Common-source amplifier circuit
Consider the following amplifier circuit:

The n-channel MOSFET has dimensions $W = 20 \, \mu m$ and $L = 2 \, \mu m$, and $k_n' = 100 \, \mu A/V^2$, $V_T = 0.5 \, V$, and $\lambda = 0$.

a) Sketch the $i_D$ vs. $v_{DS}$ characteristics of the MOSFET to scale, for $v_{GS} = 1, 2, 3, 4$ and 5 V. Draw the load line on the $i_D$ vs. $v_{DS}$ plot.

b) Draw the voltage transfer function ($v_{OUT}$ vs. $v_{IN}$).

c) What is the optimal DC operating point (“Q point”) for this circuit? (Specify the value for $V_{BIAS}$.) Estimate the open-circuit voltage gain $A_v = \frac{v_{out}}{v_{in}}$ for this operating point.